

700 V, 165 mΩ typ., 10 A, e-mode PowerGaN transistor

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT240R70ITK	700 V	240 mΩ	10 A	G-HEMT

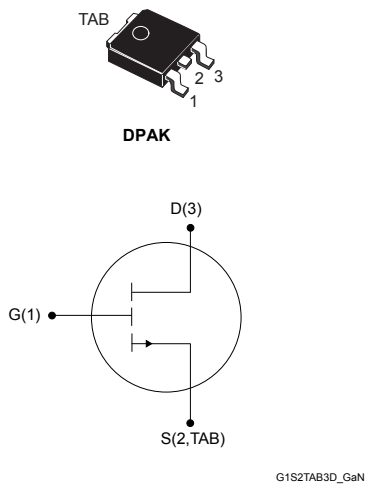
- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Zero reverse recovery charge
- ESD safeguard

Applications

- Adapters for tablets, notebook and AIO
- DC-DC converters
- USB type-C PD adapters and quick chargers

Description

The **SGT240R70ITK** is a 700 V, 10 A e-mode PowerGaN transistor. The resulting device provides extremely low conduction losses, high current capability and ultra-fast switching operation to enable high power density and unbeatable efficiency performances.



Product status link

[SGT240R70ITK](#)

Product summary

Order code	SGT240R70ITK
Marking	240R70I
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700 ⁽¹⁾	V
	Drain-source voltage (transient, $t_p < 200\text{ }\mu\text{s}$)	800	
V_{GS}	Gate-source voltage	-6 to 7	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	10 ⁽²⁾	A
I_{DM}	Pulse drain current ($t_p = 10\text{ }\mu\text{s}$)	18	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	77	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.
2. Limited by design.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.62	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	55 ⁽¹⁾	°C/W

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$		0.4	20	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$		5		
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$		50		μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 11\text{ mA}$	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 6\text{ V}, I_D = 3\text{ A}$		165	240	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 3\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$		360		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 100\text{ kHz}$	-	79	-	pF
C_{oss}	Output capacitance		-	25	-	pF
C_{rss}	Reverse transfer capacitance		-	0.2	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }400\text{ V}$	-	36	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	52	-	pF
R_g	Intrinsic gate resistance	$f = 5\text{ MHz}, I_D = 0\text{ A}$	-	6	-	Ω
V_{plat}	Gate plateau voltage	$V_{DS} = 400\text{ V}, I_D = 3\text{ A}$	-	2.5	-	V
Q_g	Total gate charge	$V_{GS} = 0\text{ to }6\text{ V}, V_{DS} = 400\text{ V}, I_D = 3\text{ A}$	-	2	-	nC
Q_{gs}	Gate-source charge		-	0.2	-	nC
Q_{gd}	Gate-drain charge		-	0.7	-	nC
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	-	0	-	nC
Q_{oss}	Output charge		-	21	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}, I_D = 6\text{ A}, V_{GS} = 6\text{ V},$ $R_{G(on)} = 10\text{ }\Omega, R_{G(off)} = 2\text{ }\Omega, L = 318\text{ }\mu\text{H}$	-	2	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	4	-	ns
t_f	Fall time		-	6	-	ns

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 3\text{ A}$	-	2.6	-	V

2.1 Electrical characteristics (curves)

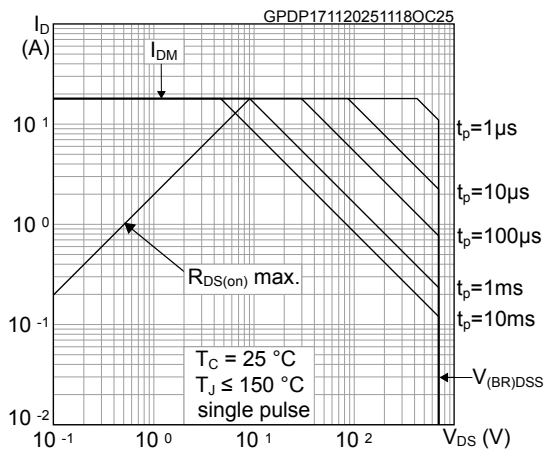
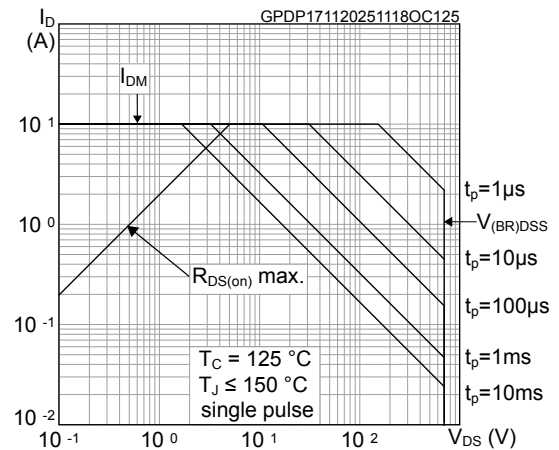
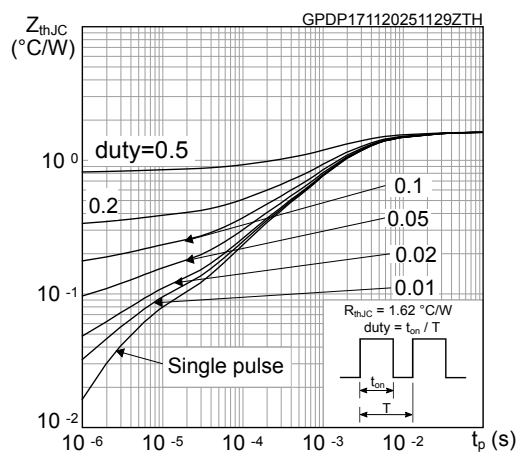
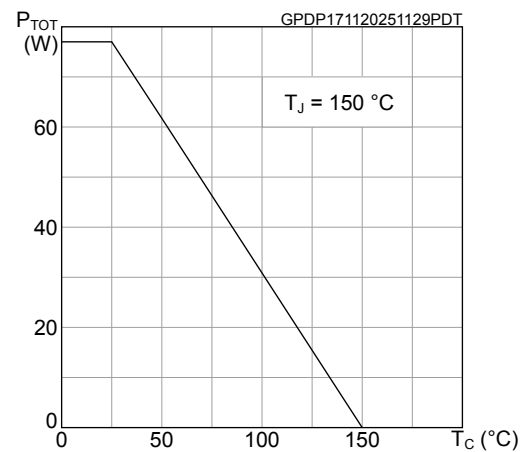
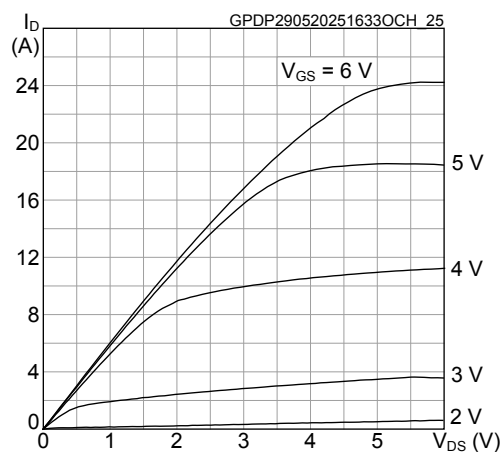
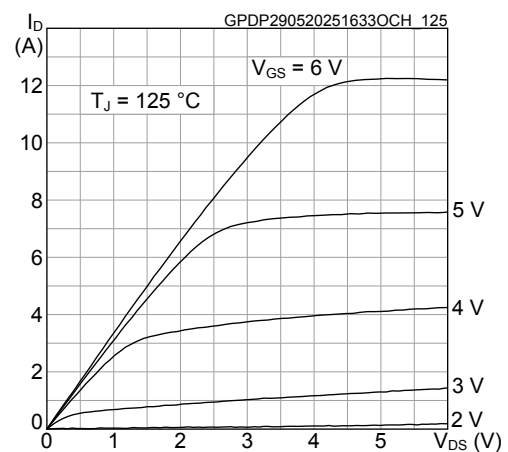
Figure 1. Safe operating area ($T_C = 25^\circ\text{C}$)

Figure 2. Safe operating area ($T_C = 125^\circ\text{C}$)

Figure 3. Maximum transient thermal impedance

Figure 4. Total power dissipation

Figure 5. Typical output characteristics ($T_J = 25^\circ\text{C}$)

Figure 6. Typical output characteristics ($T_J = 125^\circ\text{C}$)


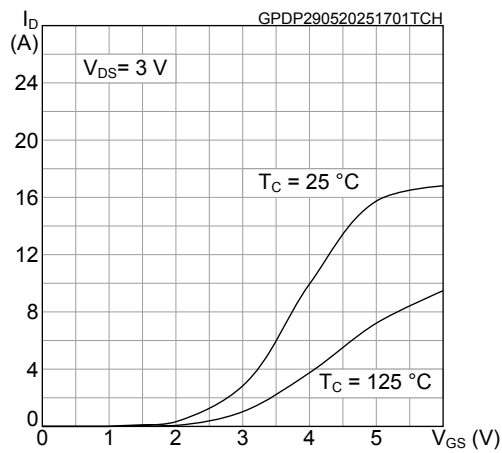
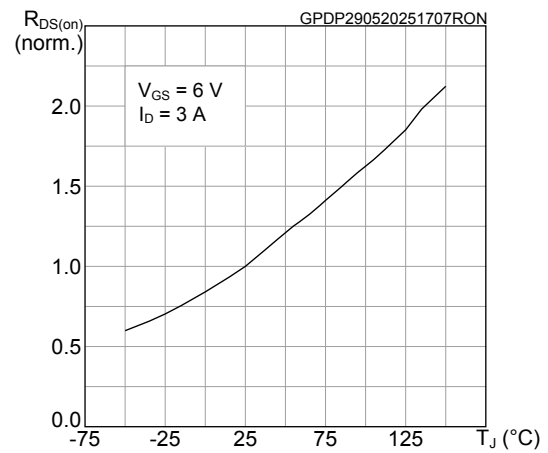
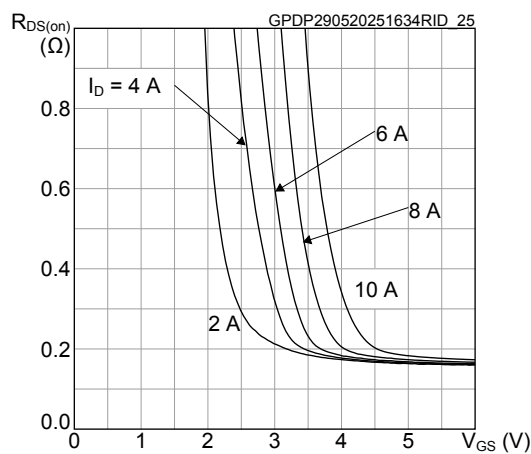
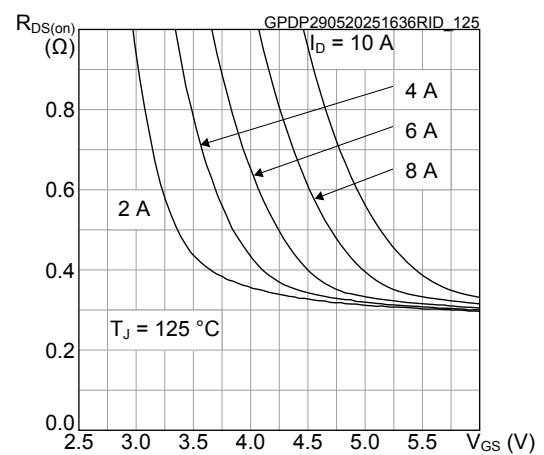
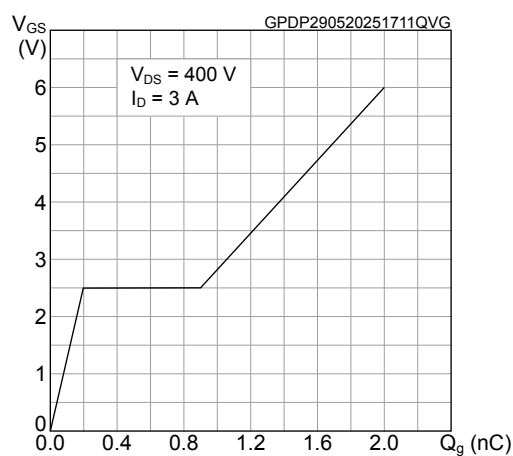
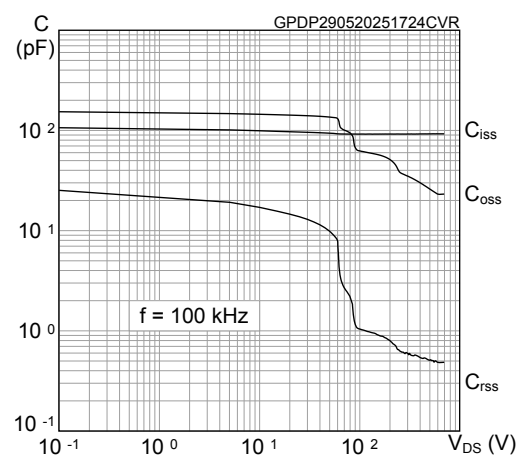
Figure 7. Typical transfer characteristics

Figure 8. Normalized on-resistance vs temperature

Figure 9. Typical drain-source on-resistance ($T_J = 25 \text{ }^{\circ}\text{C}$)

Figure 10. Typical drain-source on-resistance ($T_J = 125 \text{ }^{\circ}\text{C}$)

Figure 11. Typical gate charge characteristics

Figure 12. Typical capacitance characteristics


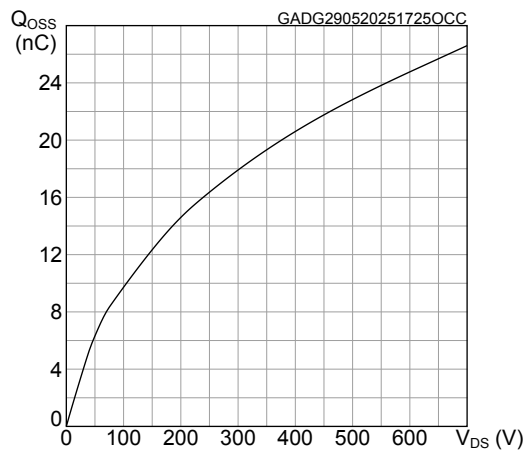
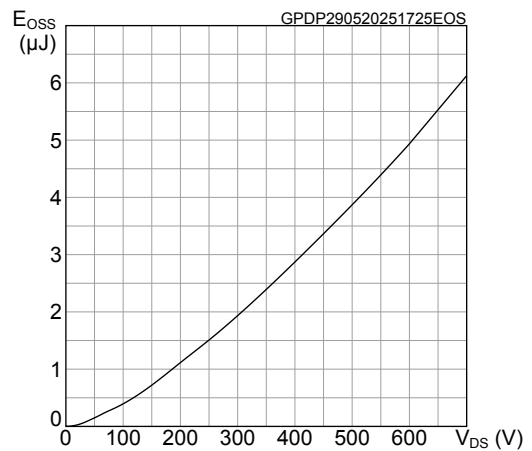
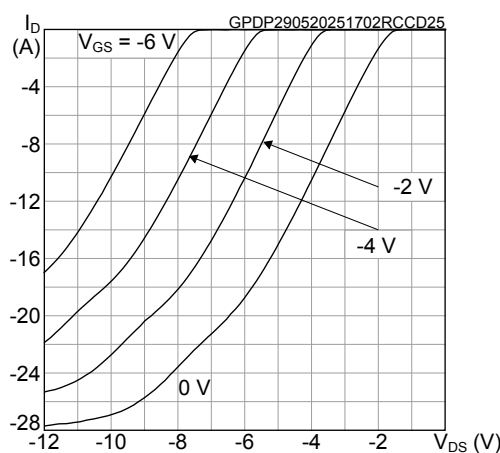
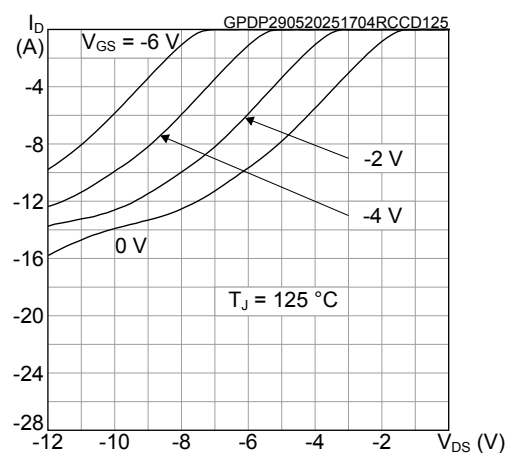
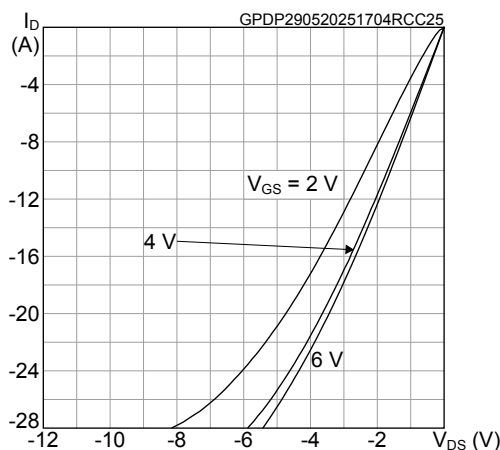
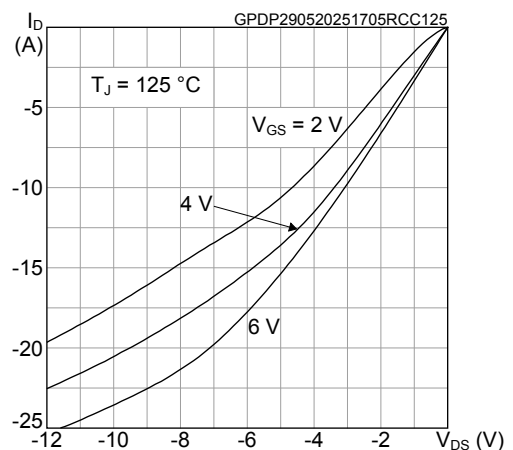
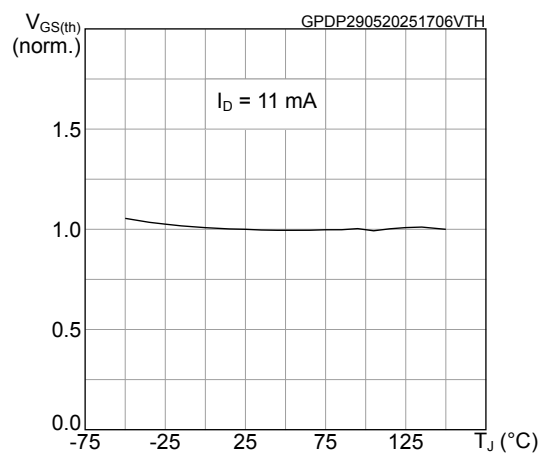
Figure 13. Typical output capacitance charge

Figure 14. Typical output capacitance stored energy

Figure 15. Typical diode reverse conduction characteristics ($T_J = 25^\circ C$)

Figure 16. Typical diode reverse conduction characteristics ($T_J = 125^\circ C$)

Figure 17. Typical reverse conduction characteristics ($T_J = 25^\circ C$)

Figure 18. Typical reverse conduction characteristics ($T_J = 125^\circ C$)


Figure 19. Normalized gate threshold vs temperature



3 Test circuits

Figure 20. Test circuit for inductive load switching times

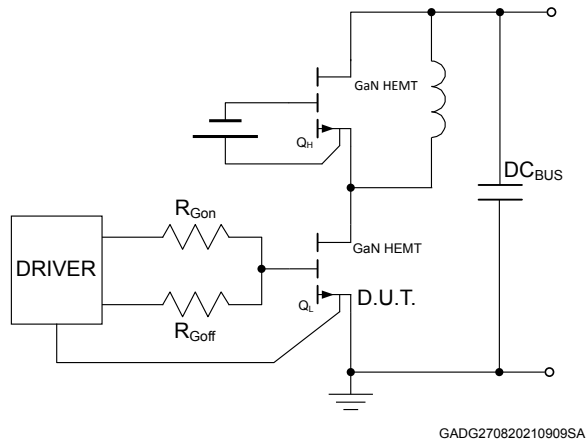
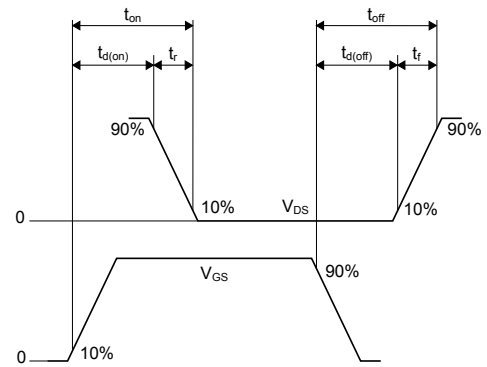


Figure 21. Switching time waveforms



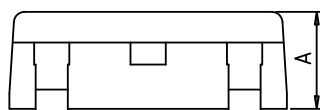
AM01473v1

4 Package information

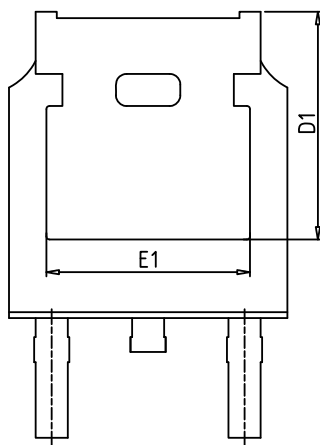
To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type L for PowerGaN package information

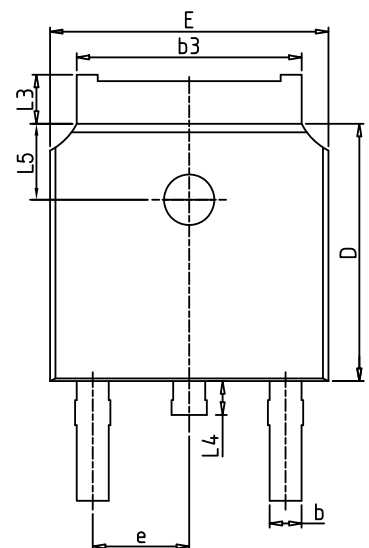
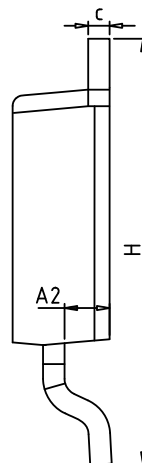
Figure 22. DPAK (TO-252) type L for PowerGaN package outline



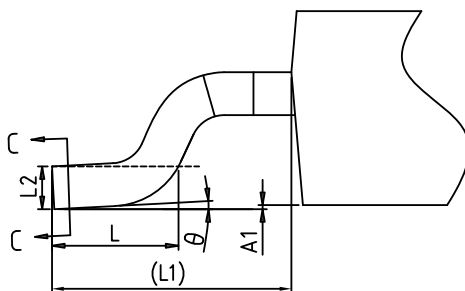
SIDE VIEW



BOTTOM VIEW



TOP VIEW

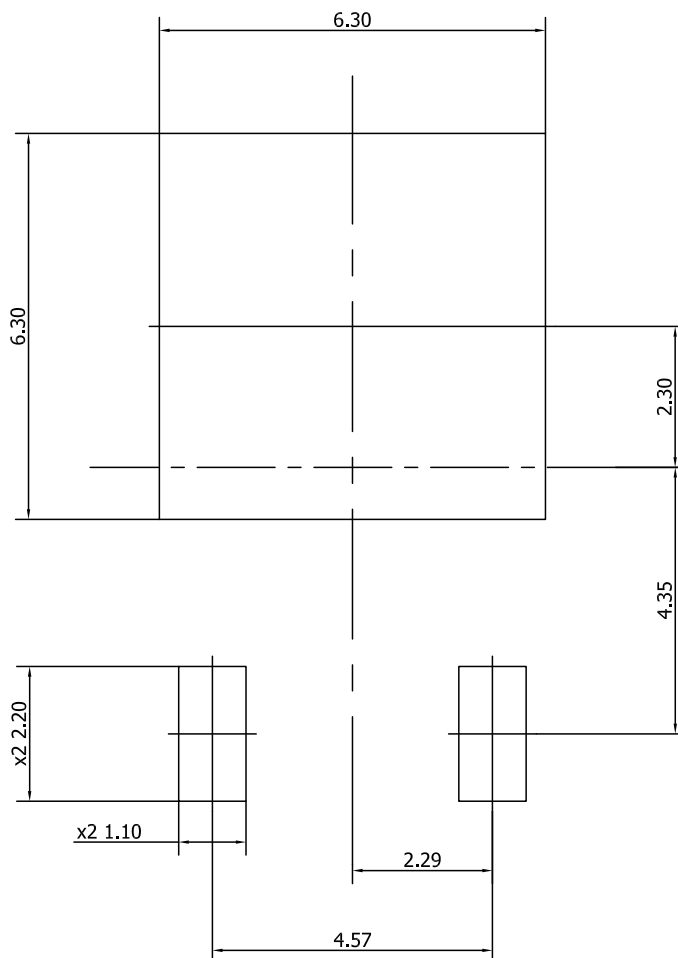


0068772_type_L_PowerGaN_rev36

Table 7. DPAK (TO-252) type L for PowerGaN mechanical data

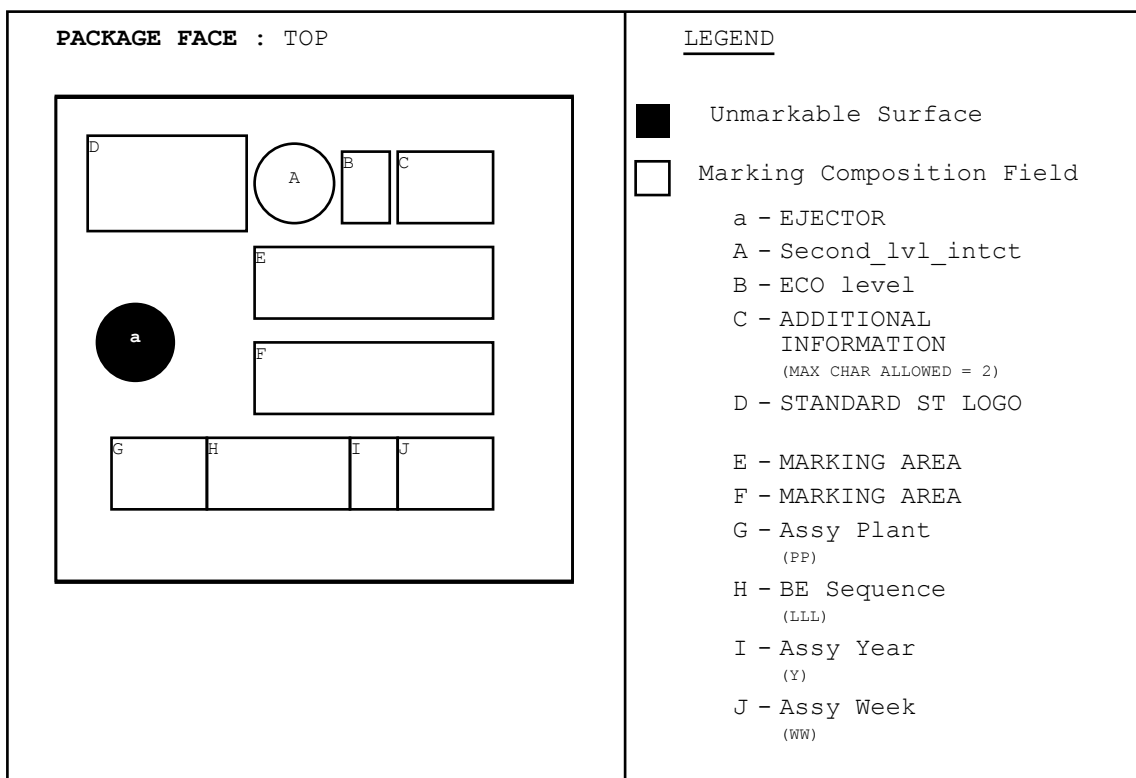
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30 REF		
E	6.40	6.60	6.73
E1	4.63		
e	2.286 BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90 REF		
L2	0.51 BSC		
L3	0.88		1.28
L4	0.50		1.00
L5	1.65	1.80	1.95
V2	0°		8°

Figure 23. DPAK (TO-252) type L for PowerGaN recommended footprint (dimensions are in mm)



FP_type_L_PowerGaN_0068772_36

Figure 24. Marking composition for DPAK (TO-252) type L for PowerGaN for PowerGaN



CD00330413_Rev.2

Engineering samples

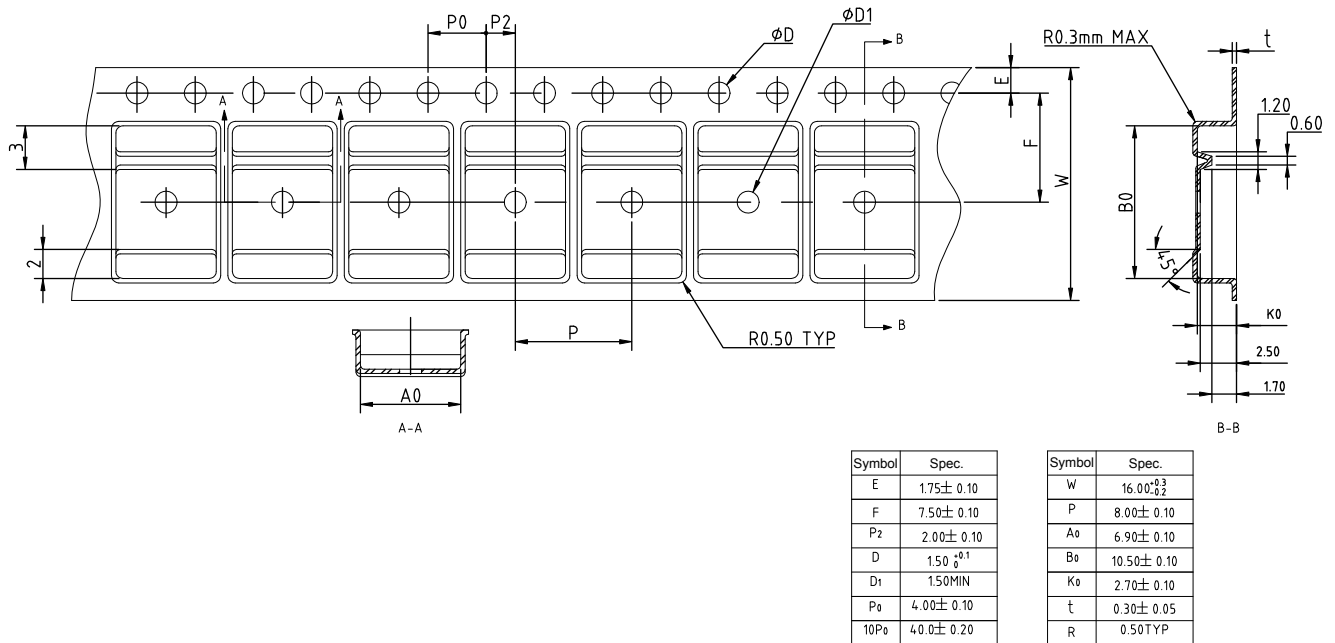
These samples are clearly identified by "ES" digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

4.2 DPAK (TO-252) type L for PowerGaN packing information

Figure 25. DPAK (TO-252) type L for PowerGaN tape drawing (dimensions are in mm)



069909_typeL_GaN_12

Revision history

Table 8. Document revision history

Date	Revision	Changes
02-Dec-2025	1	First release.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	9
4	Package information	10
4.1	DPAK (TO-252) type L for PowerGaN package information	10
4.2	DPAK (TO-252) type L for PowerGaN packing information	14
	Revision history	15

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved