Datasheet

Nitrogen95 SMARC

Version 0.3

Revision History

Version	Date	Notes	Contributors	Approver
0.1	19 February 2025	Preliminary Release	Jody Van	Dan Kephart
0.2	27 June 2025	Updates to Block Diagram. Updated with new part numbering scheme and parts with NX611 wireless.	Jody Van Gary Bisson Dan Kephart	Dan Kephart
0.3	19 Sept 2025	Preliminary release.	Dave Drogowski	Dan Kephart

Contents

1 Scope

This document describes key hardware aspects of Ezurio's Nitrogen95 SMARC system-on-module which is based on the i.MX 95 processor family and the Sona family Wi-Fi/BT combo radio. Data in this document is drawn from several sources and includes information found in the documentation for NXP's i.MX 95 and our Sona family.

Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 Introduction

The Nitrogen95 SMARC is an integrated platform solution with up to six Arm Cortex A55 cores, a high-performance real-time domain with Arm Cortex M7, and low-power/safety domain with Arm Cortex M33, each able to access interfaces including CAN-FD, 10GbE networking, PCIe Gen 3 x1 interfaces, and accelerators such as V2X, ISP, and VPU. The i.MX 95 family enables machine vision through its integrated eIQ Neutron NPU as part of a vision processing pipeline for use with multiple camera sensors or network attached smart cameras.

Additionally, it offers the latest high-speed interfaces for connectivity and fast data transfer with 2x PCIe Gen 3.0, 1x USB 2.0 Type C, 2x USB 3.0, 1x USB 2.0, 3x SD/SDIO 3.01, 2x 1 Gbps Ethernet with TSN, 1x 10 Gbps Ethernet with TSN, IEEE 1588, EEE, in addition to 2x CAN-FD interfaces. The memory interfaces supported are 16-bit LPDDR5X and eMMC 5.1.

The module also includes 2x 4-lane MIPI-CSI camera and optional ISP interfaces capable of supporting 1x 4Kp60, 2x 4Kp30, 4x 1080p60, or 8x 1080p30

The i.MX 95 family implements security via NXP's EdgeLock® secure enclave, a preconfigured, self-managed and autonomous security subsystem. EdgeLock eases the complexity of implementing robust, device-wide security intelligence for IoT applications through autonomous management of critical security functions, such as root of trust, run-time attestation, trust provisioning, secure boot, key management and cryptographic services while also simplifying the path to industry-standard security certifications.

The Nitrogen95 SMARC includes the Sona family which is pre-calibrated and integrates the complete transmit/receive RF paths including bandpass filter, diplexer, switches, reference crystal oscillator, and power management units (PMU). Three RF connectors (MHF4) on the module provide the most flexibility for antenna selection, installation and performance. Two ports for WLAN and one dedicated for Bluetooth. Several high-performance antennas are certified with the Sona family onboard the Nitrogen95 SMARC.

The Nitrogen95 SMARC has several product SKUs providing different eMMC and LPDDR5 memory configurations, see Ordering Information section.

3 Nitrogen95 SMARC Features Summary

The Nitrogen95 SMARC module complies with the SMARC v2.1 specification from SGET.

Key features of Nitrogen95 SMARC are described in Table 1.

Table 1: Key Features of Nitrogen95 SMARC

Feature	Description
CPU	Six Cortex®-A55 processors operation up to 2.0 GHz • Arm v8.2 fully 64-bit capable • L1, L2, and L3 cache with ECC Cortex®-M33 core platform operating up to 333 MHz Cortex®-M7 core platform operating up to 800 MHz • Arm v8-M supporting Trustzone-M • 16 kB + 16 kB / 32 kB + 32 kB cache (ECC) • 256 kB / 512 kB Tightly Coupled Memory (TCM) / on-chip SRAM (ECC)
Memory interface	• On module: 16-bits LPDDR5 with inline ECC (size, please refer to Ordering Information) • On module: 8-bits eMMC 5.1 with HS400 speed (size, please refer Ordering Information) • On carrier: 1 SDXC (4-bit, with extended capacity)
Graphics Engine	Arm Mali-G310 Graphic Processing Unit (GPU) • 3D GPU supporting 64 GFLOPs FP32 • OpenGL® ES 3.2 • Vulkan® 1.3 • OpenCL 3.0 Video Processors • 4Kp60 H.265 and H.264 encode and decode • 1x JPEG Encoder • 1x JPEG Decoder
Neutral Processing Unit (NPU)	• 2.0 TOP/s Neural Network performance, up to 1.0 GHz (overdrive mode) and 800 MHz (nominal mode) • 1 MByte of SRAM embedded within the NPU, but it is available for other SoC usage when not using for ML purposes.
Display Controller	• 1x 350 MHz MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4kp30 or 3840 x 1440p60 • 2x 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane)
Camera and ISP Interface	• MIPI-CSI and ISP (2x 4-lane, 2.5 Gbps/lane) with PHY (one mux'd with DSI) • Up to 1x 4Kp60 fps (if one MIPI CSI is enabled), 2x 4Kp30, 4x 1080p60, or 8x 1080p30 • Up to 8x cameras with MIPI virtual channels • 96 kByte of SRAM, but it is available for other SoC usage when not using for ISP purposes
Audio	• 17-lane I2S TDM (32-bit at 768 kHz frequency) • SPDIF Rx and SPDIF Tx • 8-channel PDM Microphone Interface (MICFIL)
Connectivity	• 2x PCIe Gen 3.0 (1-lane) • 1x USB3.0 Type C with PHY • 2x USB3.0 with PHY • 1x USB2.0 with PHY • 2x 1 Gbps Ethernet ports with Time Sensitive Networking (TSN) capabilities • 1x 10 Gbps Ethernet port with Time Sensitive Networking (TSN) capabilities • IEEE 1588 for sync; and EEE • 2x CAN-FD • 4x UART

Feature	Description
Security	• Trusted Resource Domain Controller (TRDC) • Arm® TrustZone® (TZ) architecture • Secure and trusted access control • EdgeLock® secure enclave • Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, fine-grain key management augmented by extensive crypto services
Debug Interface	• Arm CoreSight® debug and trace architecture • Trace Port Interface Unit (TPIU) to support off-chip real-time trace • Support for 4-pin (JTAG) and SWD debug interfaces

4 Block Diagram

The figure below shows the block diagram of the Nitrogen95 SMARC which contains the NXP i.MX 95 processor, PMIC (PF09/PF53*2) and the Sona family Wi-Fi/BT combo.

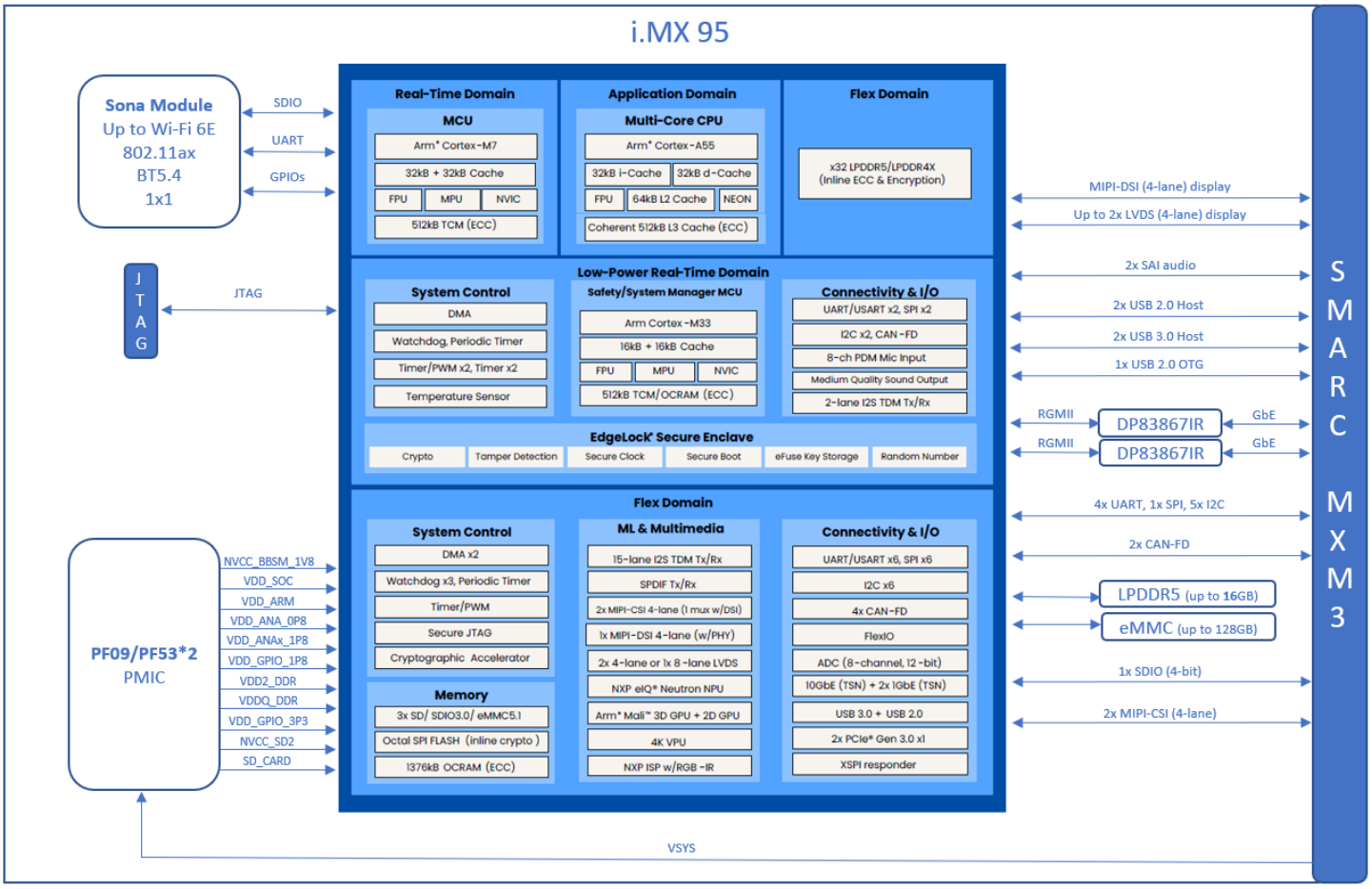


Figure 1: Nitrogen95 SMARC block diagram

Detailed connections between a Sona module and the i.MX 95 are detailed in Table 2 below.

Table 2: Sona IF573 to i.MX 95 Connections

	IF573	i.MX 95
SDIO	SDIO_CLK/CMD/DATA[0:3]	SD3_CLK/SD3_CMD/SD3_DATA0-3
UART	UART_RX/UART_TX/UART_CTS/UART_RTS	GPIO_IO05/ GPIO_IO04/ GPIO_IO07/ GPIO_IO06 (UART6)
CLK	SUSCLK	CCM_CLKO4
BT_EN	W_DISABLE2#	P0_2 (from U21 GPIO expander)
BT_IRQ	UART_WAKE#	
WL_EN	W_DISABLE1#	P1_4 (from U21 GPIO expander)
WL_IRQ	SDIO_WAKE#	P0_0 (from U21 GPIO expander)

5 DC Power Tree

The Nitrogen95 SMARC requires a primary 5V input (VSYS) as its main power source. This inputs powers the on-module NXP PPF0900AVNA1ES power management IC (PMIC), which generates all necessary voltages for the module's components. Additional power management is provided by the PPF5302AVNAAEP and PPF5301AVNABEP PMICs.

5.1 Power Modes Diagram

NXP PPF0900AVNA1ES has ten power modes: ULPOFF, LPOFF, DBGOFF, Self-Test, PWRUP, RUN, STANDBY, PWRDN, Fail-Safe and Deep Fail Safe. Below figure shows the state transition diagram showing the conditions to enter and exit each state.

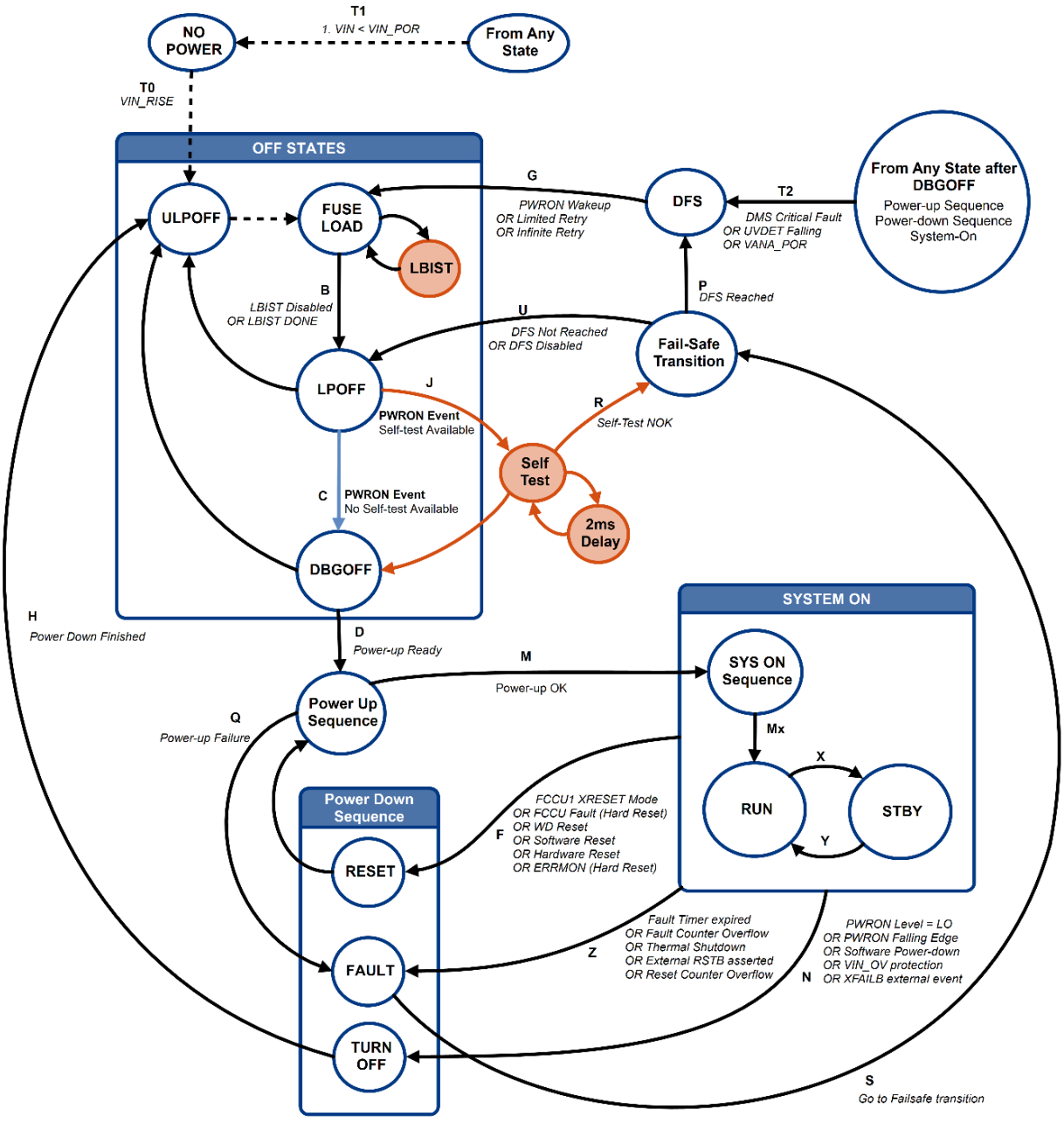


Figure 2: State transition diagram for PMIC

- **ULPOFF Mode:**
  The ULPOFF (Ultra-low power off) state is provided to allow the PMIC to remain in an OFF condition with minimum functional operation, minimum quiescent current and the ability to wake-up if the PWRON pin is asserted high.
- **LPOFF Mode:**
  During the LPOFF (Low power off) state, only the VAON regulator can be enabled if it is configured as an always-on supply via the OTP configuration. All other system regulators will remain disabled until the power-up sequence is started.
- **DBGOFF Mode:**
  During normal system operation, the DBGOFF (Debug Off) state will be a transitory state between a power-on event and the Power-up sequence. It serves as the gating state to ensure the PMIC is ready to start a power up sequence and allow synchronization of two or more PMICs providing full power architecture to a complex system.
- **Self-Test Mode:**
  In devices with a high safety integrity level (ASIL/SIL) the Self-test routine is performed when the state machine transitions out of the LPOFF state. During the self-test, the PF09 performs a startup self-check routine to verify the integrity of the system:
  - The high-speed oscillator circuit is operating within a maximum of 6% tolerance.
  - The output of both the voltage generation bandgap and the monitoring bandgap are not drifting apart from each other.
  - A CRC is performed on the Mirror Registers during the self-test routine, to ensure the integrity of the OTP registers before powering up.
  - Analog built-in test on all voltage monitors and Safety I/Os is performed.
- **PWRUP Mode:**
  The PF09 provides a highly configurable power-up sequence to enable the system regulators and general-purpose IO pins in a specific order and timing during the power-up state. The default configuration for the power-up sequence is loaded from the OTP registers to ensure the system always turns on with the correct configuration every power-up cycle as defined on each specific part number.
- **RUN Mode:**
  If the Power-up sequence is completed successfully, the state machine transitions directly into the RUN state. The RUN State is a full featured state providing full functionality and monitoring as described in this document.
- **STANDBY Mode:**
  The STANDBY state is a secondary functional state with programable functionality to prioritize either system monitoring or low power operation.
- **PWRDN Mode:**
  Three types of events may lead to the Power-down sequence.
  - **TURNOFF**: Non-faulty Turn off events move directly into the corresponding Low power state as soon as the power down sequence is finalized.
  - **FAULT:** Turn off events due to a PMIC fault will move into the Fail-Safe transition as soon as the power down sequence is finalized.
  - **RESET:** A RESET state is provided to allow the system to refresh the configuration without looping through a full power cycle.
- **Fail-Safe Mode:**
  During the Fail-safe transition, the VAON remains enabled if it is configured as an Always-on regulator. All system regulators will remain disabled until the next power-up sequence.
- **Deep Fail Safe Mode:**
  The DFS state is intended to work as a temporary lockdown state upon a cyclic critical failure condition. Since the system may land in the DFS state and remain there indefinitely, the DFS state is designed to consume as little current as possible, with just the minimum blocks enabled to perform the operations defined in this state.

6 Boot mode

The Nitrogen95 SMARC module contains a switch (***SW1***) connected to BOOT_MODE0 thus allowing to switch from internal fuses boot (eMMC by default) to USB serial downloader.

The other boot mode signals (BOOT_MODE[1-3]) are not exposed to the carrier as used for different functions (UART/I2S). But a BOM change can select a custom boot mode (see resistors R128 to R135).

This allows more combinations as shown in Table 3.

Table 3: Boot mode combinations

BOOT_MODE [3:0]	BOOT CORE	BOOT MODE
1000	Cortex-M33	LPB: Boot From Internal Fuses
1001	Cortex-M33	LPB: Serial Downloader (USB1)
1010	Cortex-M33	LPB: USDHC1 8-bit 1.8V eMMC 5.1
1011	Cortex-M33	LPB: USDHC2 4-bit SD 3.0
1100	Cortex-M33	LPB: FlexSPI Serial NOR
1110	Cortex-M33	Infinite Loop Mode
1111	Cortex-M33	Test Mode

7 Electrical Characteristic and Power Consumption

7.1 Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Nitrogen95 SMARC product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
$T_{STORAGE}$	Storage Temperature Range	-40	+125	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	NA	+10	dBm
ESD	Electrostatic discharge tolerance	-2000	+2000	V

7.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS_5V	Input voltage for the SOM	3.8	-	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.
Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please contact Ezurio if you need information and guidance for thermal management.

7.3 DC current consumption

Several power saving modes are available and are listed in Table 6.

Note: These figures are estimates and subject to change.

Table 6: Typical current consumption

Mode	Description	Current (Avg)
Power Saving mode	CPU is on, Stay on Wi-Fi connection only.	659mA
RAM suspend mode	CPU is on, memory and wireless connection are off.	380mA
Stress Test	wifi + eth0 con + eth1 con + iperf 0	1114mA
Stress Test	wifi + eth0 con + eth1 con + CPU/GPU/iperf stress test	1677mA

8 Module pin out and Pinmux table

Table 7 lists the pin multiplexing (PIN-MUX) of the Nitrogen95 SMARC.

PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

NXP process has configurable internal Pull-up (PU) and pull-down (PD) resistor whose values are listed below. During a reset condition, the PU and PD state are pre-defined and cannot be changed.

Table 7: Resistor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Pull-up (PU) resistor	VDD=1.65 to 1.95V Temp=0 to 95℃	12	22	49	kΩ
Pull-down (PD) resistor		13	23	48	kΩ
Pull-up (PU) resistor	VDD=3.0 to 3.6V Temp=0 to 95℃	18	37	72	kΩ
Pull-down (PD) resistor		24	43	87	kΩ

Pin configuration for the i.MX is achieved using a suite of evaluation and configuration tools that assists users from initial evaluation to production software development. Users can download the tool from the NXP website: https://www.nxp.com/design/designs/config-tools-for-i-mx-applications-processors:CONFIG-TOOLS-IMX?tab=Design_Tools_Tab

Table 8: Pinout table for Nitrogen95 SMARC edge connector (J2)

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P1	SMB_ALERT#	**SPI:** FLEXSPI1_A_DATA_BIT6 **SAI:** SAI5_TX_BCLK **SAI:** SAI5_RX_DATA_BIT3 **SAI:** NETCMIX_TOP_SAI2_RX_DATA_BIT7 **SPI:** XSPI_DATA_BIT6 **GPIO:** GPIO5_IO_BIT6	DI	1.8V	
P2	GND	NA	-	NA	
P3	CSI1_CK+	MIPI_DSICSI1_CLK_P	DO	1.8V	Populate R228 Depopulate R203
P4	CSI1_CK-	MIPI_DSICSI1_CLK_N	DO	1.8V	Populate R229 Depopulate R204
P5	GBE1_SDP	NA	-	NA	
P6	GBE0_SDP	NA	-	NA	
P7	CSI1_RX0+	MIPI_DSICSI1_D0_P	DI	1.8V	Populate R222 Depopulate R189
P8	CSI1_RX0-	MIPI_DSICSI1_D0_N	DI	1.8V	Populate R223 Depopulate R190
P9	GND	NA	-	NA	
P10	CSI1_RX1+	MIPI_DSICSI1_D1_P	DI	1.8V	Populate R224 Depopulate R191
P11	CSI1_RX1-	MIPI_DSICSI1_D1_N	DI	1.8V	Populate R225 Depopulate R192
P12	GND	NA	-	NA	
P13	CSI1_RX2+	MIPI_DSICSI1_D2_P	DI	1.8V	Populate R226 Depopulate R193

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P14	CSI1_RX2-	MIPI_DSICSI1_D2_N	DI	1.8V	Populate R227 Depopulate R194
P15	GND	NA	-	NA	
P16	CSI1_RX3+	MIPI_DSICSI1_D3_P	DI	1.8V	Populate R230 Depopulate R207
P17	CSI1_RX3-	MIPI_DSICSI1_D3_N	DI	1.8V	Populate R231 Depopulate R208
P18	GND	NA	-	NA	
P19	GBE0_MDI3-	TD_M_D	DI/O	1.8V	From DP83867IRRGZ (U14)
P20	GBE0_MDI3+	TD_P_D	DI/O	1.8V	From DP83867IRRGZ (U14)
P21	GBE0_LINK100#	LED_0	DO	3.3V	From DP83867IRRGZ (U14)
P22	GBE0_LINK1000#	LED_1	DO	3.3V	From DP83867IRRGZ (U14)
P23	GBE0_MDI2-	TD_M_C	DI/O	1.8V	From DP83867IRRGZ (U14)
P24	GBE0_MDI2+	TD_P_C	DI/O	1.8V	From DP83867IRRGZ (U14)
P25	GBE0_LINK_ACT#	LED_2	DO	3.3V	From DP83867IRRGZ (U14)
P26	GBE0_MDI1-	TD_M_B	DI/O	1.8V	From DP83867IRRGZ (U14)
P27	GBE0_MDI1+	TD_P_B	DI/O	1.8V	From DP83867IRRGZ (U14)
P28	GBE0_CTREF	NA	-	NA	Test point
P29	GBE0_MDI0-	TD_M_A	DI/O	1.8V	From DP83867IRRGZ (U14)
P30	GBE0_MDI0+	TD_P_A	DI/O	1.8V	From DP83867IRRGZ (U14)
P31	SPI0_CS1#	**GPIO**: GPIO2_IO_BIT24 **USDHC**: USDHC3_DATA0 **TPM**: TPM3_CH3 **JTAG**: JTAG_MUX_TDO **SPI**: LPSPI6_PCS1 **FLEXIO**: FLEXIO1_FLEXIO_BIT24	DO	1.8V	
P32	GND	NA	-	NA	
P33	SDIO_WP	NA	-	NA	
P34	SDIO_CMD	**USDHC**: USDHC2_CMD **NET**: NETCMIX_TOP_NETC_TMR_1588_TRIG2 **I3C**: I3C2_PUR **I3C**: I3C2_PUR_B **FLEXIO**: FLEXIO1_FLEXIO_BIT2 **GPIO**: GPIO3_IO_BIT2 **CCM**: CCMSRCGPCMIX_TOP_OBSERVE_1	DI/O	1.8 or 3.3V	
P35	SDIO_CD#	**USDHC**: USDHC2_CD_B **NET**: NETCMIX_TOP_NETC_TMR_1588_TRIG1 **I3C**: I3C2_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT0 **GPIO**: GPIO3_IO_BIT0	DI	1.8 or 3.3V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P36	SDIO_CLK	**USDHC**: USDHC2_CLK **NET**: NETCMIX_TOP_NETC_TMR_1588_PP1 **I3C**: I3C2_SDA **FLEXIO**: FLEXIO1_FLEXIO_BIT1 **GPIO**: GPIO3_IO_BIT1 **CCM**: CCMSRCGPCMIX_TOP_OBSERVE_0	DO	1.8 or 3.3V	
P37	SDIO_PWR_EN	**USDHC**: USDHC2_RESET_B **TIMER**: LPTMR2_ALT2 **NET**: NETCMIX_TOP_NETC_TMR_1588_GCLK **FLEXIO**: FLEXIO1_FLEXIO_BIT7 **GPIO**: GPIO3_IO_BIT7	DO	3.3V	
P38	GND	NA	-	NA	
P39	SDIO_D0	**USDHC**: USDHC2_DATA0 **NET**: NETCMIX_TOP_NETC_TMR_1588_PP2 **CAN**: CAN2_TX **FLEXIO**: FLEXIO1_FLEXIO_BIT3 **GPIO**: GPIO3_IO_BIT3 **CCM**: CCMSRCGPCMIX_TOP_OBSERVE_2	DI/O	1.8 or 3.3V	
P40	SDIO_D1	**USDHC**: USDHC2_DATA1 **NET**: NETCMIX_TOP_NETC_TMR_1588_CLK **CAN**: CAN2_RX **FLEXIO**: FLEXIO1_FLEXIO_BIT4 **GPIO**: GPIO3_IO_BIT4	DI/O	1.8 or 3.3V	
P41	SDIO_D2	**USDHC**: USDHC2_DATA2 **NET**: NETCMIX_TOP_NETC_TMR_1588_PP3 **NET**: NETCMIX_TOP_MQS2_RIGHT **FLEXIO**: FLEXIO1_FLEXIO_BIT5 **GPIO**: GPIO3_IO_BIT5	DI/O	1.8 or 3.3V	
P42	SDIO_D3	**USDHC**: USDHC2_DATA3 **TIMER**: LPTMR2_ALT1 **NET**: NETCMIX_TOP_MQS2_LEFT **NET**: NETCMIX_TOP_NETC_TMR_1588_ALARM1 **FLEXIO**: FLEXIO1_FLEXIO_BIT6 **GPIO**: GPIO3_IO_BIT6	DI/O	1.8 or 3.3V	
P43	SPI0_CS0#	**GPIO**: GPIO2_IO_BIT0 **I2C**: LPI2C3_SDA **SPI**: LPSPI6_PCS0 **UART**: LPUART5_TX **I2C**: LPI2C5_SDA **FLEXIO**: FLEXIO1_FLEXIO_BIT0	DO	1.8V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P44	SPI0_CK	**GPIO**: GPIO2_IO_BIT3 **I2C**: LPI2C4_SCL **SPI**: LPSPI6_SCK **UART:** LPUART5_RTS_B **I2C:** LPI2C6_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT3	DO	1.8V	
P45	SPI0_DIN	**GPIO**: GPIO2_IO_BIT1 **I2C**: LPI2C3_SCL **SPI**: LPSPI6_SIN **UART**: LPUART5_RX **I2C**: LPI2C5_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT1	DI	1.8V	
P46	SPI0_DO	**GPIO**: GPIO2_IO_BIT2 **I2C**: LPI2C4_SDA **SPI**: LPSPI6_SOUT **UART**: LPUART5_CTS_B **I2C**: LPI2C6_SDA **FLEXIO**: FLEXIO1_FLEXIO_BIT2	DO	1.8V	
P47	GND	NA	-	NA	
P48	SATA_TX+	MIPI_CSI1_D2_P	DO		
P49	SATA_TX-	MIPI_CSI1_D2_N	DO		
P50	GND	NA	-	NA	
P51	SATA_RX+	MIPI_CSI1_D3_P	DI		
P52	SATA_RX-	MIPI_CSI1_D3_N	DI		
P53	GND	NA	-	NA	
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NA	-	NA	
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NA	-	NA	
P56	SPI1_CK / ESPI_CK / QSPI_CK	**GPIO**: GPIO3_IO_BIT27 **CCM**: CCMSRCGPCMIX_TOP_CLKO_2 **NET**: NETCMIX_TOP_NETC_TMR_1588_PP1 **FLEX**: FLEXIO1_FLEXIO_BIT27	DO	1.8V	
P57	SPI1_DIN / ESPI_IO_0 / QSPI_IO_0	NA	-	NA	
P58	SPI1_DO / ESPI_IO_1 / QSPI_IO_1	NA	-	NA	
P59	GND	NA	-	NA	
P60	USB0+	USB2_D_P	DI/O	3.3V	
P61	USB0-	USB2_D_N	DI/O	3.3V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P62	USB0_EN_OC#	P2_5	DI	3.3V	From PCAL6524EVJ (U21)
P63	USB0_VBUS_DET	USB2_VBUS	DI	3.3V	
P64	USB0_OTG_ID	USB2_ID	DI	3.3V	
P65	USB1+	USB2DN_DP2/PRT_DIS_P2	DI/O	3.3V	From USB5744T/2GX01 (U9)
P66	USB1-	USB2DN_DM2/PRT_DIS_M2	DI/O	3.3V	From USB5744T/2GX01 (U9)
P67	USB1_EN_OC#	PRT_CTL2	DI	3.3V	From USB5744T/2GX01 (U9)
P68	GND	NA	-	NA	
P69	USB2+	USB2DN_DP3/PRT_DIS_P3	DI/O	3.3V	From USB5744T/2GX01 (U9)
P70	USB2-	USB2DN_DM3/PRT_DIS_M3	DI/O	3.3V	From USB5744T/2GX01 (U9)
P71	USB2_EN_OC#	PRT_CTL3	DI/O	3.3V	From USB5744T/2GX01 (U9)
P72	RSVD	ADC_IN0	DI	1.8V	
P73	RSVD	ADC_IN1	DI	1.8V	
P74	USB3_EN_OC#	PRT_CTL1	DI/O	3.3V	From USB5744T/2GX01 (U9)
P75	PCIE_A_RST#	P1_5	DI	1.8V	From PCAL6524EVJ (U21)
P76	USB4_EN_OC#	PRT_CTL4/GANG_PWR	DI/O	3.3V	From USB5744T/2GX01 (U9)
P77	PCIE_B_CKREQ-	NA	-	NA	
P78	PCIE_CLK_REQ	P2_0	DI	1.8V	From PCAL6524EVJ (U21)
P79	GND	NA	-	NA	
P80	PCIE_C_REFCK+	ETH_REF_PAD_CLK_P	DI/O	0.8V	
P81	PCIE_C_REFCK-	ETH_REF_PAD_CLK_N	DI/O	0.8V	
P82	GND	NA	-	NA	
P83	PCIE_A_REFCK+	PCIE_REF_OUT_CLK_P	DI/O	1.8V	
P84	PCIE_A_REFCK-	PCIE_REF_OUT_CLK_N	DI/O	1.8V	
P85	GND	NA	-	NA	
P86	PCIE_A_RX+	PCIE1_RX0_P	DI/O	1.8V	
P87	PCIE_A_RX-	PCIE1_RX0_N	DI/O	1.8V	
P88	GND	NA	-	NA	
P89	PCIE_A_TX+	PCIE1_TX0_P	DI/O	NA	
P90	PCIE_A_TX-	PCIE1_TX0_N	DI/O	NA	
P91	GND	NA	-	NA	
P92	HDMI_D2+ / DP1_LANE0+	NA	-	NA	
P93	HDMI_D2- / DP1_LANE0-	NA	-	NA	
P94	GND	NA	-	NA	
P95	HDMI_D1+ / DP1_LANE1+	NA	-	NA	
P96	HDMI_D1- / DP1_LANE1-	NA	-	NA	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P97	GND	NA	-	NA	
P98	HDMI_D0+ / DP1_LANE2+	NA	-	NA	
P99	HDMI_D0- / DP1_LANE2-	NA	-	NA	
P100	GND	NA	-	NA	
P101	HDMI_CK+ / DP1_LANE3+	NA	-	NA	
P102	HDMI_CK- / DP1_LANE3-	NA	-	NA	
P103	GND	NA	-	NA	
P104	HDMI_HPD / DP1_HPD	NA	-	NA	
P105	HDMI_CTRL_CK / DP1_AUX+	NA	-	NA	
P106	HDMI_CTRL_CK / DP1_AUX-	NA	-	NA	
P107	DP1_AUX_SEL	NA	-	NA	
P108	GPIO0 / CAM0_PWR#	**GPIO**: GPIO2_IO_BIT19 **SAI:** SAI3_RX_SYNC **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT3 **FLEXIO**: FLEXIO1_FLEXIO_BIT19 **SPI**: LPSPI5_SIN **SPI**: LPSPI4_SIN **TPM**: TPM6_CH2 **SAI**: SAI3_TX_DATA_BIT0	DI/O	1.8V	
P109	GPIO1 / CAM1_PWR#	**GPIO**: GPIO2_IO_BIT22 **USD:** USDHC3_CLK **SPD**: SPDIF_IN **CAN**: CAN5_TX **TPM**: TPM5_CH1 **TPM**: TPM6_EXTCLK **I2C**: LPI2C5_SDA **FLEXIO**: FLEXIO1_FLEXIO_BIT22	DI/O	1.8V	
P110	GPIO2 / CAM0_RST#	**GPIO**: GPIO2_IO_BIT23 **USD:** USDHC3_CMD **SPD**: SPDIF_OUT **CAN**: CAN5_RX **TPM**: TPM6_CH1 **I2C**: LPI2C5_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT23	DI/O	1.8V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P111	GPIO3 / CAM1_RST#	**SPI**: FLEXSPI1_A_SCLK **NET:** NETCMIX_TOP_SAI2_RX_DATA_BIT4 **SAI**: SAI4_RX_SYNC **EARC**: EARC_DC_HPD_IN **SPI**: XSPI_CLK **GPIO**: GPIO5_IO_BIT9	DI/O	1.8V	
P112	GPIO4 / HDA_RST#	**SPI**: FLEXSPI1_A_DATA_BIT0 **NET:** NETCMIX_TOP_SAI2_TX_DATA_BIT4 **SAI**: SAI4_TX_BCLK **SAI**: SAI4_RX_DATA_BIT1 **SPI**: XSPI_DATA_BIT0 **GPIO**: GPIO5_IO_BIT0	DI/O	1.8V	
P113	GPIO5 / PWM_OUT	**SPI**: FLEXSPI1_A_DATA_BIT7 **SAI**: SAI5_RX_DATA_BIT0 **SAI**: SAI5_TX_DATA_BIT1 **SPI**: XSPI_DATA_BIT7 **GPIO**: GPIO5_IO_BIT7	DI/O	1.8V	
P114	GPIO6 / TACHIN	**GPIO**: GPIO2_IO_BIT30 **I2C**: LPI2C4_SDA **CAN**: CAN5_TX **FLEXIO**: FLEXIO1_FLEXIO_BIT30	DI/O	1.8V	
P115	GPIO7	**GPIO**: GPIO2_IO_BIT31 **I2C**: LPI2C4_SCL **CAN**: CAN5_RX **FLEXIO**: FLEXIO1_FLEXIO_BIT31	DI/O	1.8V	
P116	GPIO8	**GPIO**: GPIO5_IO_BIT12 **MIX**: HSIOMIX_TOP_PCIE1_CLKREQ_B **UART**: LPUART6_TX **SPI**: LPSPI4_PCS2	DI/O	1.8V	
P117	GPIO9	**GPIO**: GPIO5_IO_BIT13 **UART**: LPUART6_RX **SPI**: LPSPI4_PCS1	DI/O	1.8V	
P118	GPIO10	**SPI**: FLEXSPI1_A_SS0_B **NET:** NETCMIX_TOP_SAI2_RX_DATA_BIT5 **SAI**: SAI4_RX_BCLK **EARC**: EARC_CEC_OUT **SPI**: XSPI_CS **GPIO**: GPIO5_IO_BIT10	DI/O	1.8V	
P119	GPIO11	**SPI**: FLEXSPI1_A_SS1_B **SAI:** SAI5_RX_BCLK **SAI**: SAI5_TX_DATA_BIT3 **NET**: NETCMIX_TOP_SAI2_RX_DATA_BIT7 **GPIO**: GPIO5_IO_BIT11	DI/O	1.8V	
P120	GND	NA	-	NA	
P121	I2C_PM_CK	SC3	DI/O	1.8V	From PCA9546APW (U23)

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P122	I2C_PM_DAT	SD3	DI/O	1.8V	From PCA9546APW (U23)
P123	BOOT_SEL0#	BT_MODE1	DI	1.8V	
P124	BOOT_SEL1#	BT_MODE2	DI	1.8V	
P125	BOOT_SEL2#	BT_MODE3	DI	1.8V	
P126	RESET_OUT#	P1_3	DI/O	1.8V	From PCAL6524EVJ (U21)
P127	RESET_IN#	POR_B	DI	1.8 - 5V	
P128	POWER_BTN#	ONOFF	DI	1.8 - 5V	
P129	SER0_TX	**SPI**: LPSPI4_SOUT **GPIO**: GPIO5_IO_BIT16 **UART**: LPUART7_TX	DO	1.8V	
P130	SER0_RX	**GPIO**: GPIO5_IO_BIT17 **UART**: LPUART7_RX **SPI:** LPSPI4_SCK	DI	1.8V	
P131	SER0_RTS#	**GPIO:** GPIO2_IO_BIT11 **SPI**: LPSPI3_SCK **TMP**: TPM5_EXTCLK **UART**: LPUART7_RTS_B **I2C**: LPI2C8_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT11	DI	1.8V	
P132	SER0_CTS#	**GPIO:** GPIO2_IO_BIT10 **SPI**: LPSPI3_SOUT **TMP**: TPM4_EXTCLK **UART**: LPUART7_CTS_B **I2C**: LPI2C8_SDA **FLEXIO**: FLEXIO1_FLEXIO_BIT10	DO	1.8V	
P133	GND	NA	-	NA	
P134	SER1_TX	**UART**: AONMIX_TOP_LPUART1_TX **UART**: S400_UART_TX **SPI**: AONMIX_TOP_LPSPI2_PCS0 **TPM**: AONMIX_TOP_TPM1_CH1 **GPIO**: AONMIX_TOP_GPIO1_IO_BIT5	DO	1.8V	
P135	SER1_RX	**UART**: AONMIX_TOP_LPUART1_RX **UART**: S400_UART_RX **SPI**: AONMIX_TOP_LPSPI2_SIN **TPM**: AONMIX_TOP_TPM1_CH0 **GPIO**: AONMIX_TOP_GPIO1_IO_BIT4	DI	1.8V	
P136	SER2_TX	**GPIO**: GPIO2_IO_BIT14 **UART**: LPUART3_TX **SPI**: LPSPI8_SOUT **UART**: LPUART8_CTS_B **UART**: LPUART4_TX **FLEXIO**: FLEXIO1_FLEXIO_BIT14	DO	1.8V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P137	SER2_RX	**GPIO**: GPIO2_IO_BIT15 **UART**: LPUART3_RX **SPI**: LPSPI8_SCK **UART**: LPUART8_RTS_B **UART**: LPUART4_RX **FLEXIO**: FLEXIO1_FLEXIO_BIT15	DI	1.8V	
P138	SER2_RTS#	NA	-	NA	
P139	SER2_CTS#	NA	-	NA	
P140	SER3_TX	**UART**: AONMIX_TOP_LPUART2_TX **UART**: AONMIX_TOP_LPUART1_RTS_B **SPI**: AONMIX_TOP_LPSPI2_SCK **TPM**: AONMIX_TOP_TPM1_CH3 **GPIO**: AONMIX_TOP_GPIO1_IO_BIT7	DO	1.8V	
P141	SER3_RX	**UART**: AONMIX_TOP_LPUART2_RX **UART**: AONMIX_TOP_LPUART1_CTS_B **SPI**: AONMIX_TOP_LPSPI2_SOUT **TPM**: AONMIX_TOP_TPM1_CH2 **SAI**: AONMIX_TOP_SAI1_MCLK **GPIO**: AONMIX_TOP_GPIO1_IO_BIT6	DI	1.8V	
P142	GND	NA	-	NA	
P143	CAN0_TX	**PDM**: AONMIX_TOP_PDM_CLK **MQS**: AONMIX_TOP_MQS1_LEFT **LPTMR**: AONMIX_TOP_LPTMR1_ALT1 **GPIO**: AONMIX_TOP_GPIO1_IO_BIT8 **CAN**: AONMIX_TOP_CAN1_TX	DO	1.8V	
P144	CAN0_RX	**PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT0 **MQS**: AONMIX_TOP_MQS1_RIGHT **SPI**: AONMIX_TOP_LPSPI1_PCS1 **TPM**: AONMIX_TOP_TPM1_EXTCLK **LPTMR**: AONMIX_TOP_LPTMR1_ALT2 **GPIO**: AONMIX_TOP_GPIO1_IO_BIT9 **CAN**: AONMIX_TOP_CAN1_RX	DI	1.8V	
P145	CAN1_TX	**GPIO**: GPIO2_IO_BIT25 **USDHC**: USDHC3_DATA1 **CAN**: CAN2_TX **TPM**: TPM4_CH3 **JTAG**: JTAG_MUX_TCK **SPI**: LPSPI7_PCS1 **FLEXIO**: FLEXIO1_FLEXIO_BIT25	DO	1.8V	
P146	CAN1_RX	**GPIO**: GPIO2_IO_BIT27 **USDHC**: USDHC3_DATA3 **CAN**: CAN2_RX **TPM**: TPM6_CH3 **JTAG**: JTAG_MUX_TMS **SPI**: LPSPI5_PCS1 **FLEXIO**: FLEXIO1_FLEXIO_BIT27	DI	1.8V	
P147	VDD_IN	VSYS	A	3.0 - 5.25V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P148	VDD_IN	VSYS	A	3.0 - 5.25V	
P149	VDD_IN	VSYS	A	3.0 - 5.25V	
P150	VDD_IN	VSYS	A	3.0 - 5.25V	
P151	VDD_IN	VSYS	A	3.0 - 5.25V	
P152	VDD_IN	VSYS	A	3.0 - 5.25V	
P153	VDD_IN	VSYS	A	3.0 - 5.25V	
P154	VDD_IN	VSYS	A	3.0 - 5.25V	
P155	VDD_IN	VSYS	A	3.0 - 5.25V	
P156	VDD_IN	VSYS	A	3.0 - 5.25V	
S1	CSI1_TX+ / I2C_CAM1_CK	SC1	DI/O	1.8V	From PCA9546APW (U23)
S2	CSI1_TX- / I2C_CAM1_DAT	SD1	DI/O	1.8V	From PCA9546APW (U23)
S3	GND	NA	-	NA	
S4	RSVD	ADC_IN2	DI	1.8V	
S5	I2C_CAM0_CK / CSI0_TX-	SC0	DO	1.8V	From PCA9546APW (U23)
S6	CAM_MCK	**CCM:** CCMSRCGPCMIX_TOP_CLKO_1 **NET:** NETCMIX_TOP_NETC_TMR_1588_TRIG1 **FLEXIO:** FLEXIO1_FLEXIO_BIT26 **GPIO:** GPIO3_IO_BIT26	DO	1.8V	
S7	I2C_CAM0_DAT / CSI0_TX+	SD0	DI/O	1.8V	From PCA9546APW (U23)
S8	CSI0_CK+	MIPI_CSI1_CLK_P	DO	1.8V	
S9	CSI0_CK-	MIPI_CSI1_CLK_N	DO	1.8V	
S10	GND	NA	-	NA	
S11	CSI0_RX0+	MIPI_CSI1_D0_P	DI	1.8V	
S12	CSI0_RX0-	MIPI_CSI1_D0_N	DI	1.8V	
S13	GND	NA	-	NA	
S14	CSI0_RX1+	MIPI_CSI1_D1_P	DI	1.8V	
S15	CSI0_RX1-	MIPI_CSI1_D1_N	DI	1.8V	
S16	GND	NA	-	NA	
S17	GBE1_MDI0+	TD_P_A	DI/O	1.8V	From DP83867IRRGZ (U17)
S18	GBE1_MDI0-	TD_M_A	DI/O	1.8V	From DP83867IRRGZ (U17)
S19	GBE1_LINK100#	LED_0	DO	3.3V	From DP83867IRRGZ (U17)
S20	GBE1_MDI1+	TD_P_B	DI/O	1.8V	From DP83867IRRGZ (U17)
S21	GBE1_MDI1-	TD_M_B	DI/O	1.8V	From DP83867IRRGZ (U17)
S22	GBE1_LINK1000#	LED_1	DO	3.3V	From DP83867IRRGZ (U17)
S23	GBE1_MDI2+	TD_P_C	DI/O	1.8V	From DP83867IRRGZ (U17)

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S24	GBE1_MDI2-	TD_M_C	DI/O	1.8V	From DP83867IRRGZ (U17)
S25	GND	NA	-	NA	
S26	GBE1_MDI3+	TD_P_D	DI/O	1.8V	From DP83867IRRGZ (U17)
S27	GBE1_MDI3-	TD_M_D	DI/O	1.8V	From DP83867IRRGZ (U17)
S28	GBE1_CTREF	NA	-	NA	
S29	PCIE_D_TX+ / SERDES_0_TX+	NA	-	NA	
S30	PCIE_D_TX- / SERDES_0_TX-	NA	-	NA	
S31	GBE1_LINK_ACT#	LED_2	DO	3.3V	From DP83867IRRGZ (U17)
S32	PCIE_D_RX+ / SERDES_0_RX+	NA	-	NA	
S33	PCIE_D_RX- / SERDES_0_RX-	NA	-	NA	
S34	GND	NA	-	NA	
S35	USB4+	USB2DN_DP4/PRT_DIS_P4	DI	3.3V	From USB5744T/2GX01 (U9)
S36	USB4-	USB2DN_DM4/PRT_DIS_M4	DI	3.3V	From USB5744T/2GX01 (U9)
S37	USB3_VBUS_DET	NA	-	NA	
S38	AUDIO_MCK	**GPIO**: GPIO2_IO_BIT17 **SAI**: SAI3_MCLK **UART**: LPUART3_RTS_B **SPI**: LPSPI4_PCS1 **UART**: LPUART4_RTS_B **FLEXIO**: FLEXIO1_FLEXIO_BIT17	DO	1.8V	
S39	I2S0_LRCK	**GPIO**: GPIO2_IO_BIT26 **USDH**: USDHC3_DATA2 **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT1 **FLEXIO:** FLEXIO1_FLEXIO_BIT26 **TPM**: TPM5_CH3 **JTAG**: JTAG_MUX_TDI **SPI**: LPSPI8_PCS1 **SAI**: SAI3_TX_SYNC	DI/O	1.8V	
S40	I2S0_SDOUT	**GPIO**: GPIO2_IO_BIT21 **SAI**: SAI3_TX_DATA_BIT0 **PDM**: AONMIX_TOP_PDM_CLK **FLEXIO**: FLEXIO1_FLEXIO_BIT21 **SPI**: LPSPI5_SCK **SPI**: LPSPI4_SCK **TPM**: TPM4_CH1 **SAI**: SAI3_RX_BCLK	DO	1.8V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S41	I2S0_SDIN	**GPIO**: GPIO2_IO_BIT20 **SAI**: SAI3_RX_DATA_BIT0 **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT0 **SPI**: LPSPI5_SOUT **SPI**: LPSPI4_SOUT **TPM**: TPM3_CH1 **FLEXIO**: FLEXIO1_FLEXIO_BIT20	DI	1.8V	
S42	I2S0_CK	**GPIO**: GPIO2_IO_BIT16 **SAI**: SAI3_TX_BCLK **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT2 **UART**: LPUART3_CTS_B **SPI**: LPSPI4_PCS2 **UART**: LPUART4_CTS_B **FLEXIO**: FLEXIO1_FLEXIO_BIT16	DI/O	1.8V	
S43	ESPI_ALERT0#	NA	-	NA	
S44	ESPI_ALERT1#	NA	-	NA	
S45	MDIO_CLK	**NET:** NETCMIX_TOP_NETC_MDC **UART**: LPUART3_DCD_B **I3C**: I3C2_SCL **HSIO**: HSIOMIX_TOP_USB1_OTG_ID **FLEXIO**: FLEXIO2_FLEXIO_BIT0 **GPIO:** GPIO4_IO_BIT0	DI/O		
S46	MDIO_DAT	**NET:** NETCMIX_TOP_NETC_MDIO **UART**: LPUART3_RIN_B **I3C**: I3C2_SDA **HSIO**: HSIOMIX_TOP_USB1_OTG_PWR **FLEXIO**: FLEXIO2_FLEXIO_BIT1 **GPIO:** GPIO4_IO_BIT1	DI/O		
S47	GND	NA	-	NA	
S48	I2C_GP_CK	SC2	DO	1.8V	From PCA9546APW (U23)
S49	I2C_GP_DAT	SD2	DI/O	1.8V	From PCA9546APW (U23)
S50	I2S2_LRCK / HDA_SYNC	NA	DI/O	1.8V	
S51	I2S2_SDOUT / HDA_SDO	NA	DO	1.8V	
S52	I2S2_SDIN / HDA_SDI	NA	DI	1.8V	
S53	I2S2_CK / HDA_CK	NA	DI/O	1.8V	
S54	SATA_ACT#	NA	-	NA	
S55	USB5_EN_OC-	NA	-	NA	
S56	ESPI_IO_2 / QSPI_IO_2	NA	DI/O	1.8V	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S57	ESPI_IO_3 / QSPI_IO_3	NA	-	NA	
S58	ESPI_RESET#	NA	-	NA	
S59	USB5+	NA	-	NA	
S60	USB5-	NA	-	NA	
S61	GND	NA	-	NA	
S62	USB3_SSTX+	USB3DN_TXDP1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S63	USB3_SSTX-	USB3DN_TXDM1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S64	GND	NA	-	NA	
S65	USBSSRX+	USB3DN_RXDP1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S66	USBSSRX-	USB3DN_RXDM1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S67	GND	NA	-	NA	
S68	USB3+	USB2DN_DP1/PRT_DIS_P1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S69	USB3-	USB2DN_DM1/PRT_DIS_M1	DI/O	3.3V	From USB5744T/2GX01 (U9)
S70	GND	NA	-	NA	
S71	USB2_SSTX+	USB3DN_TXDP3	DI/O	3.3V	From USB5744T/2GX01 (U9)
S72	USB2_SSTX-	USB3DN_TXDM3	DI/O	3.3V	From USB5744T/2GX01 (U9)
S73	GND	NA	-	NA	
S74	USB2_SSRX+	USB3DN_RXDP3	DI/O	3.3V	From USB5744T/2GX01 (U9)
S75	USB2_SSRX-	USB3DN_RXDM3	DI/O	3.3V	From USB5744T/2GX01 (U9)
S76	PCIE_B_RST#	P1_6	DI	1.8V	From PCAL6524EVJ (U21)
S77	PCIE_C_RST#	P2_2	DI	1.8V	From PCAL6524EVJ (U21)
S78	PCIE_C_RX+ / SERDES_1_RX+	ETH_RX0_P	DI/O	0.8V	
S79	PCIE_C_RX- / SERDES_1_RX-	ETH_RX0_N	DI/O	0.8V	
S80	GND	NA	-	NA	
S81	PCIE_C_TX+ / SERDES_1_TX+	ETH_TX0_P	DI/O	0.8V	
S82	PCIE_C_TX- / SERDES_1_TX-	ETH_TX0_N	DI/O	0.8V	
S83	GND	NA	-	NA	
S84	PCIE_B_REFCK+	CLK1_P	DI/O	1.8V	From DSC557-0344FL1T (U22)
S85	PCIE_B_REFCK-	CLK1_N	DI/O	1.8V	From DSC557-0344FL1T (U22)
S86	GND	NA	-	NA	
S87	PCIE_B_RX+	PCIE2_RX0_P	DI/O	1.8V	
S88	PCIE_B_RX-	PCIE2_RX0_N	DI/O	1.8V	
S89	GND	NA	-	NA	

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S90	PCIE_B_TX+	PCIE2_TX0_P	DI/O	1.8V	
S91	PCIE_B_TX-	PCIE2_TX0_N	DI/O	1.8V	
S92	GND	NA	-	NA	
S93	DP0_LANE0+	NA	-	NA	
S94	DP0_LANE0-	NA	-	NA	
S95	DP0_AUX_SEL	NA	-	NA	
S96	DP0_LANE1+	NA	-	NA	
S97	DP0_LANE1-	NA	-	NA	
S98	DP0_HPD	NA	-	NA	
S99	DP0_LANE2+	NA	-	NA	
S100	DP0_LANE2-	NA	-	NA	
S101	GND	NA	-	NA	
S102	DP0_LANE3+	NA	-	NA	
S103	DP0_LANE3-	NA	-	NA	
S104	USB3_OTG_ID	NA	-	NA	
S105	DP0_AUX+	NA	-	NA	
S106	DP0_AUX-	NA	-	NA	
S107	LCD1_BKLT_EN	**SPI**: FLEXSPI1_A_DATA_BIT4 **SAI**: SAI5_TX_DATA_BIT0 **SAI**: SAI5_RX_DATA_BIT1 **SPI**: XSPI_DATA_BIT4 **GPIO**: GPIO5_IO_BIT4	DI/O	1.8V	
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	DO	1.8V	
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	DO	1.8V	
S110	GND	NA	-	NA	
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P	DO	1.8V	
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N	DO	1.8V	
S113	eDP1_HPD / DSI1_TE	NA	-	NA	
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P	DO	1.8V	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N	DO	1.8V	
S116	LCD1_VDD_EN	P0_3	DI/O	1.8V	

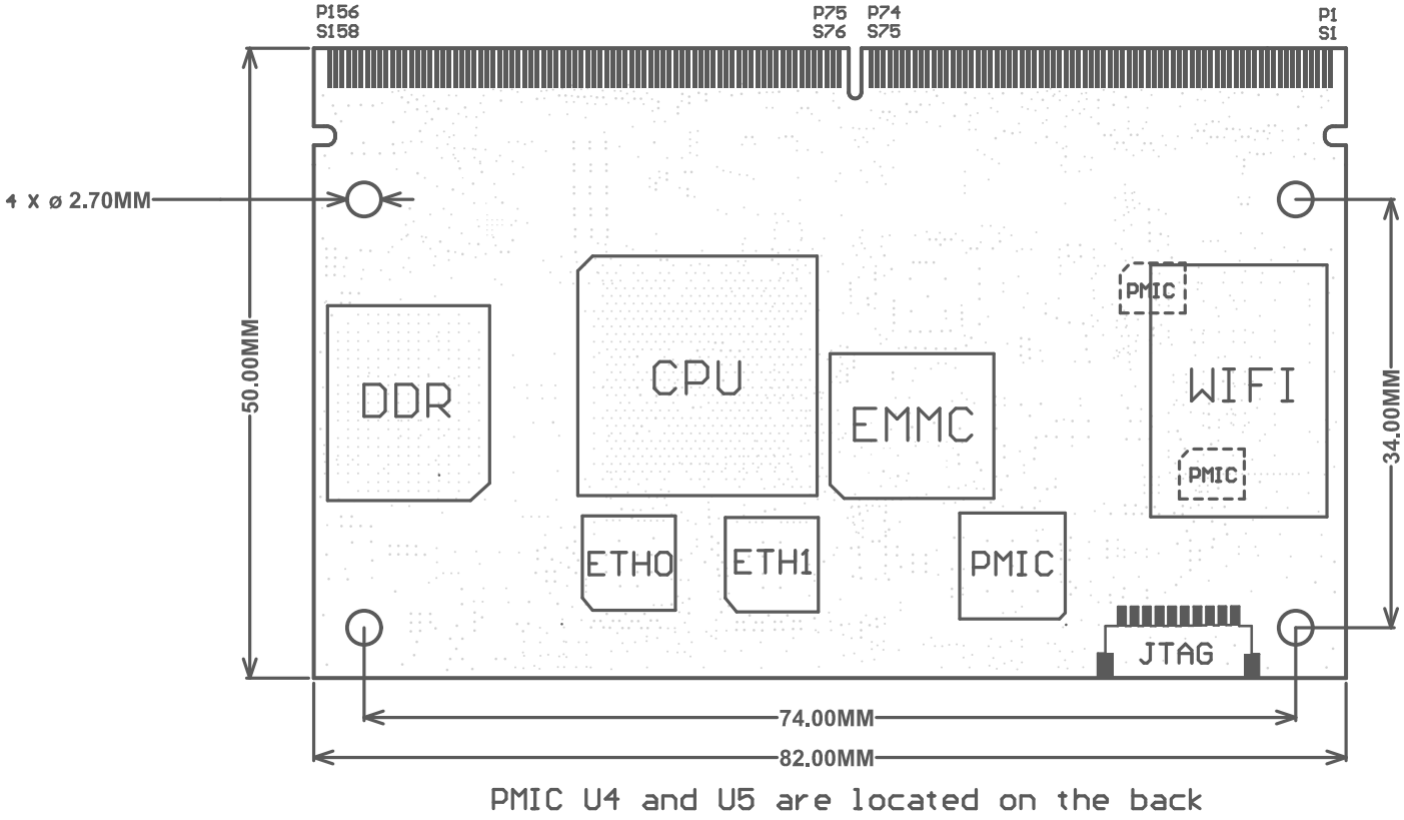
SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P	DO	1.8V	
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N	DO	1.8V	
S119	GND	NA	-	NA	
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P	DO	1.8V	
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N	DO	1.8V	
S122	LCD1_BKLT_PWM	**GPIO**: GPIO2_IO_BIT12 **TPM**: TPM3_CH2 **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT2 **FLEXIO**: FLEXIO1_FLEXIO_BIT12 **SPI**: LPSPI8_PCS0 **UART**: LPUART8_TX **I2C**: LPI2C8_SDA **SAI**: SAI3_RX_SYNC	DO	1.8V	
S123	GPIO13	**NETC**: NETCMIX_TOP_NETC_MDIO **UART**: LPUART4_RIN_B **SAI**: NETCMIX_TOP_SAI2_RX_BCLK **FLEXIO**: FLEXIO2_FLEXIO_BIT15 **GPIO**: GPIO4_IO_BIT15	DI/O	1.8V	
S124	GND	NA	-	NA	
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSICSI1_D0_P	DO	1.8V	For LVDS, populate R195 and depopulate R189
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSICSI1_D0_N	DO	1.8V	For LVDS, populate R196 and depopulate R190
S127	LCD0_BKLT_EN	P2_4	DO	1.8V	From PCAL6524EVJ (U21)
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	MIPI_DSICSI1_D1_P	DO	1.8V	For LVDS, populate R197 and depopulate R191
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	MIPI_DSICSI1_D1_N	DO	1.8V	For LVDS, populate R198 and depopulate R192
S130	GND	NA	-	NA	
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSICSI1_D2_P	DO	1.8V	For LVDS, populate R199 and depopulate R193

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	MIPI_DSICSI1_D2_N	DO	1.8V	For LVDS, populate R200 and depopulate R194
S133	LCD0_VDD_EN	P0_1	DO	1.8V	From PCAL6524EVJ (U21)
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	MIPI_DSICSI1_CLK_P	DO	1.8V	For LVDS, populate R201 and depopulate R203
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	MIPI_DSICSI1_CLK_N	DO	1.8V	For LVDS, populate R202 and depopulate R204
S136	GND	NA	-	NA	
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	MIPI_DSICSI1_D3_P	DO	1.8V	For LVDS, populate R205 and depopulate R207
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	MIPI_DSICSI1_D3_N	DO	1.8V	For LVDS, populate R206 and depopulate R208
S139	I2C_LCD_CK	I2C2_SCL	DI/O	1.8V	
S140	I2C_LCD_DAT	I2C2_SDA	DI/O	1.8V	
S141	LCD0_BKLT_PWM	**GPIO**: GPIO2_IO_BIT13 **TPM:** TPM4_CH2 **PDM**: AONMIX_TOP_PDM_BIT_STREAM_BIT3 **SPI**: LPSPI8_SIN **UART**: LPUART8_RX **I2C**: LPI2C8_SCL **FLEXIO**: FLEXIO1_FLEXIO_BIT13	DI/O	1.8V	
S142	GPIO12	**NETC**: NETCMIX_TOP_NETC_MDC **UART**: LPUART4_DCD_B **SAI**: NETCMIX_TOP_SAI2_RX_SYNC **FLEXIO**: FLEXIO2_FLEXIO_BIT14 **GPIO**: GPIO4_IO_BIT14	DI/O	1.8V	
S143	GND	NA	-	NA	
S144	eDP0_HPD / DSI0_TE	NA	-	NA	
S145	WDT_TIME_OUT#	WDOG_ANY	DO	1.8V	
S146	PCIE_WAKE#	P1_7	DO	1.8V	
S147	VDD_RTC	NVCC_BBSM	A	2.0 - 3.25V	
S148	LID#	TAMPER0	DI	1.8 - 5V	
S149	SLEEP#	P0_5	DI	1.8 - 5V	From PCAL6524EVJ (U21)
S150	VIN_PWR_BAD#	PWRON	DI	1.8V	
S151	CHARGING#	P0_6	DI	1.8 - 5V	From PCAL6524EVJ (U21)
S152	CHARGER_PRSNT#	P0_7	DI	1.8 - 5V	From PCAL6524EVJ (U21)
S153	CARRIER_STBY#	P1_0	DO	1.8V	From PCAL6524EVJ (U21)
S154	CARRIER_PWR_ON	P1_1	DO	1.8V	From PCAL6524EVJ (U21)

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S155	FORCE_RECOV#	BOOT_MODE0	DI	1.8V	
S156	BATLOW#	P1_2	DI	1.8 - 5V	From PCAL6524EVJ (U21)
S157	TEST#	P2_7	DI	1.8 - 5V	From PCAL6524EVJ (U21)
S158	GND	NA	-	NA	

9 Mechanical and PCB footprint specification

Module dimensions of the Nitrogen95 SMARC are 82 x 50 mm. Detail drawings are shown below.



10 Storage instructions

Required Storage Conditions:

- **Prior to Opening the Dry Packing**
  The following are required storage conditions prior to opening the dry packing:
  - Normal temperature: 5~40℃
  - Normal humidity: 80% (Relative humidity) or less
  - Storage period: One year or less

11 Ordering Information

Order Model	Description
EZSMC-955-0416-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / 0 to +70°C / Without Wireless
EZSMI-955-0416-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / -40 to +85°C / Without Wireless
EZSMC-955-0816-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / 0 to +70°C / Without Wireless
EZSMI-955-0816-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / -40 to +85°C / Without Wireless
EZSMC-955-1616-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 16GB / 16GB eMMC / 0 to +70°C / Without Wireless
EZSMI-955-1616-00000-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 16GB / 16GB eMMC / -40 to +85°C / Without Wireless
EZSMC-955-0416-00117-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / IF573 3MHF / 0 to +70°C
EZSMC-955-0816-00117-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / IF573 3MHF / 0 to +70°C
EZSMI-955-0416-00117-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / IF573 3MHF / -40 to +85°C
EZSMI-955-0816-00117-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / IF573 3MHF / -40 to +85°C
EZSMC-955-0416-00158-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / NX611 1MHF / 0 to +70°C
EZSMC-955-0816-00158-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / NX611 1MHF / 0 to +70°C
EZSMI-955-0416-00158-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / NX611 1MHF / -40 to +85°C
EZSMI-955-0816-00158-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / NX611 1MHF / -40 to +85°C
EZSMC-955-0416-00184-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / IF513 1MHF / 0 to +70°C
EZSMC-955-0816-00184-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / IF513 1MHF / 0 to +70°C
EZSMI-955-0416-00184-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / IF513 1MHF / -40 to +85°C
EZSMI-955-0816-00184-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / IF513 1MHF / -40 to +85°C
EZSMC-955-0416-00199-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / TI351 1MHF / 0 to +70°C
EZSMC-955-0816-00199-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / TI351 1MHF / 0 to +70°C
EZSMI-955-0416-00199-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 4GB / 16GB eMMC / TI351 1MHF / -40 to +85°C
EZSMI-955-0816-00199-2	Nitrogen95 SMARC SOM: i.MX 955 6x / 8GB / 16GB eMMC / TI351 1MHF / -40 to +85°C
EZSMC-959-0816-00117-2	Nitrogen95 SMARC SOM: Beta / i.MX 959 6x / 8GB / 16GB eMMC / IF573 3MHF / 0 to +70°C
EZSMC-959-0816-00158-2	Nitrogen95 SMARC SOM: Beta / i.MX 959 6x / 8GB / 16GB eMMC / NX611 1MHF / 0 to +70°C
EZSMC-959-0816-00158-2-K2	Nitrogen95 SMARC Evaluation Kit: Beta / 7 in Display / SMARC Carrier Board / i.MX 959 / 8GB / 16GB eMMC / NX611 1MHF / Accessories
EZSMC-959-0816-00158-2-KC	Nitrogen95 SMARC Evaluation Kit: Beta / 7 in Display / 8.3MP Camera / SMARC Carrier Board / i.MX 959 / 8GB / 16GB eMMC / NX611 1MHF / Accessories
EZSMC-955-0816-00158-2-K2	Nitrogen95 SMARC Evaluation Kit: 7 in Display / SMARC Carrier Board / i.MX 955 / 8GB / 16GB eMMC / NX611 1MHF / Accessories
EZSMC-955-0816-00158-2-KC	Nitrogen95 SMARC Evaluation Kit: 7 in Display / 8.3MP Camera / SMARC Carrier Board / i.MX 955 / 8GB / 16GB eMMC / NX611 1MHF / Accessories
450-00218	Heatsink for Nitrogen Nitrogen95 SMARC family
SMARC_CAR	Kit - Universal SMARC Carrier Board. Includes 3x EFB2471A3S-10MH4L and 2x 001-0021 antennas, power supply, DB9 cable
SMARC_CAR_BRD	Universal Carrier Board - SMARC (Note - SOM sold separately)

12 Regulatory

Radio certifications for SOMs with wireless options are held under the specific wireless module listings:

Order Model with Wireless	Module Product Page	RIG
EZSMC-955-0416-00117-2	Sona IF573	Sona IF573 Regulatory Information
EZSMC-955-0816-00117-2	Sona IF573	Sona IF573 Regulatory Information
EZSMI-955-0416-00117-2	Sona IF573	Sona IF573 Regulatory Information
EZSMI-955-0816-00117-2	Sona IF573	Sona IF573 Regulatory Information
EZSMC-955-0416-00158-2	Sona NX611	Sona NX611 Regulatory information
EZSMC-955-0816-00158-2	Sona NX611	Sona NX611 Regulatory information
EZSMI-955-0416-00158-2	Sona NX611	Sona NX611 Regulatory information
EZSMI-955-0816-00158-2	Sona NX611	Sona NX611 Regulatory information
EZSMC-955-0416-00184-2	Sona IF513	Sona IF513 Regulatory Information
EZSMC-955-0816-00184-2	Sona IF513	Sona IF513 Regulatory Information
EZSMI-955-0416-00184-2	Sona IF513	Sona IF513 Regulatory Information
EZSMI-955-0816-00184-2	Sona IF513	Sona IF513 Regulatory Information
EZSMC-955-0416-00199-2	Sona TI351	Sona TI351 Regulatory Information
EZSMC-955-0816-00199-2	Sona TI351	Sona TI351 Regulatory Information
EZSMI-955-0416-00199-2	Sona TI351	Sona TI351 Regulatory Information
EZSMI-955-0816-00199-2	Sona TI351	Sona TI351 Regulatory Information

13 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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