FAIRCHILD SEMICONDUCTOR®

March 2012

FDD390N15ALZ

N-Channel PowerTrench® MOSFET

150V, 26A, 42mΩ

Features

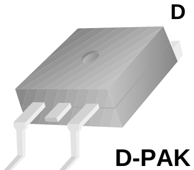
- $R_{DS(on)}$ = 33.4mΩ (Typ.) @ V_{GS} = 10V, I_D = 26A
- $R_{DS(on)}$ = 42.2mΩ (Typ.) @ V_{GS} = 4.5V, I_D = 20A
- Fast Switching Speed
- Low gate charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

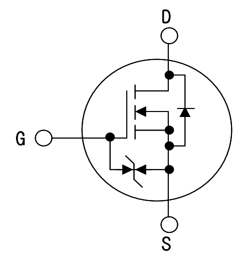
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		Rating	Units
V_{DSS}	Drain to Source Voltage		150	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)	26	A
		- Continuous (T_C = 100°C)	17	
I_{DM}	Drain Current	- Pulsed (Note 1)	104	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		96	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		13	V/ns
P_D	Power Dissipation	(T_C = 25°C)	63	W
		- Derate above 25°C	0.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Min.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	87	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD390N15ALZ	FDD390N15ALZ	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$	150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.15	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 120V$, $T_C = 125^oC$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 26A$	-	33.4	42	$m\Omega$
		$V_{GS} = 4.5V$, $I_D = 20A$	-	42.2	64	$m\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 26A$	-	50	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	$V_{DS} = 75V$, $V_{GS} = 0V$ f = 1MHz	-	1323	1760	pF
C_{oss}	Output Capacitance		-	93	120	pF
C_{rss}	Reverse Transfer Capacitance		-	4	6	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75V$, $V_{GS} = 0V$	-	165	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10V$; $V_{DS} = 75V$, $I_D = 26A$ (Note 4)	-	17.6	39	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	$V_{GS} = 4.5V$	-	8.1	10.5	nC
Q_{gs}	Gate to Source Gate Charge		-	4.7	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	2.3	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain shorted to Source, f = 1MHz	-	1.48	-	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75V$, $I_D = 26A$ $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	12.8	35.6	ns
t_r	Turn-On Rise Time		-	9.3	28.6	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26.9	63.8	ns
t_f	Turn-Off Fall Time		-	3.2	16.4	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	26	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	104	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 26A$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 26A$ $dI_F/dt = 100A/\mu s$	-	70	-	ns
Q_{rr}	Reverse Recovery Charge		-	169	-	nC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3mH, $I_{AS} = 6.75A$, Starting $T_J = 25°C$
3. $I_{SD} \le 26A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

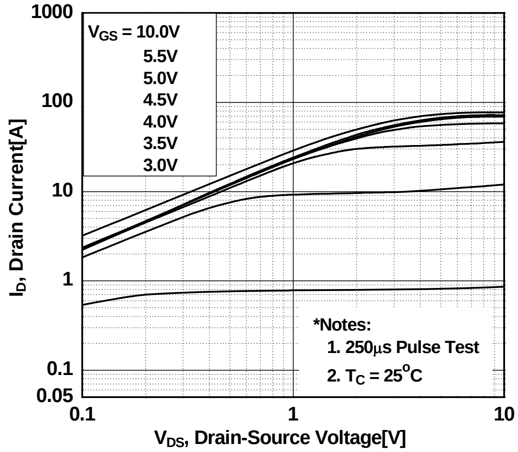


Figure 2. Transfer Characteristics

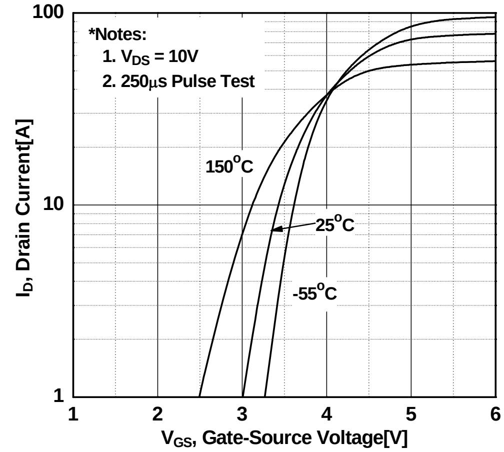


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

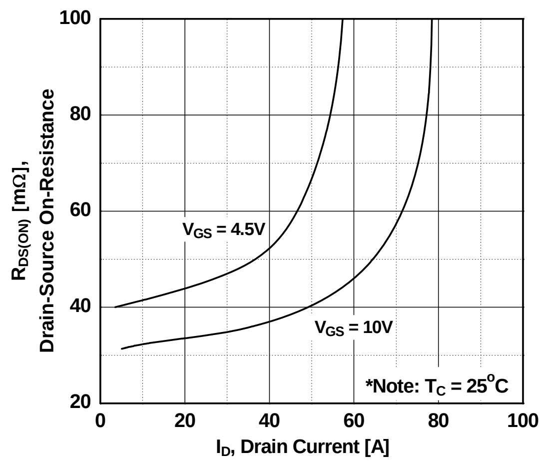


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

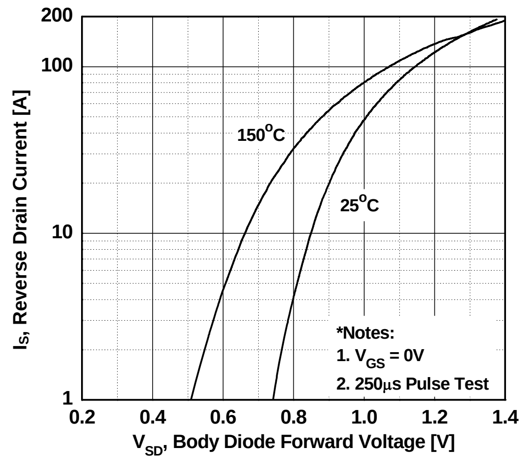


Figure 5. Capacitance Characteristics

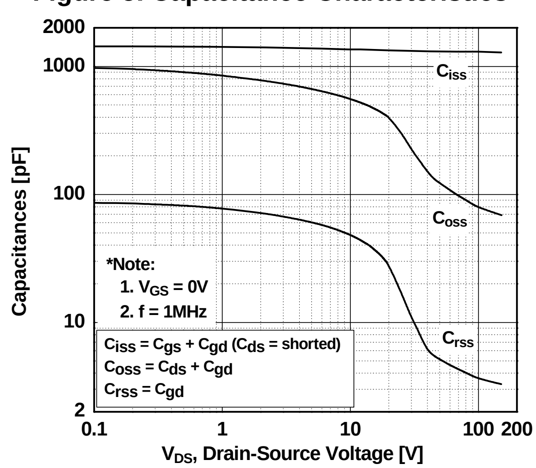
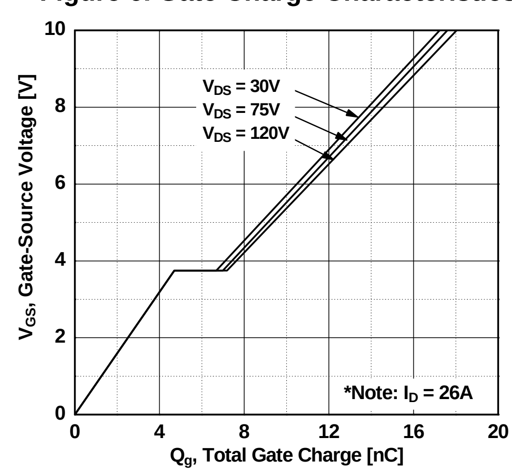


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

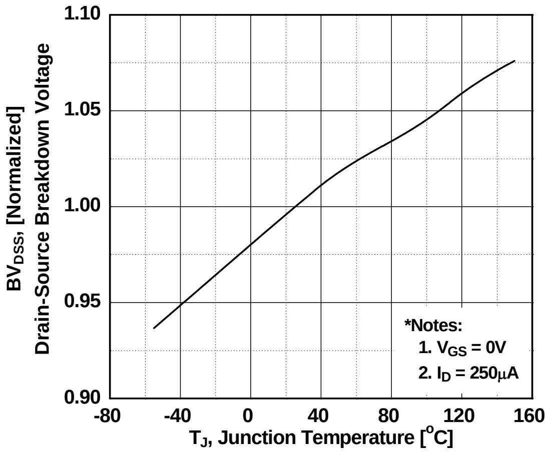


Figure 8. On-Resistance Variation vs. Temperature

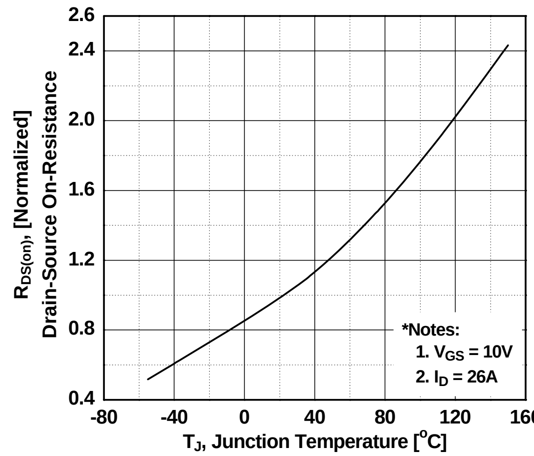


Figure 9. Maximum Safe Operating Area vs. Case Temperature

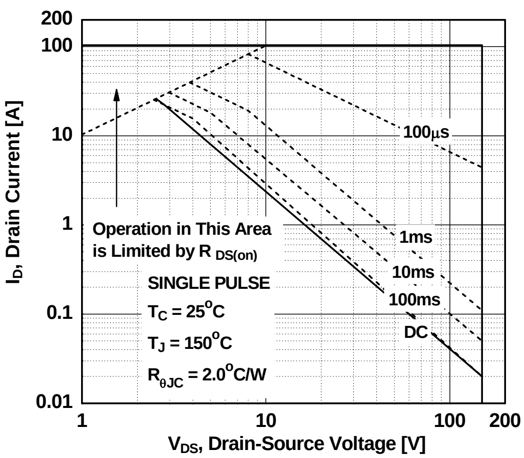


Figure 10. Maximum Drain Current

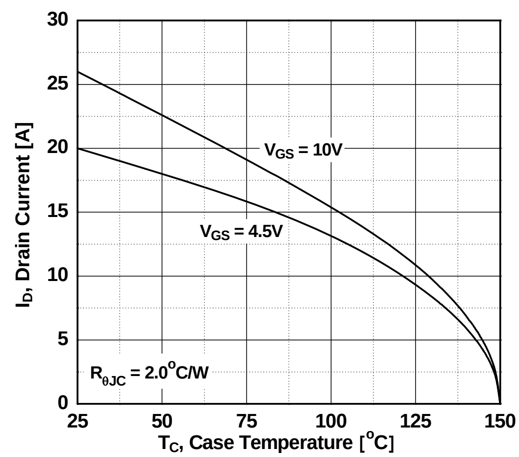


Figure 11. Eoss vs. Drain to Source Voltage

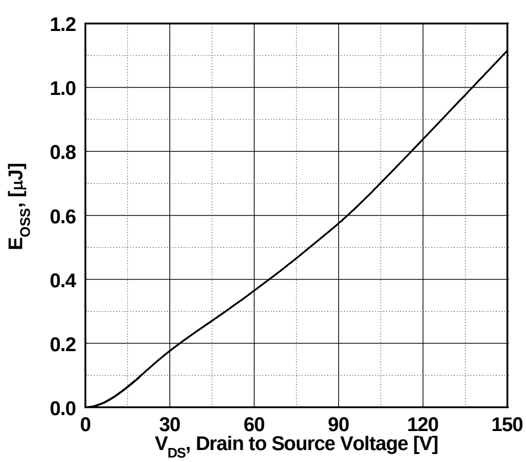
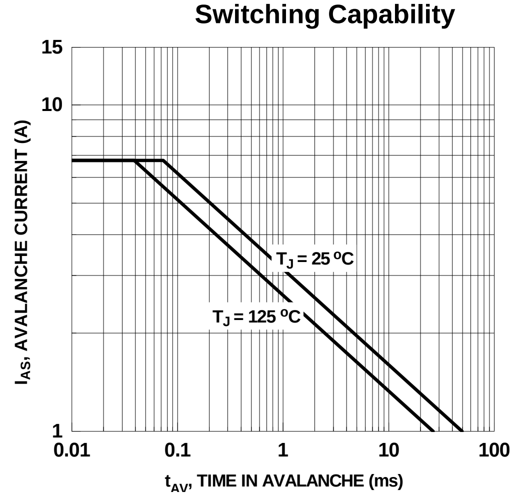
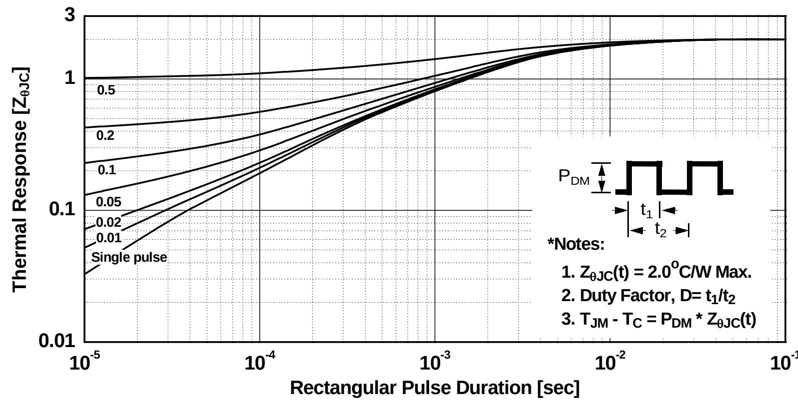


Figure 12. Unclamped Inductive Switching Capability

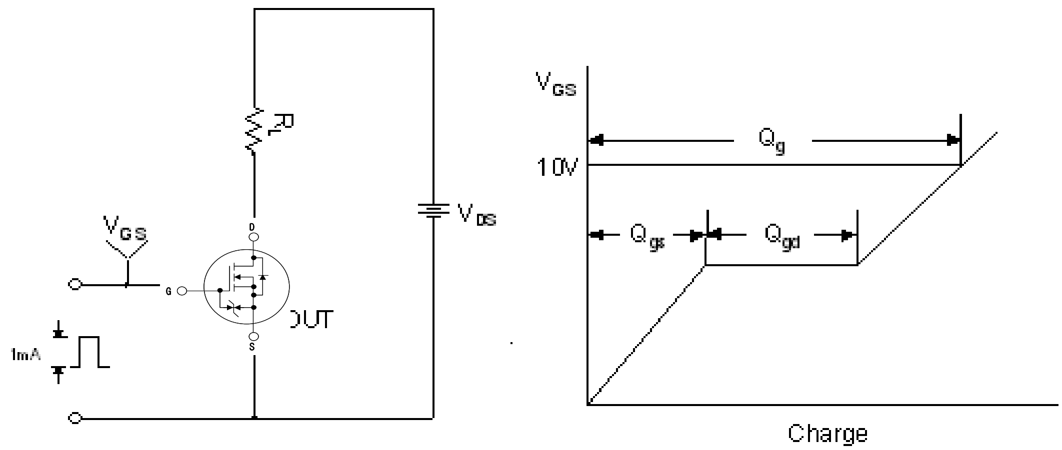


Typical Performance Characteristics (Continued)

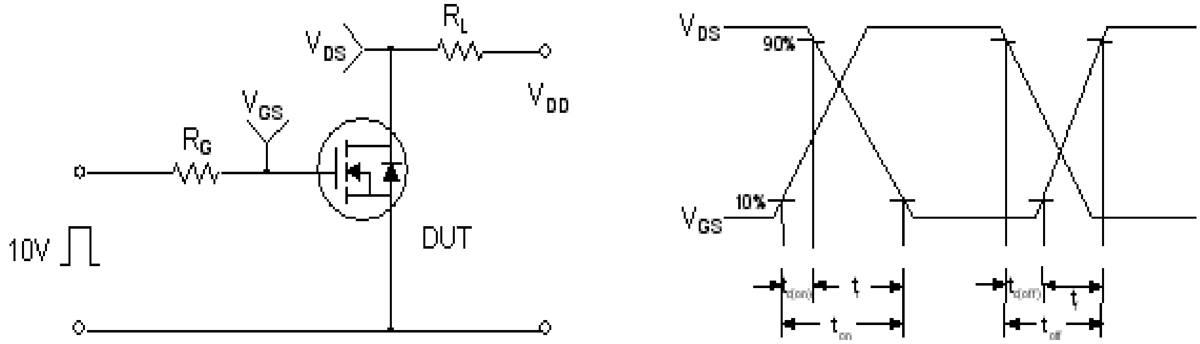
Figure 13. Transient Thermal Response Curve



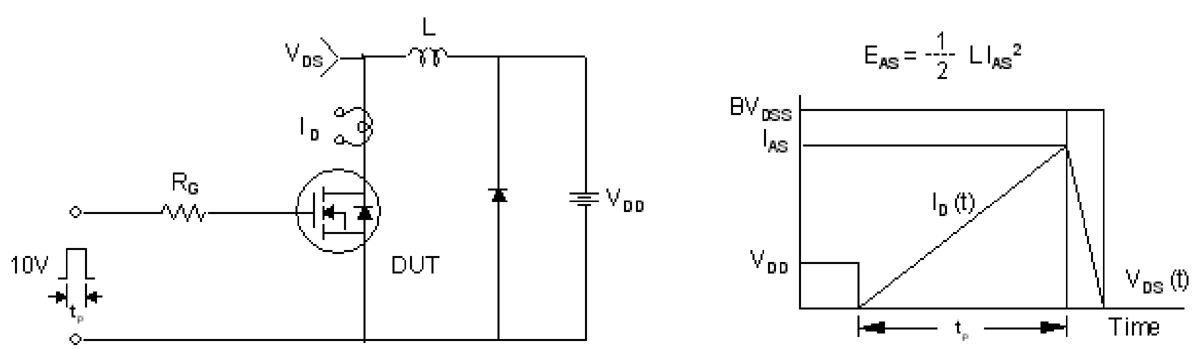
Gate Charge Test Circuit & Waveform



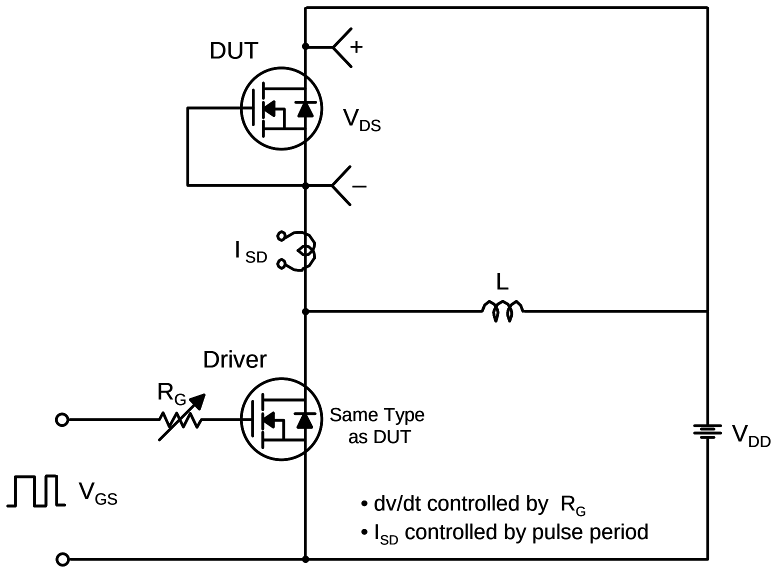
Resistive Switching Test Circuit & Waveforms

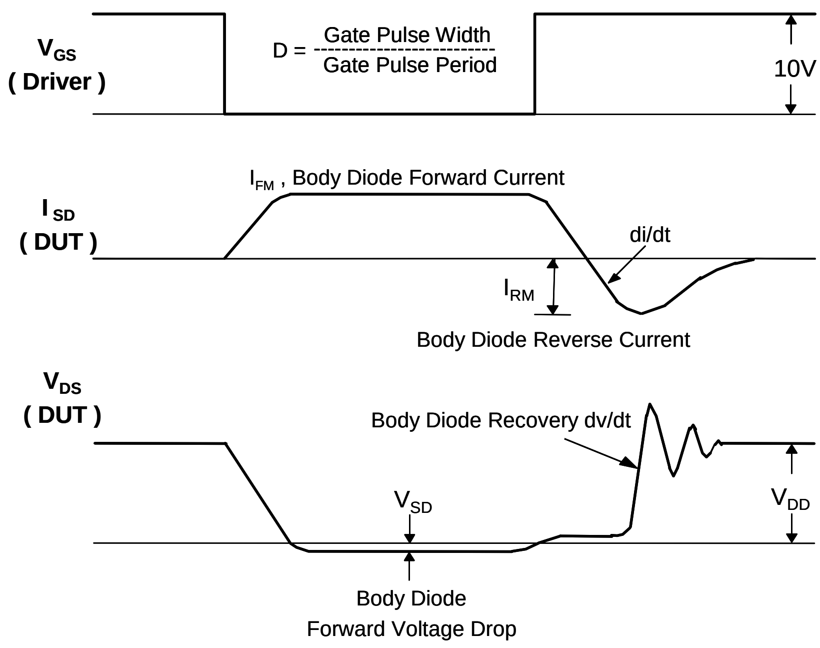


Unclamped Inductive Switching Test Circuit & Waveforms



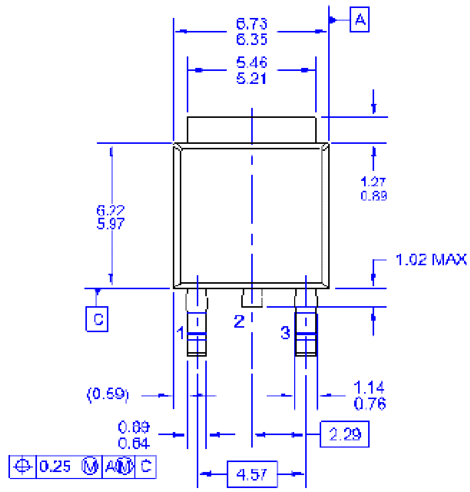
Peak Diode Recovery dv/dt Test Circuit & Waveforms

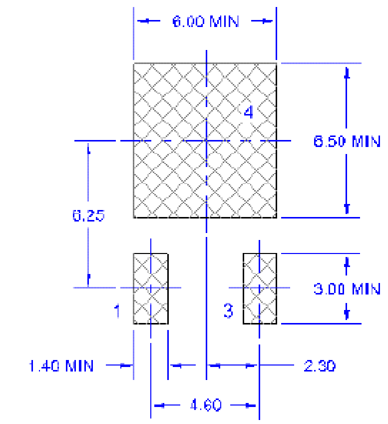




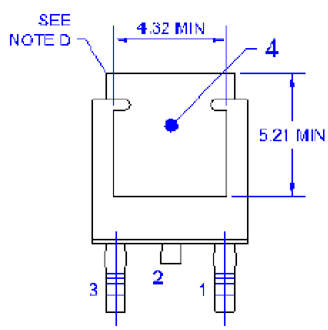
Mechanical Dimensions

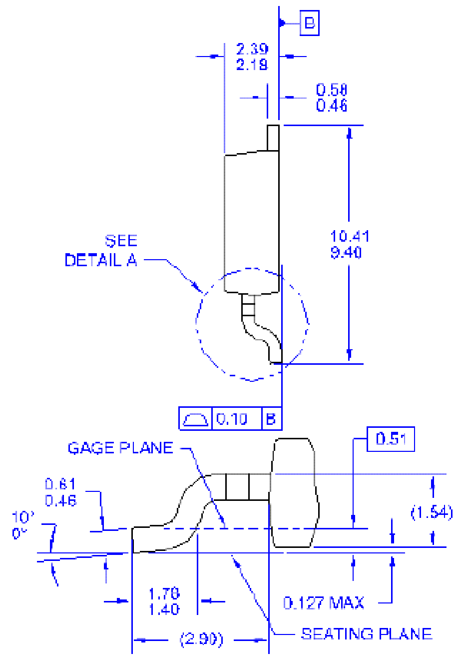
D-PAK





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P1003X238-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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