Approval Sheet

Customer	
Product Number	**M2UK-4GMJQC05-C**
Module speed	**PC2-6400**
Pin	**240 Pin**
CL	**5**
DRAM Operating Temp	**0°C ~ 85°C**
Date	**17th May 2016**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=3	CL=4	CL=5			
PC2-6400	400	533	800	15	15	60

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for 400MHz applications
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands.
- 15/10/2 Addressing (row/column/rank)-4GB
- Auto & self refresh 7.8μs (Tc ≤ +85°C)
- Golden Contact
- DRAM Operation Temperature
  - 0°C ≤ Tc ≤ +85°C
- Programmable Device Operation:
  - Burst Type: Sequential or Inteleave
  - Operation: Burst Read and Write
  - Device CAS# Latency: 3,4,5
  - Burst Length: 4, 8
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	3
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification..

3. Ordering Information

DDR2 UDIMM						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M2UK-4GMJQC05-C	4GB	PC2-6400	512Mx64	16	2	N

4. Pin Configurations (Front side/Back side)

–x64 UDIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	DQS#5	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	65	V_{SS}	185	CK0	95	DQ42	215	DQ47
6	DQS0#	126	NC	36	DQS3#	156	NC	66	V_{SS}	186	CK#0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	67	V_{DD}	187	V_{DD}	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	68	NC	188	A0	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	69	V_{DD}	189	V_{DD}	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	70	A10/AP	190	BA1	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	71	BA0	191	V_{DDQ}	101	SA2	221	CK2#
12	DQ8	132	DQ13	42	CB0	162	CB5	72	V_{DDQ}	192	RAS#	102	NC	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	73	WE#	193	S0#	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	DM8	74	CAS#	194	V_{DDQ}	104	DQS6#	224	NC
15	DQS1#	135	NC	45	DQS8#	165	NC	75	V_{DDQ}	195	ODT0	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	DQS8	166	V_{SS}	76	S1#	196	A13 [1]	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	CB6	77	ODT1	197	V_{DD}	107	DQ50	227	DQ55
18	NC	138	CK1#	48	CB2	168	CB7	78	V_{DDQ}	198	V_{SS}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	79	V_{SS}	199	DQ36	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	80	DQ32	200	DQ37	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	81	DQ33	201	V_{SS}	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	82	V_{SS}	202	DM4	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	83	DQS4#	203	NC	113	DQS7#	233	NC
24	DQ16	144	DQ21	54	BA2	174	NC	84	DQS4	204	V_{SS}	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	85	V_{SS}	205	DQ38	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	86	DQ34	206	DQ39	116	DQ58	236	DQ63
27	DQS2#	147	NC	57	A11	177	A9	87	DQ35	207	V_{SS}	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	88	V_{SS}	208	DQ44	118	V_{SS}	238	V_{DDSPD}
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	89	DQ40	209	DQ45	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	90	DQ41	210	V_{SS}	120	SCL	240	SA1

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.

5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 - CK2 CK0# - CK2#	SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power (1.8V)
S0# - S1#	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REF}	SDRAM I/O Reference supply
ODT0, ODT1	Active termination control lines	V_{SS}	Ground
DQ0 – DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0 – CB7	DIMM ECC check bit	NC	Spare Pin
DQS0 – DQS8 DQS0# - DQS8#	SDRAM data strobes	Reset	NOT use on UDIMM
DM0 – DM8	SDRAM data masks/high data strobe (x8 base x72 bit module use only)		

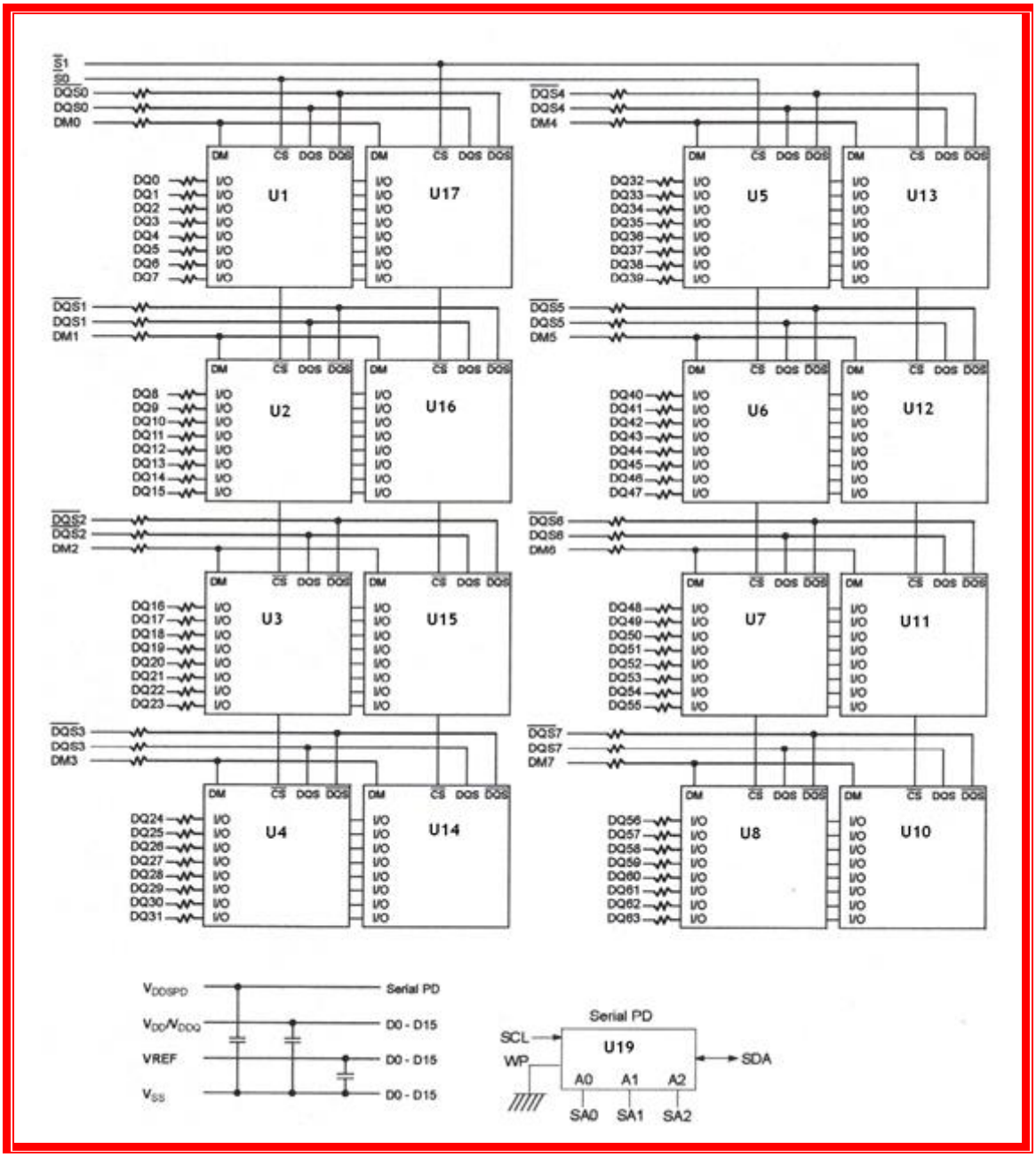
6. Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
CK0#, CK1#, CK2#	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CKE0#, CKE1#	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, RAS#, CAS#, WE# define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic

DQS0 – DQS8 DQS0# – DQS8#	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
SA0 – SA2	-	-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	-	-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL	-	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply.

7. Function Block Diagram:

- (2 Ranks, 256Mx8 DDR2 base SDRAM Module)



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter	Value	Units	Notes
VREF	Input Reference Voltage	0.5 * VDDQ	V	1
VSWING (MAX)	Input signal maximum peak to peak swing	1.7	V	1
SLEW	Input signal minimum slew rate	0	V	2,3
VIH (AC)	Input High (Logic1) Voltage	VREF + 0.125	V	
VIL (AC)	Input Low (Logic0) Voltage	-0.3	V	

Note::

1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.

- DC operating Conditions

Symbol	Parameter		Rating	Units	Note
T_{CASE}	Operating Temperature	Standard	0 to 85	°C	1,2

Note:

1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs All DRAM specification only support 0°C < t_{CASE} < 85°C

- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter	Min	Max	Units	Notes
VDD	Supply Voltage	1.7	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.9	V	1
VDDQ	I/O Supply Voltage	1.7	1.9	V	1
VREF	I/O Reference Voltage	0.49VDDQ	0.51VDDQ	V	1, 2
VTT	Termination Voltage	VREF-0.04	VREF+0.04	V	31
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ + 0.3	V	1
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	V	1

Note:

1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

9. Operating, Standby, and Refresh Currents

- 4GB UDIMM (2 Ranks, 256Mx8 DDR2 SDRAMs T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	1360	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	192	mA
I_{DD2N}	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	560	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	480	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	400	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	224	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	800	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	2080	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	2080	mA
I_{DD5}	Auto-Refresh Current: tRC = tRFC (MIN)	2720	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	192	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	4480	mA

10. AC Timing Specifications

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.40	+0.40	ns
tDQSCK	DQS output access time from CK/CK#	-0.35	+0.35	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL	-	tCK
tCK	Clock Cycle Time	2.5	8	ns
tDS	DQ and DM input setup time(differential data strobe)	0.05	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.125	-	ns
tIPW	Input pulse width	0.6	-	tCK
tDIPW	DQ and DM input pulse width (each input)	0.35	-	tCK
tHZ	Data-out high-impedance time from CK/XK	-	tACmax	ns
tLZ(DQS)	DQS low-impedance time from CK/XK	tACmin	tACmax	ns
tLZ(DQ)	DQ low-impedance time from CK/XK	$2t_{AC}$ min	t_{AC} max	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.20	ns
tQHS	Data hold Skew Factor	-	0.3	ns
tQH	Data output hold time from DQS	tHP - tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	-0.25	+0.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK

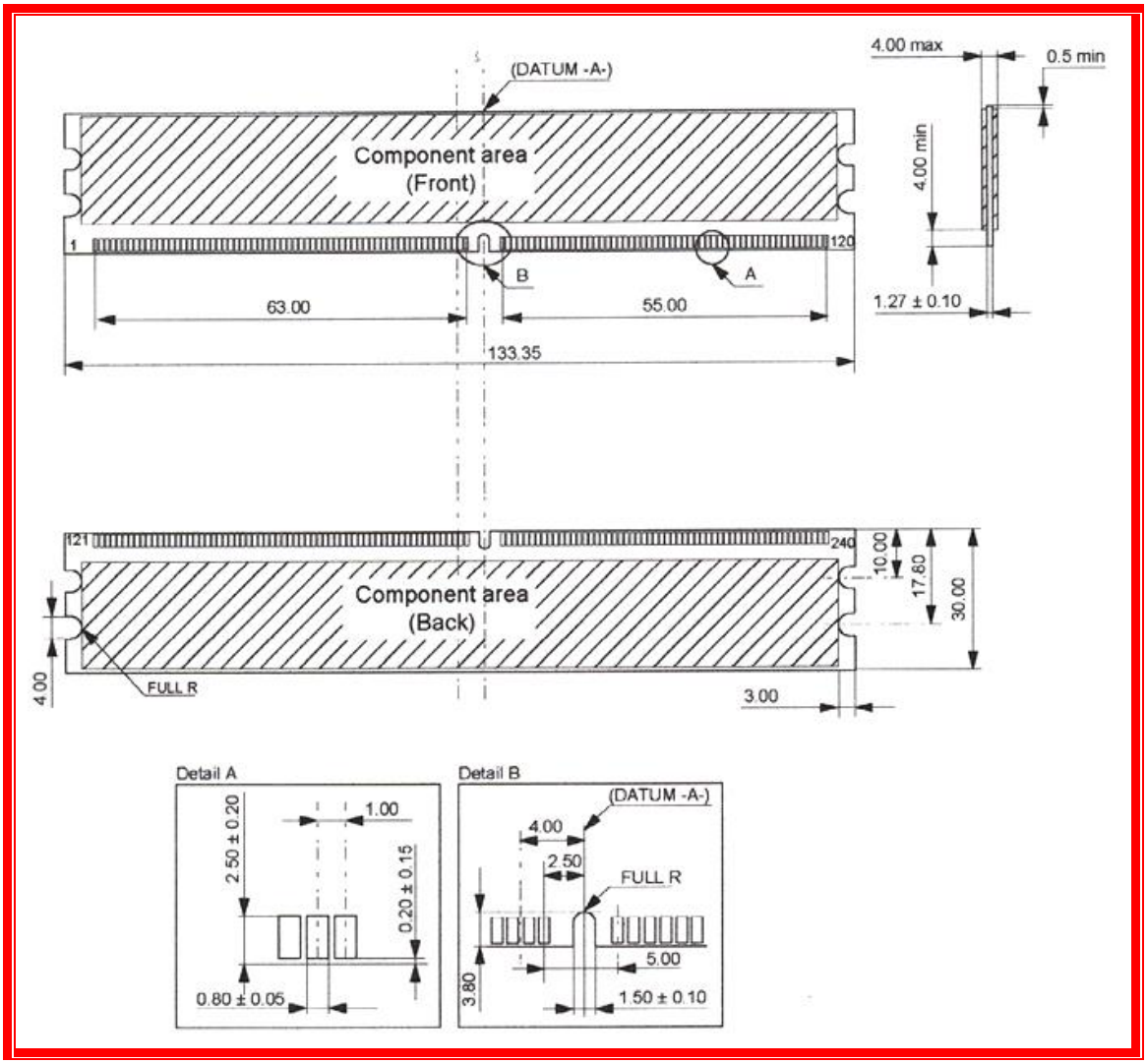
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.40	0.60	tCK
tWPRE	Write preamble	0.35	-	tCK
tIH	Address and control input hold time	250	-	ps
tIS	Address and control input setup time	175	-	ps
tRPRE	Read preamble	0.90	1.10	tCK
tRPST	Read postamble	0.40	0.60	tCK
tRRD	Active bank A to Active bank B command	7.5	-	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	tIS + tCK + tIH	-	ns
tREFI	Average Periodic Refresh Interval ($85^{o}C < T_{CASE} \leq 95^{o}C$)	3.9		µs
	Average Periodic Refresh Interval ($0^{o}C \leq T_{CASE} \leq 85^{o}C$)	7.8		µs
tOIT	OCD drive mode output delay	0	12	ns
tCCD	CAS# to CAS# delay	2		tCK
tWR	Write recovery time without Auto-Precharge	15	-	ns
WR	Write recovery time with Auto-Precharge	tWR/tCK	-	tCK
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	tCK
tWTR	Internal write to read command delay	7.5		ns
tRTP	Internal read to precharge command delay	7.5		ns
tXSNR	Exit self refresh to a Non-read command	tRFC+10		ns
tXSRD	Exit self refresh to a Read command	200		tCK
tXP	Exit precharge power down to any Non- read command	2	-	tCK
tXARD	Exit active power down to read command	2	-	tCK
tXARDS	Exit active power down to read command	8-AL		tCK
tCKE	CKE minimum pulse width	3		tCK

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
tAOND	ODT turn-on delay	2	2	tCK
tAON	ODT turn-on	tAC (min)	tAC (max) +0.7	ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	tCK
tAOF	ODT turn-off	tAC(min)	tAC(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC (min)+2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency	3		tCK
tAXPD	ODT power down exit latency	8		tCK

11. Speed Grade Definition

Symbol	Parameter	PC2-6400		Unit
		CL5		
		Min	Max	
tRAS	Row Active Time	45	70,000	ns
tRC	Row Cycle Time	60	-	ns
tRCD	RAS to CAS delay	15	-	ns
tRP	Row Precharge Time	15	-	ns

12. Physical Dimension



13. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鎮亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

14. SPD

Byte	Function Described	Data (HEX)
0	Number of Serial PD Bytes	80
1	Total number of Bytes in Serial PD device	08
2	Memory Type	08
3	Number of Row Addresses on this assembly	0F
4	Number of Column Addresses on this assembly	0A
5	Number of DIMM Ranks	61
6	Data Width of this assembly	40
7	Reserved	00
8	Voltage Interface Level of this assembly	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	25
10	SDRAM Access from Clock	40
11	DIMM configuration type (Non-parity, Parity or ECC)	00
12	Refresh Rate/Type	82
13	Primary SDRAM Width	08
14	Error Checking SDRAM Width	00
15	Reserved	00
16	SDRAM Device Attributes: Burst Lengths Supported	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	08
18	SDRAM Device Attributes: CAS Latency	38
19	DIMM Mechanical Characteristics	01
20	DIMM Type Information	02
21	SDRAM Module Attributes	00
22	SDRAM Device Attributes: General	07
23	Minimum Clock Cycle at CLX-1	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	45
25	Minimum Clock Cycle at CLX-2	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	50
27	Minimum Row Precharge Time (tRP)	3C
28	Minimum Row Active to Row Active delay (tRRD)	1E
29	Minimum RAS to CAS delay (tRCD)	3C
30	Minimum Active to Precharge Time (tRAS)	2D
31	Module Rank Density	02
32	Address and Command Input Setup Time Before Clock (tIS)	17
33	Address and Command Input Hold Time After Clock (tIH)	25
34	Data Input Setup Time Before Strobe (tDS)	05

35	Data Input Hold Time After Strobe (tDH)	12
36	Write recovery time (tWR)	3C
37	Internal write to read command delay (tWTR)	1E
38	Internal read to precharge command delay (tRTP)	1E
39	Memory Analysis Probe Characteristics	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	00
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	3C
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	C3
43	SDRAM Device Maximum device cycle time (tCKmax)	80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	1E
46	PLL Relock Time	00
47	Tcasemax Delta	00
48	PSIT- A DRAM	00
49	DT0/MODE BITS	00
50	DT2N/DTQ	00
51	DT2P	00
52	DT3N	00
53	DT3Pfast	00
54	DT3Pslow	00
55	DT4R/Mode Bit	00
56	DT5B	00
57	DT7	00
58	PSIT- A PLL	00
59	PSIT-A REG	00
60	DT PLL ACTIVE	00
61	REGSTR ACTIVE/MODE BIT	00
62	SPD REVISION	13
63	CHECKSUM FOR BYTES 0 THRU 62	EA
64	MANUFACTURERS JEDEC ID CODE	7F
65~71	MANUFACTURERS JEDEC ID CODE (CONTINUED)	7F 7F 7F 7F 7F F1 FF
72	MANUFACTURING LOCATION	-
73~90	Module Part Number	-
91~92	Module Revision Code	-
93~94	Module Manufacturing Date	-
95~98	Module Serial Number	-

99~127	Manufacturer's Specific Data	-
128~255	Open for customer use	-

Revision Log

Rev	Date	Modification
0.1	17th May 2016	Preliminary Edition
1.0	17th May 2016	Official Release