

FEATURES

Triaxial, digital gyroscope with digital range scaling
 $\pm 75^\circ/\text{sec}$, $\pm 150^\circ/\text{sec}$, $\pm 300^\circ/\text{sec}$ settings

Tight orthogonal alignment, 0.05°

Triaxial, digital accelerometer, $\pm 18 g$

Triaxial, digital magnetometer, ± 2.5 gauss

Autonomous operation and data collection

No external configuration commands required

220 ms start-up time

4 ms sleep mode recovery time

Factory calibrated sensitivity, bias, and axial alignment

Calibration temperature range: -40°C to $+85^\circ\text{C}$

SPI-compatible serial interface

Embedded temperature sensor

Programmable operation and control

Automatic and manual bias correction controls

Bartlett window FIR length, number of taps

Digital I/O: data ready, alarm indicator, general-purpose

Alarms for condition monitoring

Sleep mode for power management

DAC output voltage

Enable external sample clock input up to 1.2 kHz

Single-command self test

Single-supply operation: 4.75 V to 5.25 V

2000 g shock survivability

Operating temperature range: -40°C to $+105^\circ\text{C}$

APPLICATIONS

Unmanned aerial vehicles

Platform control

Digital compassing

Navigation

GENERAL DESCRIPTION

The **ADIS16405** iSensor[®] product is a complete inertial system that includes a triaxial gyroscope, a triaxial accelerometer, and a triaxial magnetometer. The **ADIS16405** combines the Analog Devices, Inc., proprietary iMEMS[®] technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation for correction formulas that provide accurate sensor measurements over a temperature range of -40°C to $+85^\circ\text{C}$. The magnetometers employ a self correction function to provide accurate bias performance over temperature as well.

FUNCTIONAL BLOCK DIAGRAM

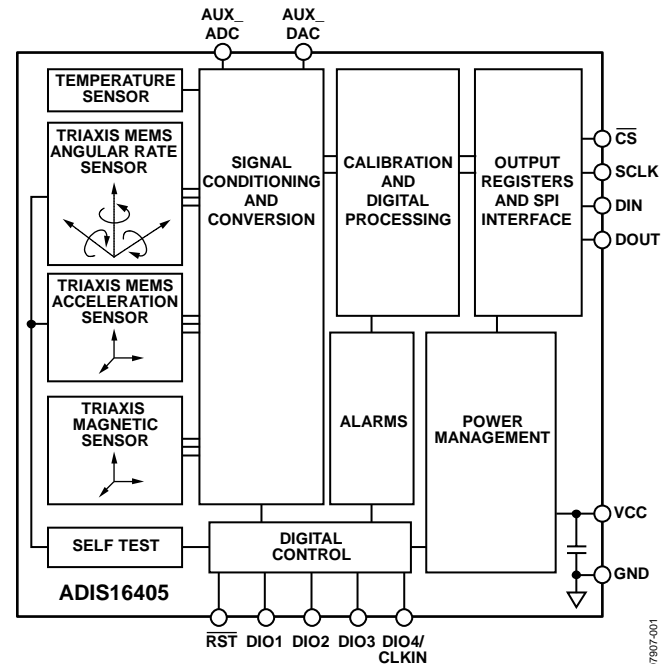


Figure 1.

The **ADIS16405** provides a simple, cost effective method for integrating accurate, multiple axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. An improved serial peripheral interface (SPI) and register structure provide faster data collection and configuration control. By using a compatible pinout and the same package as the **ADIS16362/ADIS16364/ADIS16365/ADIS16367** family, upgrading to the **ADIS16405** requires only firmware changes to accommodate additional sensors and register map updates.

This compact module is approximately 23 mm × 23 mm × 23 mm and provides a flexible connector interface that enables multiple mounting orientation options.

Rev. C

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REVISION HISTORY

1/15—Rev. B to Rev. C

Deleted ADIS16400.....	Universal
Changes to Features Section and General Description Section .	1
Changes to Table 1.....	3
Changes to Figure 2 and Figure 4.....	6
Changes to Table 5.....	8
Changes to Basic Operation Section, Figure 9 Caption, and Device Configuration Section.....	10
Deleted Figure 10; Renumbered Sequentially	10
Added Endnote 1, Table 9	11
Changes to Output Data Registers Section	12
Changes to Internal Sample Rate Section.....	13
Changes to Ordering Guide	16

7/09—Rev. A to Rev. B

Changes to Features Section.....	1
Changes to Data Retention Parameter.....	4
Changes to Table 2.....	6
Changes to Figure 6.....	8
Changes to Device Configuration Section	10
Changes to Table 8.....	11
Changes to Table 9 and Added Default Value to Table 10, Table 11, and Table 12	12

Added Default Value to Table 13, and Table 15 and changes to Internal Sample Rate Section and Table 15.....	13
Added Default Value to Table 17, Table 18, and Table 19 and Changes to Digital Filtering Section.....	14
Added Default Value to Table 20 and Changes to Table 23	15
Added Default Value to Table 24, Table 25, and Table 26 and Changes to Table 24	16
Changes to Ordering Guide	18

4/09—Rev. 0 to Rev. A

Added ADIS16400.....	Universal
Changes to Features	1
Changes to Table 1.....	3
Changes to Figure 5 and Figure 6.....	8
Changes to Reading Sensor Data Section	10
Changes to Internal Sample Rate Section	13
Changes to Input/Output Functions Section.....	14
Changes to Digital Filtering Section.....	14
Changes to Ordering Guide	17

3/09—Revision 0: Initial Version

SPECIFICATIONS

T_A = -40°C to +85°C, VCC = 5.0 V, angular rate = 0°/sec, dynamic range = ±300°/sec, ±1 g, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±300	±350		°/sec
Initial Sensitivity	Dynamic range = ±300°/sec	0.0495	0.05	0.0505	°/sec/LSB
	Dynamic range = ±150°/sec		0.025		°/sec/LSB
	Dynamic range = ±75°/sec		0.0125		°/sec/LSB
Sensitivity Temperature Coefficient	-40°C ≤ T _A ≤ +85°C		±40		ppm/°C
Misalignment	Axis to axis, Δ = 90° ideal		±0.05		Degrees
	Axis to frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line		0.1		% of FS
Initial Bias Error	1 σ		±3		°/sec
In-Run Bias Stability	1 σ, SMPL_PRD = 0x01		0.007		°/sec
Angular Random Walk	1 σ, SMPL_PRD = 0x01		2.0		°/√hr
Bias Temperature Coefficient	-40°C ≤ T _A ≤ +85°C		±0.01		°/sec/°C
Linear Acceleration Effect on Bias	Any axis, 1 σ (MSC_CTRL, Bit 7 = 1)		0.05		°/sec/g
Bias Voltage Sensitivity	VCC = 4.75 V to 5.25 V		0.32		°/sec/V
Output Noise	±300°/sec range, no filtering		0.9		°/sec rms
Rate Noise Density	f = 25 Hz, ±300°/sec, no filtering		0.05		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Resonant Frequency			14.3		kHz
Self Test Change in Output Response	±300°/sec range setting	±696		±2449	LSB
ACCELEROMETERS					
Dynamic Range		±18			g
Initial Sensitivity		3.285	3.33	3.38	mg/LSB
Sensitivity Temperature Coefficient	-40°C ≤ T _A ≤ +85°C		±50		ppm/°C
Misalignment	Axis to axis, Δ = 90° ideal		0.2		Degrees
	Axis to frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line, ±17 g		0.1		% of FS
Initial Bias Error	1 σ		±50		mg
In-Run Bias Stability	1 σ		0.2		mg
Velocity Random Walk	1 σ		0.2		m/sec/√hr
Bias Temperature Coefficient	-40°C ≤ T _A ≤ +85°C		±0.3		mg/°C
Bias Voltage Sensitivity	VCC = 4.75 V to 5.25 V		2.5		mg/V
Output Noise	No filtering		9		mg rms
Noise Density	No filtering		0.5		mg/√Hz rms
3 dB Bandwidth			330		Hz
Resonant Frequency			5.5		kHz
Self Test Change in Output Response		59		151	LSB
MAGNETOMETER					
Dynamic Range		±2.5	±3.5		gauss
Initial Sensitivity	25°C	0.49	0.5	0.51	mgauss/LSB
Sensitivity Temperature Coefficient	25°C, 1 σ		600		ppm/°C
Axis Nonorthogonality	25°C, axis to axis		0.25		Degrees
Axis Misalignment	25°C, axis to base plate and guide pins		0.5		Degrees
Nonlinearity	Best fit straight line		0.5		% of FS
Initial Bias Error	25°C, 0 gauss stimulus		±4		mgauss
Bias Temperature Coefficient			0.5		mgauss/°C
Output Noise	25°C, no filtering		1.25		mgauss rms
Noise Density	25°C, no filtering, rms		0.066		mgauss/√Hz
3 dB Bandwidth			1540		Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Scale Factor	25°C, output = 0x0000		0.14		°C/LSB
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		3.3	V
Input Capacitance	During acquisition		20		pF
DAC OUTPUT					
Resolution			12		Bits
Relative Accuracy	Code 101 to Code 4095, 5 kΩ/100 pF to GND		±4		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range		0		3.3	V
Output Impedance			2		Ω
Output Settling Time	5 kΩ/100 pF to GND		10		μs
LOGIC INPUTS ¹					
Input High Voltage, V _{INH}		2.0			V
Input Low Voltage, V _{INL}				0.8	V
$\overline{\text{CS}}$ Wake-Up Pulse Width	$\overline{\text{CS}}$ signal to wake up from sleep mode			0.55	V
Logic 1 Input Current, I _{INH}	V _{IH} = 3.3 V		±0.2	±10	μA
Logic 0 Input Current, I _{INL}	V _{IL} = 0 V				μA
All Pins Except $\overline{\text{RST}}$			-40	-60	μA
$\overline{\text{RST}}$ Pin			-1		mA
Input Capacitance, C _{IN}			10		pF
DIGITAL OUTPUTS ¹					
Output High Voltage, V _{OH}	I _{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V _{OL}	I _{SINK} = 1.6 mA			0.4	V
FLASH MEMORY					
Data Retention ³	Endurance ² T _J = 85°C	10,000 20			Cycles Years
FUNCTIONAL TIMES ⁴	Time until data is available				
Power-On Start-Up Time	Normal mode, SMPL_PRD ≤ 0x09		220		ms
	Low power mode, SMPL_PRD ≥ 0x0A		290		ms
Reset Recovery Time	Normal mode, SMPL_PRD ≤ 0x09		100		ms
	Low power mode, SMPL_PRD ≥ 0x0A		170		ms
Sleep Mode Recovery Time	Normal mode, SMPL_PRD ≤ 0x09		4		ms
	Low power mode, SMPL_PRD ≥ 0x0A		15		ms
Flash Memory Test Time	Normal mode, SMPL_PRD ≤ 0x09		17		ms
	Low power mode, SMPL_PRD ≥ 0x0A		90		ms
Flash Memory Update Time			50		ms
Automatic Self Test Time	SMPL_PRD = 0x01		12		ms
CONVERSION RATE	SMPL_PRD = 0x01 to 0xFF	0.413		819.2	SPS
Clock Accuracy				±3	%
Sync Input Clock				1.2	kHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range, VCC		4.75	5.0	5.25	V
Power Supply Current	Low power mode at $T_A = 25^\circ\text{C}$		45		mA
	Normal mode at $T_A = 25^\circ\text{C}$		70		mA
	Sleep mode at $T_A = 25^\circ\text{C}$		600		μA

¹ The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.

² Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at -40°C , $+25^\circ\text{C}$, $+85^\circ\text{C}$, and $+125^\circ\text{C}$.

³ The data retention lifetime equivalent is at a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.

⁴ These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.

TIMING SPECIFICATIONS

T_A = 25°C, VCC = 5 V, unless otherwise noted.

Table 2.

Parameter	Description	Normal Mode (SMPL_PRD ≤ 0x09)			Low Power Mode (SMPL_PRD ≥ 0x0A)			Burst Mode			Unit
		Min ¹	Typ	Max	Min ¹	Typ	Max	Min ¹	Typ	Max	
f _{SCLK}	Serial clock frequency	0.01		2.0	0.01		0.3	0.01		1.0	MHz
t _{STALL}	Stall period between data	9			75			1/f _{SCLK}			μs
t _{READRATE}	Read rate	40			150						μs
t _{CS}	Chip select to clock edge	48.8			48.8			48.8			ns
t _{DAV}	DOUT valid after SCLK edge			100			100			100	ns
t _{DSU}	DIN setup time before SCLK rising edge	24.4			24.4			24.4			ns
t _{DHD}	DIN hold time after SCLK rising edge	48.8			48.8			48.8			ns
t _{SCLKR} , t _{SCLKF}	SCLK rise/fall times		5	12.5		5	12.5		5	12.5	ns
t _{DF} , t _{DR}	DOUT rise/fall times		5	12.5		5	12.5		5	12.5	ns
t _{SFS}	\overline{CS} high after SCLK edge	5			5			5			ns
t ₁	Input sync pulse width		5						5		μs
t ₂	Input sync to data ready output		600						600		μs
t ₃	Input sync period	833						833			μs

¹Guaranteed by design and characterization but not tested in production.

TIMING DIAGRAMS

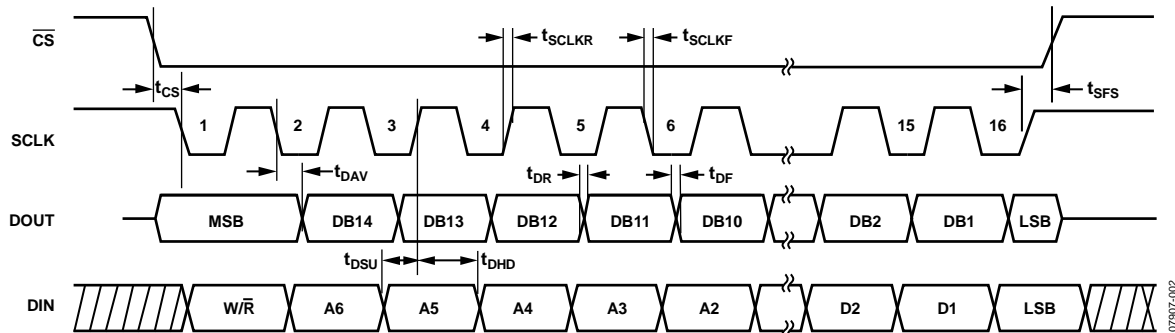


Figure 2. SPI Timing and Sequence

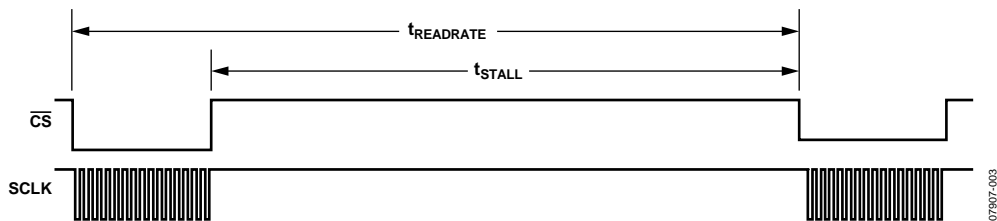


Figure 3. Stall Time and Data Rate

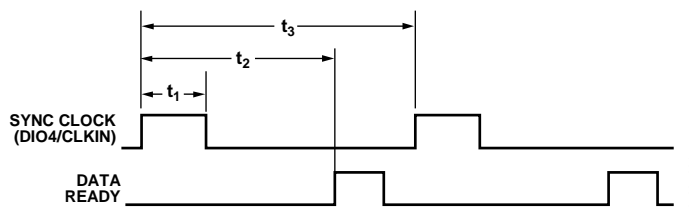


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 <i>g</i>
Any Axis, Powered	2000 <i>g</i>
VCC to GND	−0.3 V to +6.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VCC + 0.3 V
Analog Input to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C ^{1,2}

¹ Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the devices within the specified operating range of −40°C to +105°C.

² Although the device is capable of withstanding short term exposure to 125°C and above, long-term exposure threatens internal mechanical integrity.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. Package Characteristics

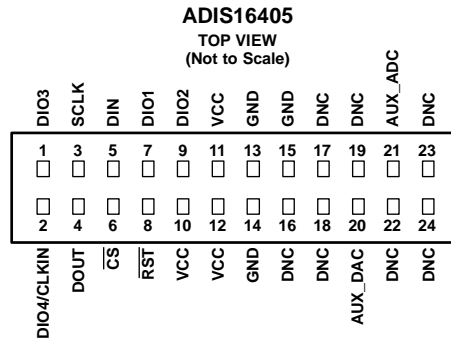
Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module	39.8°C/W	14.2°C/W	16 g

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

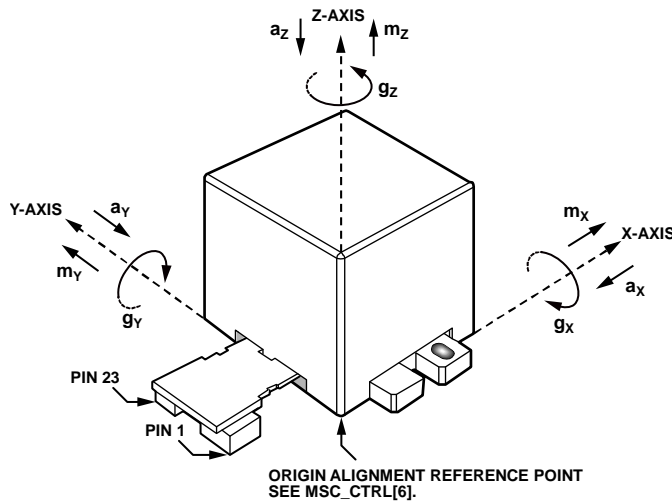
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. THIS VIEW REPRESENTS THE TOP VIEW OF THE MATING CONNECTOR.
 2. WHEN CONNECTED TO THE ADIS16405, THE PINS ARE NOT VISIBLE.
 3. MATING CONNECTOR: SAMTEC CLM-112-02 OR EQUIVALENT.
 4. DNC = DO NOT CONNECT.

07907-005

Figure 5. Pin Configuration



- NOTES**
1. a_x, a_y, a_z , ARROWS INDICATE THE DIRECTION OF ACCELERATION THAT PRODUCES A POSITIVE OUTPUT.
 2. g_x, g_y, g_z , ARROWS INDICATE THE DIRECTION OF ROTATION THAT PRODUCES A POSITIVE OUTPUT.
 3. m_x, m_y, m_z , ARROWS INDICATE THE DIRECTION OF MAGNETIC FIELD THAT PRODUCES A POSITIVE OUTPUT.

07907-006

Figure 6. Axial Orientation

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	DIO3	I/O	Configurable Digital Input/Output 3.
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output 4 or Sync Clock Input.
3	SCLK	I	SPI Serial Clock.
4	DOUT	O	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks input on SCLK rising edge.
6	CS	I	SPI Chip Select.
7	DIO1	I/O	Configurable Digital Input/Output 1.
8	RST	I	Reset.
9	DIO2	I/O	Configurable Digital Input/Output 2.
10, 11, 12	VCC	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16, 17, 18, 19, 22, 23, 24	DNC	N/A	Do Not Connect. Do not connect to these pins.
20	AUX_DAC	O	Auxiliary, 12-Bit Digital-to-Analog Converter (DAC) Output.
21	AUX_ADC	I	Auxiliary, 12-Bit Analog-to-Digital Converter (ADC) Input.

TYPICAL PERFORMANCE CHARACTERISTICS

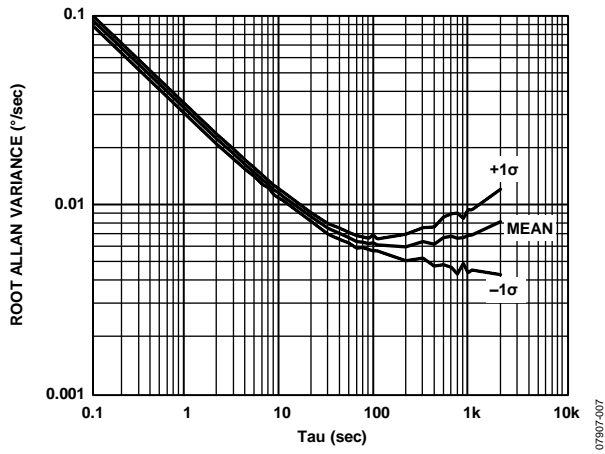


Figure 7. Gyroscope Root Allan Variance

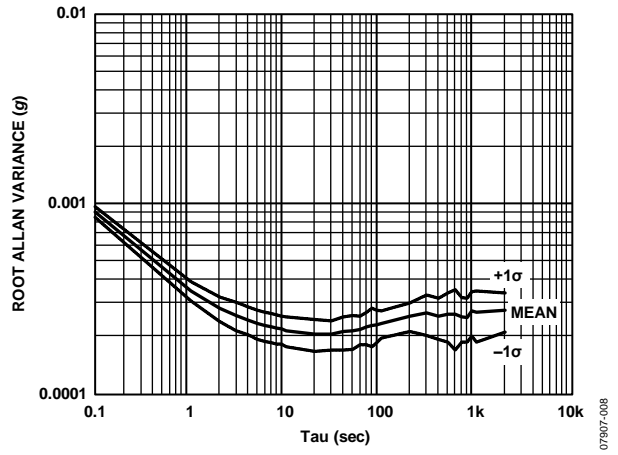


Figure 8. Accelerometer Root Allan Variance

THEORY OF OPERATION

BASIC OPERATION

The ADIS16405 is an autonomous system that requires no user initialization. When it has a valid power supply, it initializes itself and starts sampling, processing, and loading sensor data into the output registers at a sample rate of 819.2 SPS. DIO1 pulses high after each sample cycle concludes. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 9 and Table 6.

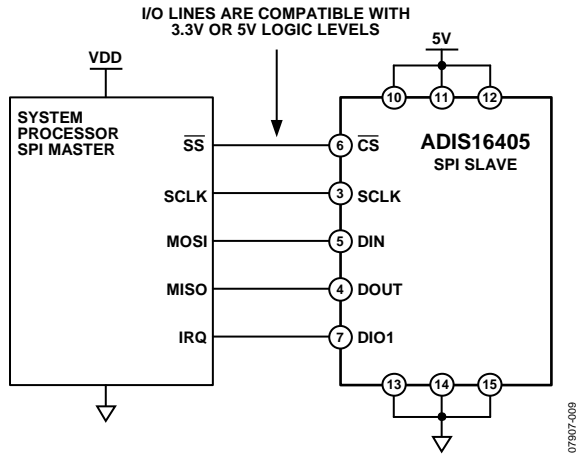


Figure 9. Electrical Connection Diagram

Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
SS	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

The ADIS16405 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 10. Table 7 provides a list of the most common settings that require attention to initialize the serial port of a processor for the ADIS16405 SPI interface.

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16405 operates as a slave.
SCLK Rate \leq 2 MHz ¹	Normal mode, SMPL_PRD[7:0] \leq 0x08.
CPOL = 1	Clock polarity.
CPHA = 1	Clock phase.
MSB First	Bit sequence.
16-Bit	Shift register/data length.

¹ For burst mode, SCLK rate \leq 1 MHz. For low power mode, SCLK rate \leq 300 kHz.

READING SENSOR DATA

Although the ADIS16405 produces data independently, it operates as a SPI slave device that communicates with system (master) processors using the 16-bit segments displayed in Figure 10. Individual register reads require two such 16-bit sequences. The first 16-bit sequence provides the read command bit ($\bar{R}/W = 0$) and the target register address (A6 to A0). The second sequence transmits the register contents (D15 to D0) on the DOUT line. For example, if DIN = 0x0A00, the content of XACCL_OUT shifts out on the DOUT line during the next 16-bit sequence.

The SPI operates in full duplex mode, which means that the master processor can read the output data from DOUT while using the same SCLK pulses to transmit the next target address on DIN.

DEVICE CONFIGURATION

The user register memory map (see Table 8) identifies configuration registers with either a W (write only) or R/W (read/write). Configuration commands also use the bit sequence displayed in Figure 10. If the MSB is equal to 1, the last eight bits (DC7 to DC0) in the DIN sequence load into the memory address associated with the address bits (A6 to A0). For example, if DIN = 0xA11F, then 0x1F loads into Address Location 0x21 (XACCL_OFF, upper byte) at the conclusion of the data frame.

Most of the registers have a backup location in nonvolatile flash memory. The master processor must manage the backup function. Set GLOB_CMD[3] = 1 (DIN = 0xBE04) to execute a manual flash update (backup) operation, which copies the user registers into their respective flash memory locations. This operation takes 50 ms and requires the power supply voltage to be within the specified limit to complete properly. The FLASH_CNT register provides a running count of these events for managing the long-term reliability of the flash memory.

BURST MODE DATA COLLECTION

Burst mode data collection offers a more efficient method for collecting data from the ADIS16405. In sequential data cycles (each separated by one SCLK period), all output registers clock out on DOUT. This sequence starts when the DIN sequence is 0011 1110 0000 0000 (0x3E00). Next, the contents of each output register are output from DOUT, starting with SUPPLY_OUT and ending with AUX_ADC (see Figure 11). The addressing sequence shown in Table 8 determines the order of the outputs in burst mode.

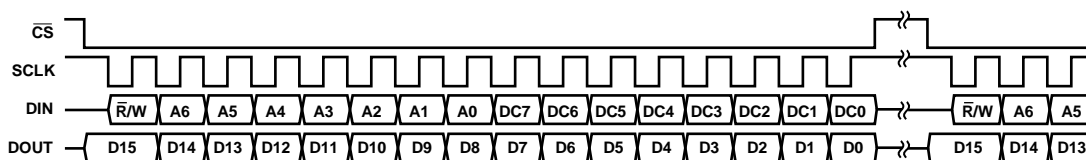
MEMORY MAP

Table 8. User Register Memory Map¹

Name	R/W	Flash Backup	Address ²	Default	Function	Bit Assignments
FLASH_CNT	R	Yes	0x00	N/A	Flash memory write count	N/A
SUPPLY_OUT	R	No	0x02	N/A	Power supply measurement	See Table 9
XGYRO_OUT	R	No	0x04	N/A	X-axis gyroscope output	See Table 9
YGYRO_OUT	R	No	0x06	N/A	Y-axis gyroscope output	See Table 9
ZGYRO_OUT	R	No	0x08	N/A	Z-axis gyroscope output	See Table 9
XACCL_OUT	R	No	0x0A	N/A	X-axis accelerometer output	See Table 9
YACCL_OUT	R	No	0x0C	N/A	Y-axis accelerometer output	See Table 9
ZACCL_OUT	R	No	0x0E	N/A	Z-axis accelerometer output	See Table 9
XMAGN_OUT	R	No	0x10	N/A	X-axis magnetometer measurement	See Table 9
YMAGN_OUT	R	No	0x12	N/A	Y-axis magnetometer measurement	See Table 9
ZMAGN_OUT	R	No	0x14	N/A	Z-axis magnetometer measurement	See Table 9
TEMP_OUT	R	No	0x16	N/A	Temperature output	See Table 9
AUX_ADC	R	No	0x18	N/A	Auxiliary ADC measurement	See Table 9
XGYRO_OFF	R/W	Yes	0x1A	0x0000	X-axis gyroscope bias offset factor	See Table 10
YGYRO_OFF	R/W	Yes	0x1C	0x0000	Y-axis gyroscope bias offset factor	See Table 10
ZGYRO_OFF	R/W	Yes	0x1E	0x0000	Z-axis gyroscope bias offset factor	See Table 10
XACCL_OFF	R/W	Yes	0x20	0x0000	X-axis acceleration bias offset factor	See Table 11
YACCL_OFF	R/W	Yes	0x22	0x0000	Y-axis acceleration bias offset factor	See Table 11
ZACCL_OFF	R/W	Yes	0x24	0x0000	Z-axis acceleration bias offset factor	See Table 11
XMAGN_HIF	R/W	Yes	0x26	0x0000	X-axis magnetometer, hard iron factor	See Table 12
YMAGN_HIF	R/W	Yes	0x28	0x0000	Y-axis magnetometer, hard iron factor	See Table 12
ZMAGN_HIF	R/W	Yes	0x2A	0x0000	Z-axis magnetometer, hard iron factor	See Table 12
XMAGN_SIF	R/W	Yes	0x2C	0x0800	X-axis magnetometer, soft iron factor	See Table 13
YMAGN_SIF	R/W	Yes	0x2E	0x0800	Y-axis magnetometer, soft iron factor	See Table 13
ZMAGN_SIF	R/W	Yes	0x30	0x0800	Z-axis magnetometer, soft iron factor	See Table 13
GPIO_CTRL	R/W	No	0x32	0x0000	Auxiliary digital input/output control	See Table 18
MSC_CTRL	R/W	Yes	0x34	0x0006	Miscellaneous control	See Table 19
SMPL_PRD	R/W	Yes	0x36	0x0001	Internal sample period (rate) control	See Table 15
SENS_AVG	R/W	Yes	0x38	0x0402	Dynamic range and digital filter control	See Table 17
SLP_CNT	W	No	0x3A	0x0000	Sleep mode control	See Table 16
DIAG_STAT	R	No	0x3C	0x0000	System status	See Table 23
GLOB_CMD	W	N/A	0x3E	0x0000	System command	See Table 14
ALM_MAG1	R/W	Yes	0x40	0x0000	Alarm 1 amplitude threshold	See Table 25
ALM_MAG2	R/W	Yes	0x42	0x0000	Alarm 2 amplitude threshold	See Table 25
ALM_SMPL1	R/W	Yes	0x44	0x0000	Alarm 1 sample size	See Table 26
ALM_SMPL2	R/W	Yes	0x46	0x0000	Alarm 2 sample size	See Table 26
ALM_CTRL	R/W	Yes	0x48	0x0000	Alarm control	See Table 24
AUX_DAC	R/W	No	0x4A	0x0000	Auxiliary DAC data	See Table 20
PRODUCT_ID			0x4C to 0x55		Reserved	
			0x56	0x4105	Product identifier	

¹ N/A means not applicable.

² Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.



NOTES

1. DOUT BITS ARE BASED ON THE PREVIOUS 16-BIT SEQUENCE ($\bar{R} = 0$).

Figure 10. SPI Communication Bit Assignments

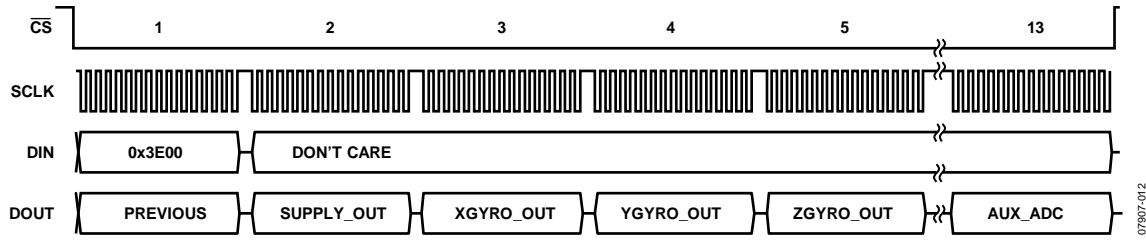


Figure 11. Burst Mode Read Sequence

OUTPUT DATA REGISTERS

Figure 6 provides the positive measurement direction for each gyroscope, accelerometer, and magnetometer. Table 9 provides the configuration and scale factor for each output data register in the ADIS16405. All inertial sensor outputs are in 14-bit, twos complement format, which means that 0x0000 is equal to 0 LSB, 0x0001 is equal to +1 LSB, and 0x3FFF is equal to -1 LSB. The following is an example of how to calculate the sensor measurement from the XGYRO_OUT:

$$XGYRO_OUT = 0x3B4A$$

$$0x000 - 0x3B4A = -0x04B6 = (4 \times 256 + 11 \times 16 + 6) - 0x04B6 = -1206 \text{ LSB}$$

$$Rate = 0.05^\circ/\text{sec} \times (-1206) = -60.3^\circ/\text{sec}$$

Therefore, an ZGYRO_OUT output of 0x3B4A corresponds to a clockwise rotation around the z-axis (see Figure 6) of 60.3°/sec when looking at the top of the package.

Table 9. Output Data Register Formats

Register	Bits	Format	Scale
SUPPLY_OUT	14	Binary, 5 V = 0x0814	2.418 mV
XGYRO_OUT ¹	14	Twos complement	0.05°/sec
YGYRO_OUT ¹	14	Twos complement	0.05°/sec
ZGYRO_OUT ¹	14	Twos complement	0.05°/sec
XACCL_OUT	14	Twos complement	3.33 mg
YACCL_OUT	14	Twos complement	3.33 mg
ZACCL_OUT	14	Twos complement	3.33 mg
XMAGN_OUT	14	Twos complement	0.5 mgauss
YMAGN_OUT	14	Twos complement	0.5 mgauss
ZMAGN_OUT	14	Twos complement	0.5 mgauss
TEMP_OUT ²	12	Twos complement	0.14°C
AUX_ADC	12	Binary, 1 V = 0x04D9	806 μV

¹ Assumes that the scaling is set to ±300°/sec. This factor scales with the range.
² The typical output for this register at 25°C is 0x0000.

Each output data register uses the bit assignments shown in Figure 12. The ND flag indicates that unread data resides in the output data registers. This flag clears and returns to 0 during an output register read sequence. It returns to 1 after the next internal sample updates the registers with new data. The EA flag indicates that one of the error flags in the DIAG_STAT register (see Table 23) is active (true). The remaining 14 bits are for data.

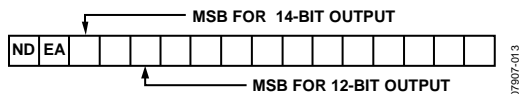


Figure 12. Output Register Bit Assignments

Auxiliary ADC

The AUX_ADC register provides access to the auxiliary ADC input channel. The ADC is a 12-bit successive approximation converter that has an equivalent input circuit to the one shown in Figure 13. The maximum input is 3.3 V. The ESD protection diodes can handle 10 mA without causing irreversible damage. The on resistance (R1) of the switch has a typical value of 100 Ω. The sampling capacitor, C2, has a typical value of 16 pF.

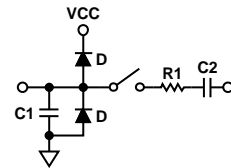


Figure 13. Equivalent Analog Input Circuit
 (Conversion Phase: Switch Open, Track Phase: Switch Closed)

CALIBRATION

Manual Bias Calibration

The bias offset registers in Table 10, Table 11, and Table 12 (hard iron correction for magnetometer) provide a manual adjustment function for the output of each sensor. For example, if XGYRO_OFF equals 0x1FF6, the XGYRO_OUT offset shifts by -10 LSB, or -0.125°/sec. The DIN command for the upper byte is DIN = 0x9B1F; for the lower byte, DIN = 0x9AF6.

Table 10. XGYRO_OFF, YGYRO_OFF, ZGYRO_OFF

Bits	Description (Default = 0x0000)
[15:13]	Not used.
[12:0]	Data bits. Twos complement, 0.0125°/sec per LSB. Typical adjustment range = ±50°/sec.

Table 11. XACCL_OFF, YACCL_OFF, ZACCL_OFF

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:0]	Data bits. Twos complement, 3.33 mg/LSB. Typical adjustment range = ±6.75 g.

Table 12. XMAGN_HIF, YMAGN_HIF, ZMAGN_HIF

Bits	Description (Default = 0x0000)
[15:14]	Not used.
[13:0]	Data bits. Twos complement, 0.5 mgauss/LSB. Typical adjustment range = ±4 gauss.

Magnetometer Soft Iron Correction (Scale Factor)

The soft iron correction factor for the magnetometer provides the opportunity to change the scale factor for each individual axis.

Table 13. XMAGN_SIF, YMAGN_SIF, ZMAGN_SIF

Bits	Description (Default = 0x0800)
[15:12]	Not used.
[11:0]	Data bits. Binary, linear scale adjustment factor between 0x0000 (0x) and 0x3FFF (2x).

Gyroscope Automatic Bias Null Calibration

Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute this function, which measures the gyroscope outputs and then loads the gyroscope offset registers with the opposite values to provide a quick bias calibration. Then, all sensor data resets to 0, and the flash memory updates automatically within 50 ms (see Table 14).

Gyroscope Precision Automatic Bias Null Calibration

Set GLOB_CMD[4] = 1 (DIN = 0xBE10) to execute this function, which takes the sensor offline for 30 sec while it collects a set of gyroscope data and calculates a more accurate bias correction factor for each gyroscope. When calculated, the correction factor loads into the three gyroscope offset registers, all sensor data resets to 0, and the flash memory updates automatically within 50 ms (see Table 14).

Restoring Factory Calibration

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute this function, which resets each user calibration register (see Table 10, Table 11, and Figure 11) to 0x0000, resets all sensor data to 0, and automatically updates the flash memory within 50 ms (see Table 14).

Linear Acceleration Bias Compensation (Gyroscope)

Set MSC_CTRL[7] = 1 (DIN = 0xB486) to enable correction for low frequency acceleration influences on gyroscope bias. Note that the DIN sequence also preserves the factory default condition for the data ready function (see Table 19).

OPERATIONAL CONTROL**Global Commands**

The GLOB_CMD register provides trigger bits for several useful functions. Setting the assigned bit to 1 starts each operation, which returns the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This includes loading the control registers with their respective flash memory locations prior to producing new data. Reading the GLOB_CMD registers (DIN = 0x3E00) starts the burst mode read sequence.

Table 14. GLOB_CMD

Bits	Description
[15:8]	Not used
7	Software reset command
[6:5]	Not used
4	Precision autonull command
3	Flash update command
2	Auxiliary DAC data latch
1	Factory calibration restore command
0	Autonull command

Internal Sample Rate

The SMPL_PRD register provides discrete sample rate settings, using the bit assignments in Table 15 and the following equation:

$$t_s = t_B \times (N_s + 1)$$

where:

t_s is the sample rate. When SMPL_PRD[7:0] = 0x0A, the sample rate is 149 SPS.

t_B is the time base.

N_s is the increment setting.

Table 15. SMPL_PRD

Bits	Description (Default = 0x0001)
[15:8]	Not used
7	Time base (t_B) 0 = 0.61035 ms, 1 = 18.921 ms
[6:0]	Increment setting (N_s) Internal sample period = $t_s = t_B \times (N_s + 1)$

The default sample rate setting of 819.2 SPS preserves the sensor bandwidth and provides optimal performance. For systems that value slower sample rates, simply read the device at a slower rate and keep the internal sample rate at 819.2 SPS. Use the programmable filter (SENS_AVG) to reduce the bandwidth along with the reduced read rates. The data-ready function (MSC_CTRL) can drive an interrupt routine that uses a counter to help ensure data coherence at the reduced update rates.

Power Management

Setting SMPL_PRD \geq 0x0A also sets the sensor in low power mode. For systems that require the lower power dissipation, in-system characterization helps users to quantify the associated performance trade-offs. In addition to sensor performance, this mode affects SPI data rates (see Table 2). Set SLP_CNT[8] = 1 (DIN = 0xBB01) to start the indefinite sleep mode, which requires a \overline{CS} assertion (high to low), reset, or power cycle to wake up. Use SLP_CNT[7:0] to put the device in sleep mode for a given period of time. For example, SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the device to sleep for 50 seconds.

Table 16. SLP_CNT

Bits	Description
[15:9]	Not used
8	Indefinite sleep mode, set to 1
[7:0]	Programmable sleep time bits, 0.5 sec/LSB

Digital Filtering

A programmable low-pass filter provides additional opportunity for noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window FIR filter response (see Figure 14). For example, SENS_AVG[2:0] = 100 (DIN = B804) sets each stage tap to 16. When used with the default sample rate of 819.2 SPS, this filter setting reduces the sensor bandwidth to approximately 16 Hz.

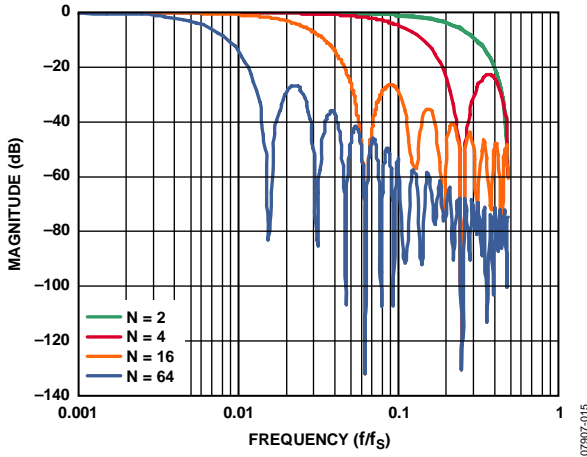


Figure 14. Bartlett Window FIR Frequency Response (Taps = 2N + 1, Phase = N Samples)

Dynamic Range

There are three dynamic range settings for the gyroscope. The lower dynamic range settings ($\pm 75^\circ/\text{sec}$ and $\pm 150^\circ/\text{sec}$) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of $\pm 150^\circ/\text{sec}$. Because this setting can influence the filter settings, program SENS_AVG[10:8], then SENS_AVG[2:0] if more filtering is required.

Table 17. SENS_AVG

Bits	Description (Default = 0x0402)
[15:11]	Not used
[10:8]	Measurement range (sensitivity) selection 100 = $\pm 300^\circ/\text{sec}$ (default condition) 010 = $\pm 150^\circ/\text{sec}$, filter taps ≥ 4 (Bits[2:0] $\geq 0x02$) 001 = $\pm 75^\circ/\text{sec}$, filter taps ≥ 16 (Bits[2:0] $\geq 0x04$)
[7:3]	Not used
[2:0]	Number of taps in each stage $N = 2^M$

INPUT/OUTPUT FUNCTIONS

General-Purpose I/O

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x080C (DIN = 0xB308, and then 0xB20C) to set DIO1 and DIO2 as inputs and DIO3 and DIO4 as outputs, with DIO3 set low and DIO4 set high.

Table 18. GPIO_CTRL

Bits	Description (Default = 0x0000)
[15:12]	Not used
11	General-Purpose I/O Line 4 (DIO4) data level
10	General-Purpose I/O Line 3 (DIO3) data level
9	General-Purpose I/O Line 2 (DIO2) data level
8	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Not used
3	General-Purpose I/O Line 4 (DIO4), direction control 1 = output, 0 = input
2	General-Purpose I/O Line 3 (DIO3), direction control 1 = output, 0 = input
1	General-Purpose I/O Line 2 (DIO2), direction control 1 = output, 0 = input
0	General-Purpose I/O Line 1 (DIO1), direction control 1 = output, 0 = input

Input Clock Configuration

The input clock allows external control over sampling in the ADIS16405. Set GPIO_CTRL[3] = 0 (DIN = 0x0B200) and SMPL_PRD[7:0] = 0x00 (DIN = 0xB600) to enable this function. See Table 2 and Figure 4 for timing information.

Data Ready I/O Indicator

The factory default sets DIO1 as a positive data ready indicator signal. The MSC_CTRL[2:0] register provides configuration options for changing this. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal for interrupt inputs that require negative logic inputs for activation. The resulting pulse width is between 100 μs and 200 μs over all conditions.

Table 19. MSC_CTRL

Bits	Description (Default = 0x0006)
[15:12]	Not used
11	Memory test (clears on completion) 1 = enabled, 0 = disabled
10	Internal self test enable (clears on completion) 1 = enabled, 0 = disabled
9	Manual self test, negative stimulus 1 = enabled, 0 = disabled
8	Manual self test, positive stimulus 1 = enabled, 0 = disabled
7	Linear acceleration bias compensation for gyroscopes 1 = enabled, 0 = disabled
6	Linear accelerometer origin alignment 1 = enabled, 0 = disabled
[5:3]	Not used
2	Data ready enable 1 = enabled, 0 = disabled
1	Data ready polarity 1 = active high, 0 = active low
0	Data ready line select 1 = DIO2, 0 = DIO1

Auxiliary DAC

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

Table 20. AUX_DAC

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:0]	Data bits. Scale factor = 0.8059 mV/code, offset binary format, 0 V = 0 codes.

Table 21. Setting AUX_DAC = 1 V

DIN	Description
0xB0D9	AUX_DAC[7:0] = 0xD9 (217 LSB).
0xB104	AUX_DAC[15:8] = 0x04 (1024 LSB).
0xBE04	GLOB_CMD[2] = 1. Move values into the DAC input register, resulting in a 1 V output level.

DIAGNOSTICS

Self Test

The self test function offers the opportunity to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self test routine, which exercises all inertial sensors, measures each response, makes pass/fail decisions, and reports them to error flags in the DIAG_STAT register. MSC_CTRL[10] resets itself to 0 after completing the routine. MSC_CTRL[9:8] (DIN = 0xB502 or 0xB501) provide manual control over the self test function. Table 22 shows an example test flow for using this option to check the x-axis gyroscope. Zero motion provides results that are more reliable. The settings in Table 22 are flexible and provide opportunity for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the opportunity for noise influence.

Memory Test

Setting MSC_CTRL[11] = 1 (DIN = 0xB508) performs a checksum verification of the flash memory locations. The pass/fail result loads into DIAG_STAT[6].

Status

The error flags provide indicator functions for common system level issues. All of the flags clear (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. DIAG_STAT[1:0] does not require a read of this register to return to 0.

Table 22. Manual Self Test Example Sequence

DIN	Description
0xB601	SMPL_PRD[7:0] = 0x01, sample rate = 819.2 SPS.
0xB904	SENS_AVG[15:8] = 0x04, gyroscope range = ±300°/sec.
0xB802	SENS_AVG[7:0] = 0x02, four-tap averaging filter. Delay = 50 ms.
0x0400	Read XGYRO_OUT.
0xB502	MSC_CTRL[9] = 1, gyroscope negative self test. Delay = 50 ms.
0x0400	Read XGYRO_OUT. Calculate the positive change from the first reading to the second reading of XGYRO_OUT, and check to make sure the change is within the positive self test response range specified in Table 1.
0xB501	MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self test. Delay = 50 ms.
0x0400	Read XGYRO_OUT. Calculate the negative change from the first reading to the third reading of XGYRO_OUT, and check to make sure the change is within the positive self test response range specified in Table 1.
0xB500	MSC_CTRL[15:8] = 0x00.

Table 23. DIAG_STAT Bit Descriptions

Bit	Description
15	Z-axis accelerometer self test failure 1 = fail, 0 = pass
14	Y-axis accelerometer self test failure 1 = fail, 0 = pass
13	X-axis accelerometer self test failure 1 = fail, 0 = pass
12	Z-axis gyroscope self test failure 1 = fail, 0 = pass
11	Y-axis gyroscope self test failure 1 = fail, 0 = pass
10	X-axis gyroscope self test failure 1 = fail, 0 = pass
9	Alarm 2 status 1 = active, 0 = inactive
8	Alarm 1 status 1 = active, 0 = inactive
7	Not used
6	Flash test, checksum flag 1 = fail, 0 = pass
5	Self test diagnostic error flag 1 = fail, 0 = pass
4	Sensor overrange 1 = fail, 0 = pass
3	SPI communication failure 1 = fail, 0 = pass
2	Flash update failure 1 = fail, 0 = pass
1	Power supply above 5.25 V 1 = power supply ≥ 5.25 V, 0 = power supply ≤ 5.25 V
0	Power supply below 4.75 V 1 = power supply ≤ 4.75 V, 0 = power supply ≥ 4.75 V

Alarm Registers

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static comparison, dynamic rate of change (ROC) comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations.

Table 27 gives an example of how to configure a static alarm. The ALM_SMPLx registers provide the number of samples to use in the dynamic ROC configuration. The period equals the number in the ALM_SMPLx register multiplied by the sample period time, which is established by the SMPL_PRD register. See Table 28 for an example of how to configure the sensor for this type of function.

Table 24. ALM_CTRL Bit Designations

Bits	Description (Default = 0x0000)
[15:12]	Alarm 2 source selection 0000 = disable 0001 = power supply output 0010 = x-axis gyroscope output 0011 = y-axis gyroscope output 0100 = z-axis gyroscope output 0101 = x-axis accelerometer output 0110 = y-axis accelerometer output 0111 = z-axis accelerometer output 1000 = x-axis magnetometer output 1001 = y-axis magnetometer output 1010 = z-axis magnetometer output 1011 = gyroscope temperature output 1100 = auxiliary ADC input
[11:8]	Alarm 1 source selection (same as Alarm 2)
7	ROC enable for Alarm 2 1 = rate of change, 0 = static level
6	ROC enable for Alarm 1 1 = rate of change, 0 = static level
5	Not used
4	Comparison data filter setting 1 = filtered data, 0 = unfiltered data
3	Not used
2	Alarm output enable 1 = enabled, 0 = disabled
1	Alarm output polarity 1 = active high, 0 = active low
0	Alarm output line select 1 = DIO2, 0 = DIO1

Table 25. ALM_MAG1, ALM_MAG2

Bits	Description (Default = 0x0000)
15	Comparison polarity 1 = greater than, 0 = less than
14	Not used
[13:0]	Data bits that match the format of the trigger source selection

Table 26. ALM_SMPL1, ALM_SMPL2

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Data bits: number of samples (both 0x00 and 0x01 = 1)

Table 27. Alarm Configuration Example 1

DIN	Description
0xAF55,	ALM_CTRL = 0x5517.
0xAE17	Alarm 1 input = XACCL_OUT. Alarm 2 input = XACCL_OUT. Static level comparison, filtered data. DIO2 output indicator, positive polarity.
0xA783,	ALM_MAG1 = 0x8341.
0xA641	Alarm 1 is true if XACCL_OUT > +0.5 g.
0xA93C,	ALM_MAG2= 0x3CBF.
0xA8BF	Alarm 2 is true if XACCL_OUT < -0.5 g.

Table 28. Alarm Configuration Example 2

DIN	Description
0xAF76,	ALM_CTRL = 0x7687.
0xAE87	Alarm 1 input = ZACCL_OUT. Alarm 2 input = YACCL_OUT. Rate of change comparison, unfiltered data. DIO2 output indicator, positive polarity.
0xB601	SMPL_PRD = 0x0001. Sample rate = 819.2 SPS.
0xAB08	ALM_SMPL1 = 0x0008. Alarm 1 rate of change period = 9.77 ms.
0xAC50	ALM_SMPL2= 0x0050. Alarm 2 rate of change period = 97.7 ms.
0xA783,	ALM_MAG1 = 0x8341.
0xA641	Alarm 1 is true if XACCL_OUT > +0.5 g.
0xA93C,	ALM_MAG2= 0x3CBE.
0xA8BE	Alarm 2 is true if XACCL_OUT < -0.5 g.

OUTLINE DIMENSIONS

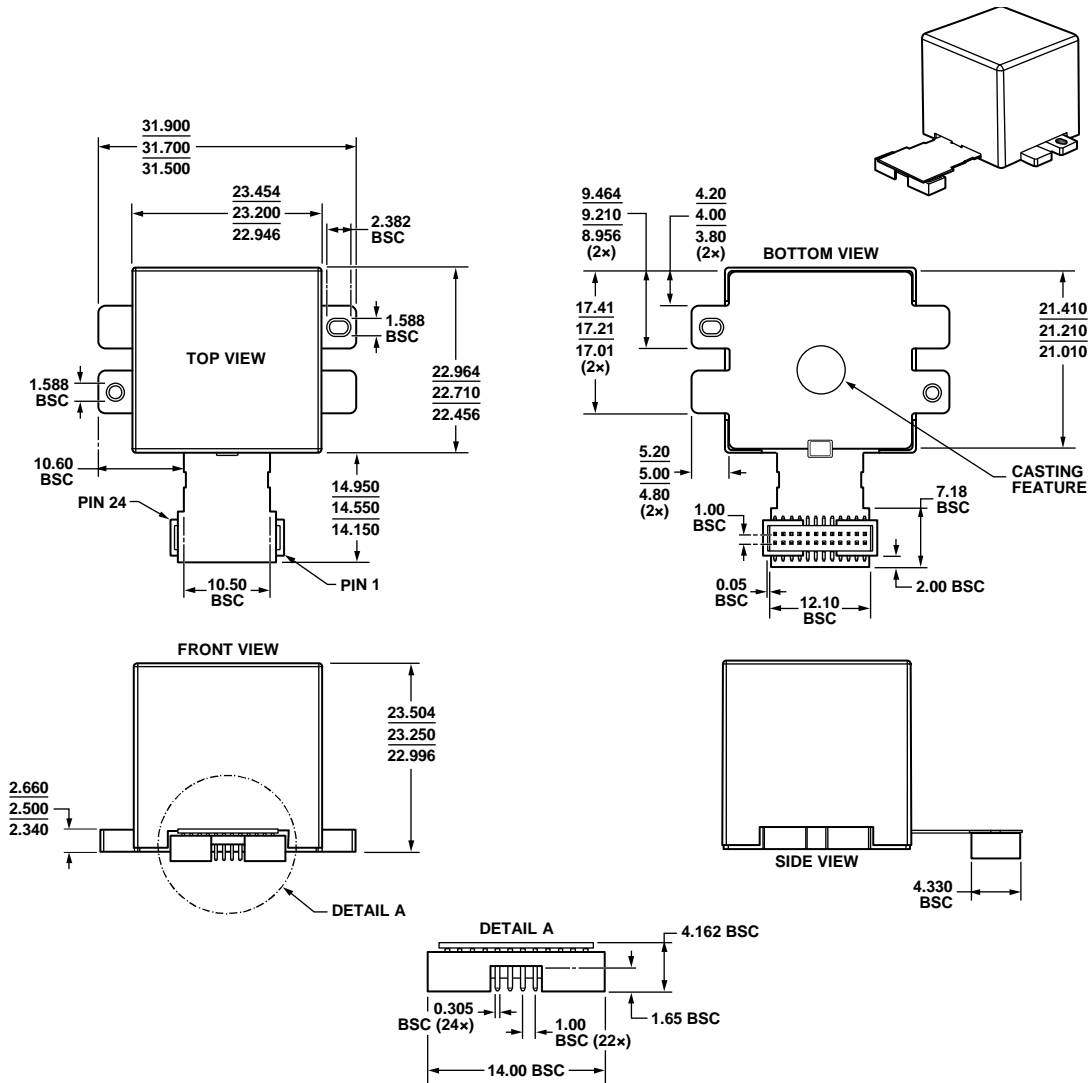


Figure 15. 24-Lead Module with Connector Interface (ML-24-2)
Dimensions shown in millimeters

12-16-2011-C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADIS16405BMLZ	-40°C to +105°C	24-Lead Module with Connector Interface	ML-24-2

¹ Z = RoHS Compliant Part.