Z86E02/E04/E08/E09

General-Purpose OTP MCU with 14 I/O LInes

Product Specification

PS004602-0401

PRELIMINARY

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Architectural Overview

ZiLOG's Z86E02/E04/E08/E09 Microcontrollers (MCU) are One-Time Programmable (OTP) members of ZiLOG's single-chip Z8® MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02/E04/E08/E09's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Z86E02/E04/E08/E09 Features

Table 1. Z86E02/E04/E08/E09 Features

Device	OTP (KB)	RAM* (Bytes)	Speed (MHz)
Z86E02	0.5	125	12
Z86E04	1.0	125	12
Z86E08	2.0	125	12
Z86E09	4.0	125	12

Note: *General-Purpose.

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - RC Oscillator
- Two Programmable 8-Bit Counter/Timers, each with 6-bit Programmable Prescaler
- WDT/ Power-On Reset (POR)

- On-Chip Oscillator that accepts Crystal, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mW typical)
- Fast Instruction Pointer (1 µs @ 12 MHz)
- RAM Bytes (125)

Note: All Signals with an overline, "$\overline{\ }$", are active Low, for example: B/W (WORD is active Low); B/W (BYTE is active Low, only).

Power connections follow conventional descriptions, as noted below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Block Diagrams

Figure 1. Functional Block Diagram

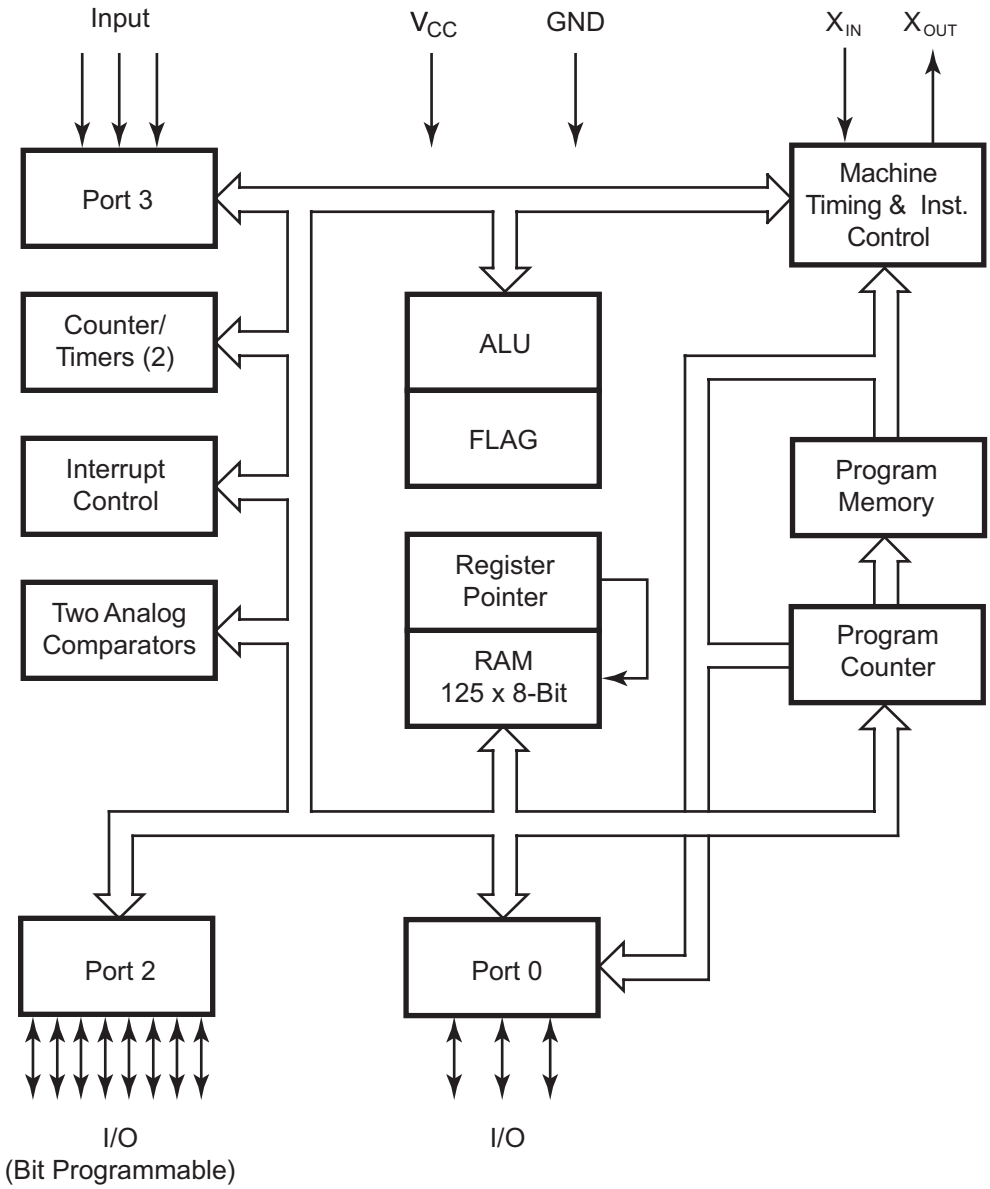
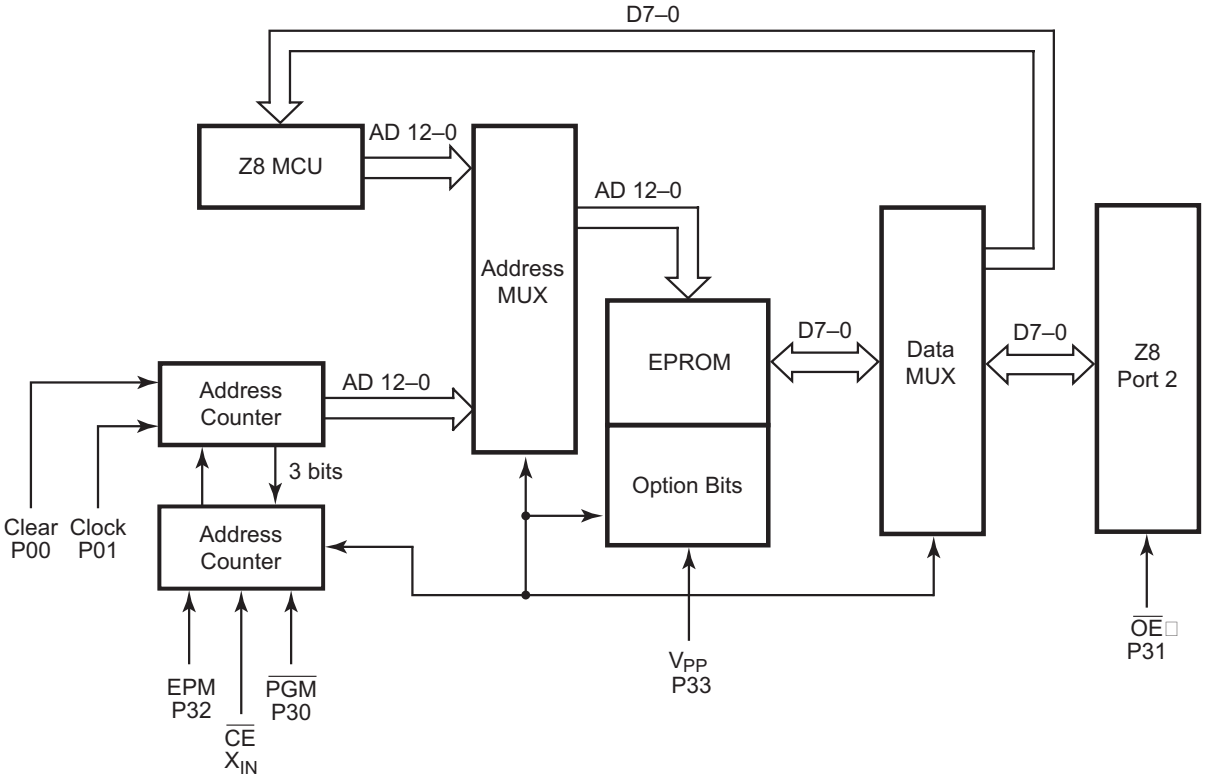


Figure 2. EPROM Programming Mode Block Diagram



Pin Description

Pin diagrams and identification for the device are displayed in Figures 3 and 4, and in Tables 2 and 3.

Figure 3. 18-Pin DIP/SOIC Configuration, STANDARD Mode

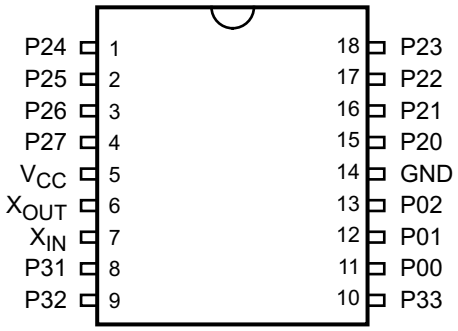


Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1	P24	Port 2, Pin 4	Input/Output
2	P25	Port 2, Pin 5	Input/Output
3	P26	Port 2, Pin 6	Input/Output
4	P27	Port 2, Pin 7	Input/Output
5	V_{CC}	Power Supply	
6	X_{OUT}	Crystal Oscillator Clock	Output
7	X_{IN}	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11	P00	Port 0, Pin 0	Input/Output
12	P01	Port 0, Pin 1	Input/Output
13	P02	Port 0, Pin 2	Input/Output
14	GND	Ground	
15	P20	Port 2, Pin 0	Input/Output

Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode (Continued)

Pin #	Symbol	Function	Direction
16	P21	Port 2, Pin 1	Input/Output
17	P22	Port 2, Pin 2	Input/Output
18	P23	Port 2, Pin 3	Input/Output

Figure 4. 18-Pin DIP/SOIC Configuration, EPROM Mode

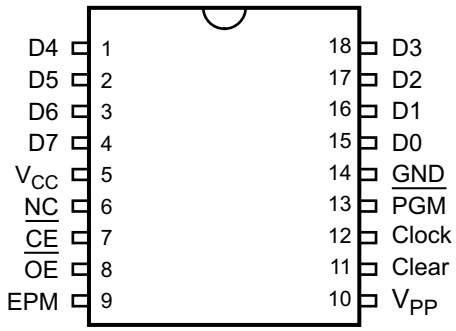


Table 3. 18-Pin DIP/SOIC Pin Identification, EPROM Mode

Pin #	Symbol	Function	Direction
1	D4	Data 4	Input/Output
2	D5	Data 5	Input/Output
3	D6	Data 6	Input/Output
4	D7	Data 7	Input/Output
5	V_{CC}	Power Supply	
6	NC	No Connection	
7	$\overline{CE}$	Chip Enable	Input
8	$\overline{OE}$	Output Enable	Input
9	EPM	EPROM Program Mode	Input
10	V_{PP}	Program Voltage	Input
11	CLEAR	Clear Clock	Input
12	CLOCK	Address	Input
13	$\overline{PGM}$	Program Mode	Input
14	GND	Ground	
15	D0	Data 0	Input/Output
16	D1	Data 1	Input/Output
17	D2	Data 2	Input/Output
18	D3	Data 3	Input/Output

Figure 5. 20-Pin SSOP Pin Configuration, STANDARD Mode

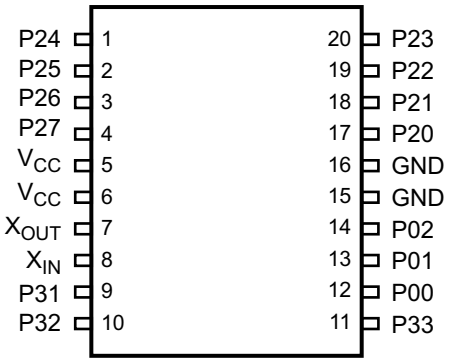


Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1	P24	Port 2, Pin 4	Input/Output
2	P25	Port 2, Pin 5	Input/Output
3	P26	Port 2, Pin 6	Input/Output
4	P27	Port 2, Pin 7	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	X_{OUT}	Crystal Oscillator Clock	Output
8	X_{IN}	Crystal Oscillator Clock	Input
9	P31	Port 3, Pin 1, AN1	Input
10	P32	Port 3, Pin 2, AN2	Input
11	P33	Port 3, Pin 3, REF	Input
12	P00	Port 0, Pin 0	Input/Output
13	P01	Port 0, Pin 1	Input/Output
14	P02	Port 0, Pin 2	Input/Output
15	GND	Ground	
16	GND	Ground	
17	P20	Port 2, Pin 0	Input/Output

Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
18	P21	Port 2, Pin 1	Input/Output
19	P22	Port 2, Pin 2	Input/Output
20	P23	Port 2, Pin 3	Input/Output

Figure 6. 20-Pin SSOP Pin Configuration, EPROM Mode

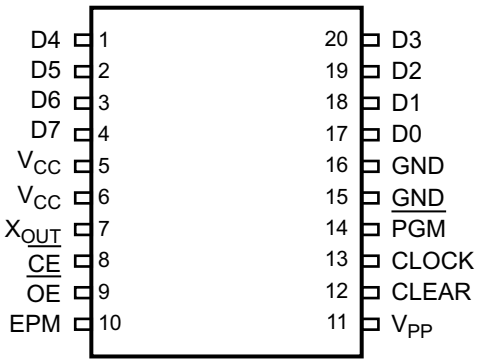


Table 5. 18-Pin DIP/SOIC Pin Identification, EPROM Mode

Pin #	Symbol	Function	Direction
1	D4	Data 4	Input/Output
2	D5	Data 5	Input/Output
3	D6	Data 6	Input/Output
4	D7	Data 7	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	X_{OUT}	Crystal Oscillator Clock	Output
8	$\overline{CE}$	Chip Enable	Input
9	$\overline{OE}$	Output Enable	Input
10	EPM	EPROM Program Mode	Input
11	V_{PP}	Program Voltage	Input
12	CLEAR	Clear Clock	Input
13	CLOCK	Address	Input
14	$\overline{PGM}$	Program Mode	Input
15	GND	Ground	
16	GND	Ground	
17	D0	Data 1	Input/Output
18	D1	Data 0	Input/Output

Table 5. 18-Pin DIP/SOIC Pin Identification, EPROM Mode

Pin #	Symbol	Function	Direction
19	D2	Data 2	Input/Output
20	D3	Data 3	Input/Output

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. See Table 6. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

Table 6. Absolute Maximum Ratings

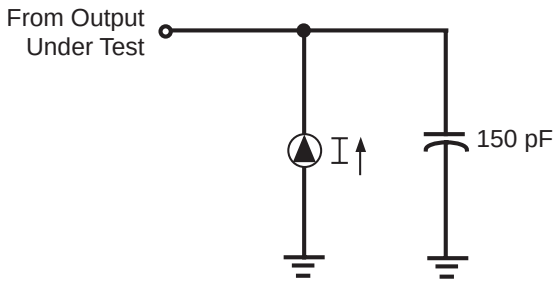
Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Total Power Dissipation		1.65	W	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		220	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	2
Maximum Allowable Output Current Sinked by any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by any I/O Pin		25	mA	
Total Maximum Output Current Sinked by a Port		60	mA	
Total Maximum Output Current Sourced by a Port		45	mA	

Notes:
1. Applies to all pins except where otherwise noted. Maximum current into or out of pin must be ± 600 µA.
2. Device pin is not at an output Low state.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin See Figure 7.

Figure 7. Test Load Diagram



Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND. See Table 7.

Table 7. Capacitance

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC Electrical Characteristics

Standard Temperature Range

Table 8 provides Direct Current characteristics for the Z86E02/E04/E08/E09 microcontroller, at a standard ambient temperature range of 0ºC to 70ºC.

Table 8. DC Characteristics, Standard Temperature Range

			T_A = 0°C to +70°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
V_{INMAX}	Max Input Voltage	3.0V	–12	12		V	I_{IN} < 250 µA	2
		5.5V	–12	12		V	I_{IN} < 250 mA	2
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
		3.0V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 8. DC Characteristics, Standard Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
V_{OL1}	Output Low Voltage	3.0V		0.8	0.1	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		3.0V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	3.0V		0.8	0.8	V	I_{OL} = +12 mA,	3
		5.5V		0.8	0.8	V	I_{OL} = +12 mA,	3
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.2	3.0	2.8	V	@ 6 MHz Maximum Internal Clock Frequency	4
					2.2	V		5
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} – 1.0		V		

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 8. DC Characteristics, Standard Temperature Range (Continued)

			T_A = 0°C to +70°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	3,6
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	3,6
		3.0V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	3,6
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	3,6
		3.0V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	3,6
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	3,6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 8. DC Characteristics, Standard Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC1}	Standby Current	3.0V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	3,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	3,6
		3.0V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	3,6
		5.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	3,6
		3.0V		7.0	4.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	3,6
		5.5V		7.0	4.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	3,6
I_{CC}	Supply Current (LOW NOISE mode)	3.0V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	6
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	6
		3.0V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	6
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	6
		3.0V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	6
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 8. DC Characteristics, Standard Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC1}	Standby Current (LOW NOISE mode)	3.0V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	6
		3.0V		3.0	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	6
		5.5V		3.0	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	6
		3.0V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	6
		5.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	6
I_{CC2}	Standby Current	3.0V		10.0	1.0	µA	STOP mode V_{IN} = 0V, V_{CC}; WDT is not Running	6,7,8
		5.5V		10.0	1.0	µA	STOP mode V_{IN} = 0V,V_{CC}; WDT is not Running	6,7,8
I_{ALL}	Auto Latch Low Current	3.0V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.0V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Extended Temperature Range

Table 9 provides Direct Current characteristics for the Z86E02/E04/E08/E09 microcontroller, at an extended ambient temperature range of –40ºC to 105ºC.

Table 9. DC Characteristics, Extended Temperature Range

			T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
V_{INMAX}	Max Input Voltage	4.5V		12.0		V	I_{IN} < 250 µA	2
		5.5V		12.0		V	I_{IN} < 250 µA	2
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
		4.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 9. DC Characteristics, Extended Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +105°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		4.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I_{OL} = +12 mA	3
		5.5V		1.0	0.3	V	I_{OL} = +12 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Maximum Internal Clock Frequency	4
					2.2	V		5
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} – 1.5		V		

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	3,6
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	3,6
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	3,6
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	3,6
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	3,6
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	3,6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 9. DC Characteristics, Extended Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +105°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	3,6
		5.5V		5.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	3,6
		4.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	3,6
		5.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	3,6
		4.5V		7.0	4.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	3,6
		5.5V		7.0	4.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	3,6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current (LOW NOISE mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	6
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	6
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	6
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	6
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	6
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

Table 9. DC Characteristics, Extended Temperature Range (Continued)

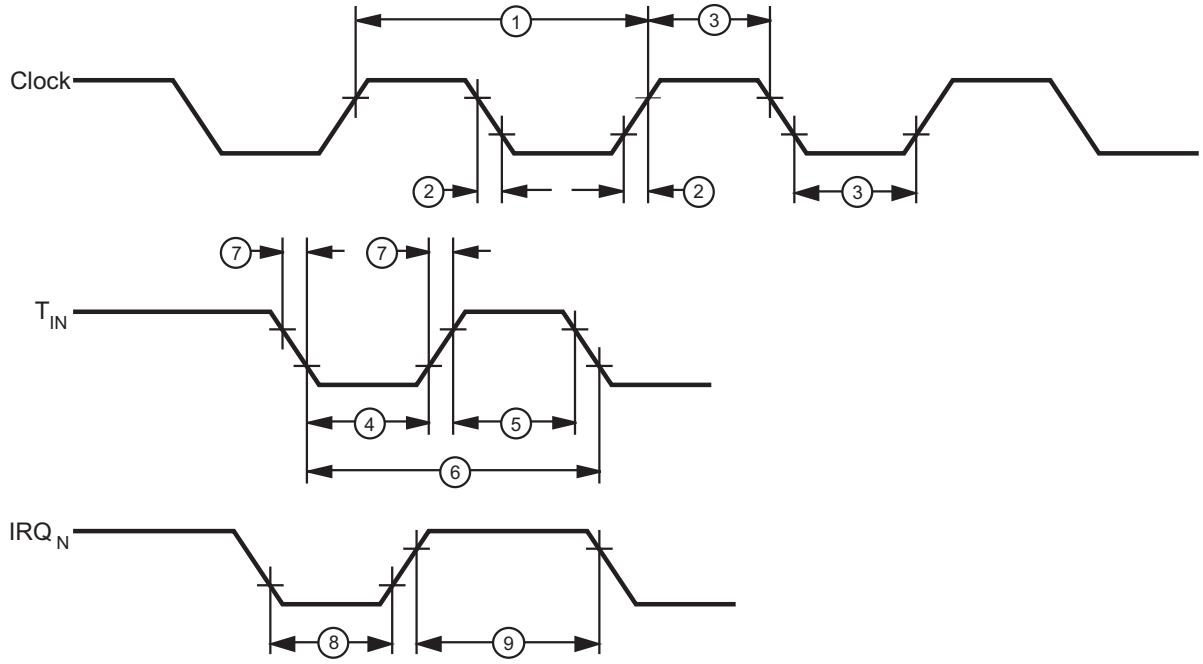
Sym	Parameter	V_{CC}	T_A = –40°C to +105°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC1}	Standby Current (LOW NOISE mode)	4.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	6
		4.5V		3.0	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	6
		5.5V		3.0	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	6
		4.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	6
		5.5V		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	6
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC}; WDT is not Running	6,7,8
		5.5V		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC}; WDT is not Running	6,7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not LOW EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the X_{IN} pin to the V_{CC} pin.

AC Electrical Timing Characteristics

Figure 8 illustrates Alternating Current timing for the Z86E02/E04/E08/E09 microcontroller.

Figure 8. AC Electrical Timing



STANDARD Mode at Standard Temperature

Table 10 describes timing characteristics in STANDARD mode at standard temperature for the timing diagram noted in Figure 8.

Table 10. AC Electrical Characteristics—STANDARD Mode and Temperature

				T_A = 0ºC to +70ºC						
				8MHz		12MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.0V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.0V		25		15	ns	1
			5.5V		25		15	ns	1
3	T_WC	Input Clock Width	3.0V	62		41		ns	1
			5.5V	62		41		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	$5T_PC$		$5T_PC$			1
			5.5V	$5T_PC$		$5T_PC$			1
6	T_PT_{IN}	Timer Input Period	3.0V		$8T_PC$	$8T_PC$			1
			5.5V		$8T_PC$	$8T_PC$			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.0V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.0V		$5T_PC$	$5T_PC$			1,2
			5.5V		$5T_PC$	$5T_PC$			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.0V	12		12		ms	1,3
			5.5V	12		12		ms	1,3
11	T_{POR}	Power-On Reset Time	3.0V	2	25	2	25	ms	1,4
			5.5V	2	25	2	25	ms	1,4

Notes:
1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

STANDARD Mode at Extended Temperature

Table 11 describes timing characteristics in STANDARD mode at extended temperature for the timing diagram noted in Figure 8.

Table 11. AC Electrical Timing—STANDARD Mode at Extended Temperature

				T_A = –40ºC to +105ºC					
				8MHz		12MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.0V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.0V		25		15	ns	1
			5.5V		25		15	ns	1
3	T_WC	Input Clock Width	3.0V		62		41	ns	1
			5.5V		62		41	ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.0V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	$5T_PC$		$5T_PC$			1
			5.5V	$5T_PC$		$5T_PC$			1
6	T_PT_{IN}	Timer Input Period	3.0V	$8T_PC$		$8T_PC$			1
			5.5V	$8T_PC$		$8T_PC$			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.0V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.0V	$5T_PC$		$5T_PC$			1,2
			5.5V	$5T_PC$		$5T_PC$			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.0V	12		12		ms	1,3
			5.5V	12		12		ms	1,3

Notes:
1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

Table 11. AC Electrical Timing—STANDARD Mode at Extended Temperature (Continued)

				T_A = –40ºC to +105ºC						
				8MHz		12MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	3.0V	2	25	2	25	ms	1,4
			5.5V	2	25	2	25	ms	1,4

Notes:
1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

LOW NOISE Mode at Standard Temperature

Table 12 describes timing characteristics in LOW NOISE mode at standard temperature for the timing diagram noted in Figure 8.

Table 12. AC Electrical Timing—LOW NOISE Mode at Standard Temperature

				T_A = 0ºC to +70ºC						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.0V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC, T_FC	Clock Input Rise and Fall Times	3.0V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.0V	500		125		ns	1
			5.5V	500		125		ns	1
4.	$T_WT_{IN}L$	Timer Input Low Width	3.0V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1

Notes:
1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

Table 12. AC Electrical Timing—LOW NOISE Mode at Standard Temperature (Continued)

				T_A = 0ºC to +70ºC						
				1MHz		4MHz			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
6	T_PT_{IN}	Timer Input Period	3.0V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL Low Time	Interrupt Request Input	3.0V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH High Time	Interrupt Request Input	3.0V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time for Time-out	3.0V	12		12		ms	1,3
			5.5V	12		12		ms	1,3
11	T_{POR}	Power-On Reset Time	3.0V	2	25	2	25	ms	1,4
			5.5V	2	25	2	25	ms	1,4

Notes:
1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

LOW NOISE Mode at Extended Temperature

Table 13 describes timing characteristics in LOW NOISE mode at extended temperature for the timing diagram noted in Figure 8.

Table 13. AC Electrical Timing—LOW NOISE Mode at Extended Temperature

				T_A = –40ºC to +105ºC						
				1 MHz		4 MHz				
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC, T_FC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	$2.5T_PC$		$2.5T_PC$			1
			5.5V	$2.5T_PC$		$2.5T_PC$			1
6	T_PT_{IN}	Timer Input Period	4.5V		$4T_PC$	$4T_PC$			1
			5.5V		$4T_PC$	$4T_PC$			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL Low Time	Interrupt Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH High Time	Interrupt Request Input High Time	4.5V	$2.5T_PC$		$2.5T_PC$			1,2
			5.5V	$2.5T_PC$		$2.5T_PC$			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time for Time-out	4.5V	12		12		ms	1,3
			5.5V	12		12		ms	1,3

Notes:
1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

Table 13. AC Electrical Timing—LOW NOISE Mode at Extended Temperature (Continued)

				T_A = –40ºC to +105ºC						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	4.5V	2	25	2	25	ms	1,4
			5.5V	2	25	2	25	ms	1,4

Notes:
1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 55msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 7msec @ 5.0V and 25ºC.

Low-Noise Version

Low-EMI Emission

The device can be programmed to operate in a LOW EMI EMISSION mode by means of an OTP bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical
- Internal SCLK and TCLK operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 500Ω
- Oscillator divide-by-two circuitry eliminated

The LOW EMI mode is an OPT option bit that can be selected by the customer at the time the ROM code is programmed into the OTP EPROM. The default condition is a disabled LOW EMI mode.

Pin Functions

EPROM Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during all EPROM operations (PROGRAM, PROGRAM VERIFY, etc.).

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM READ mode, PROGRAM mode, and PROGRAM VERIFY mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the data bus is output. When High, the data bus is input.

EPM EPROM Program Mode. This pin controls the selection of EPROM operation modes.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear (active High). This pin resets the internal address counter at the High level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one count with one clock cycle.

$\overline{PGM}$ Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the data bus.

Pin Function Changes in EPROM Mode

With the exception of V_{CC} and GND, the Z8 changes all of its pin functions in EPROM mode. X_{OUT} offers no function; X_{IN} functions as CE, P31 functions as OE, P32 functions as EPM, P33 functions as V_{PP}, P00 functions as CLEAR, P01 functions as CLOCK, and P02 functions as PGM. Please refer to the Programming Specification for additional EPROM mode descriptions.

STANDARD Mode

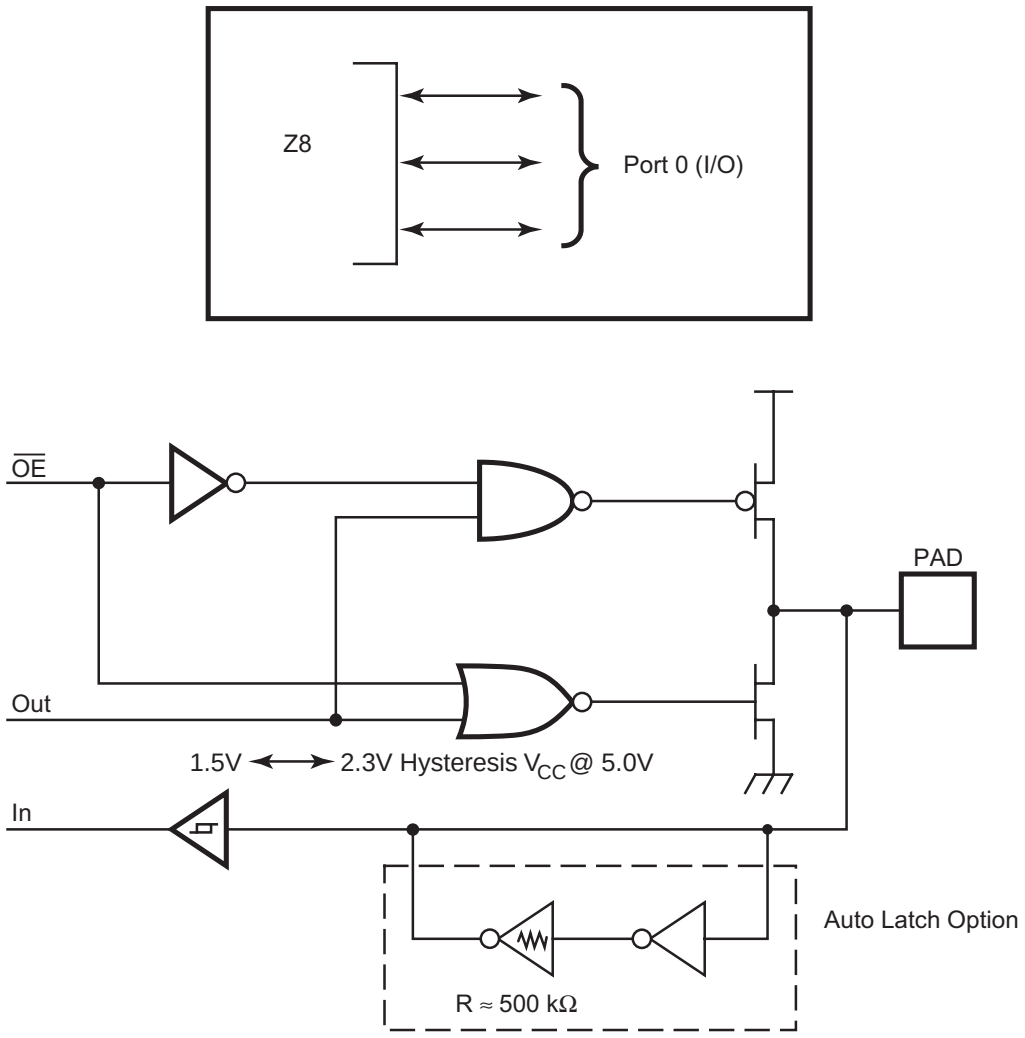
X_{IN}, X_{OUT}. *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 9).

Auto Latch. The Auto Latch places valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather

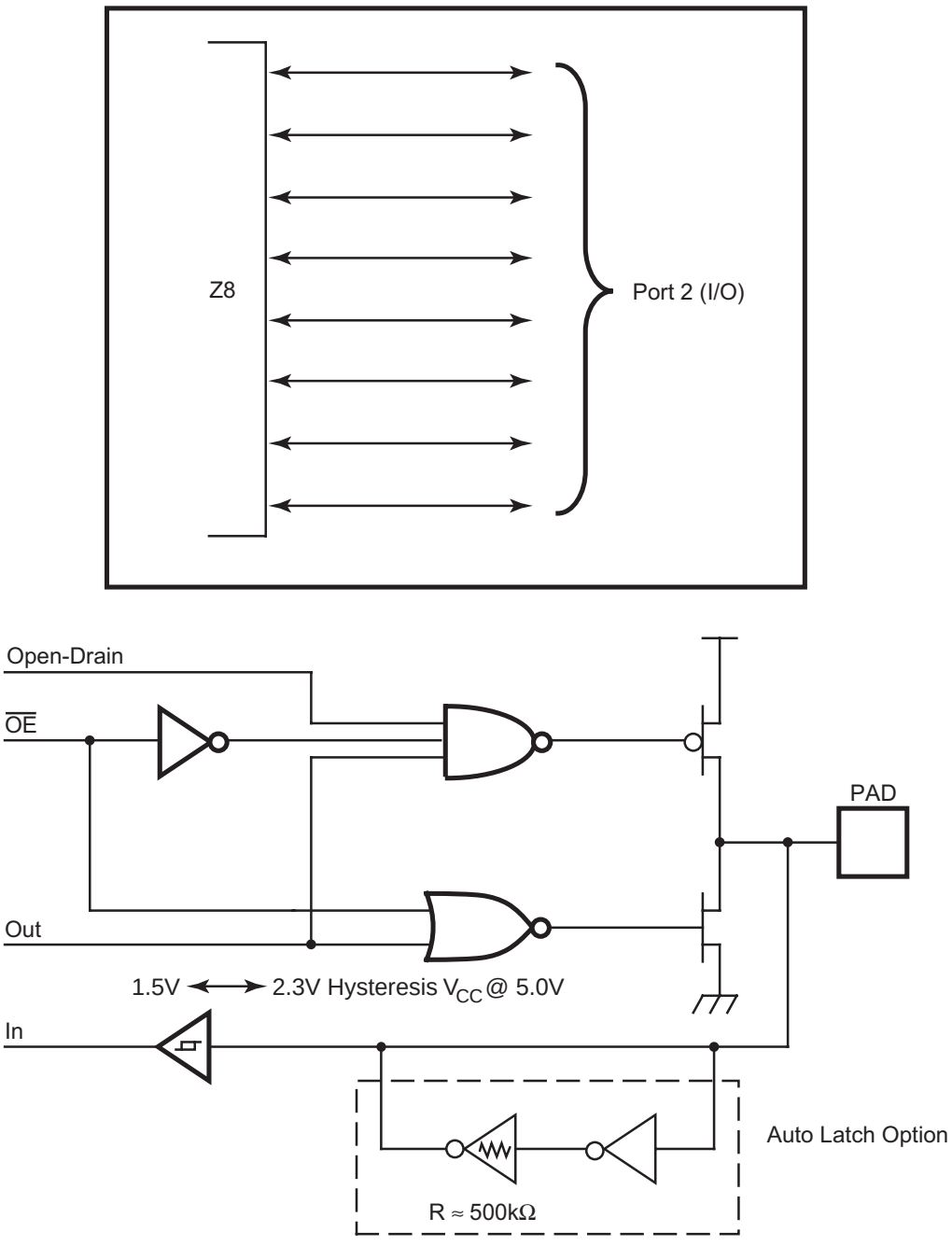
than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch sets the ports to an undetermined state of 0 or 1. The default condition is AUTO LATCHES ENABLED. The Auto Latch can be disabled by programming the AUTO LATCH DISABLE option bit.

Figure 9. Port 0 Configuration



Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).

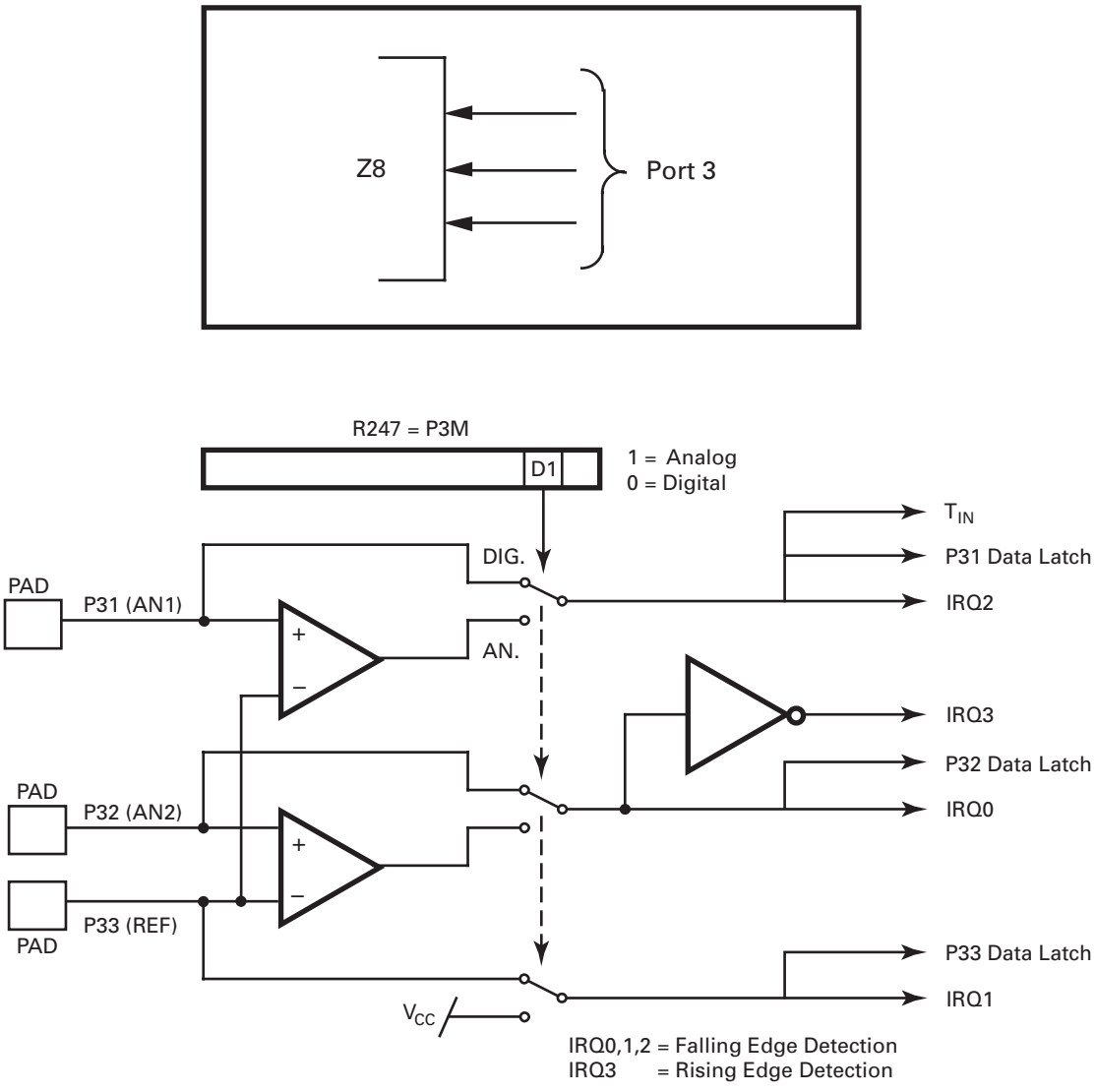
Figure 10. Port 2 Configuration



Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 11).

Figure 11. Port 3 Configuration



Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; zero-crossing detection, A/D conversion, voltage scaling, and threshold detection. In ANALOG mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

The comparator requires two NOPs to be stable after setting its enable bit. ZiLOG recommends that interrupts IRQ0, IRQ1, and IRQ2 be disabled before setting the enable bit. After enabling the comparator, IRQ0, IRQ1, and IRQ2 should be cleared prior to reenabling these interrupts. ZiLOG also recommends clearing these interrupts when disabling the comparator.

Functional Description

The following special functions are incorporated into the Z8 devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000Ch (Figure 12). The Z8 control registers' reset value is indicated in Table 14.

Figure 12. Internal Reset Configuration

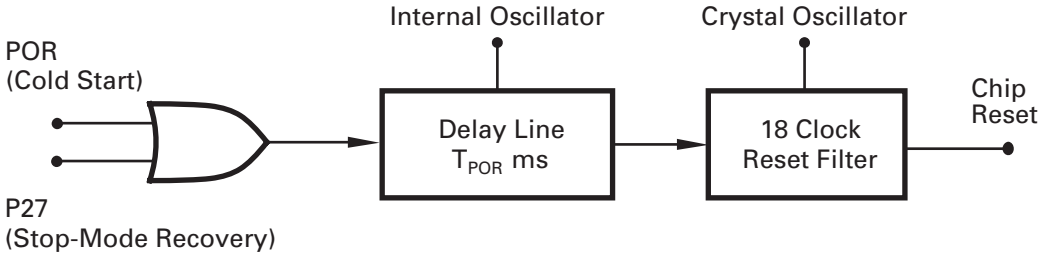


Table 14. Z8 Control Registers Reset Values*

		Reset Condition								
Address	**Register**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FFh	SPL	0	0	0	0	0	0	0	0	
FDh	RP	0	0	0	0	0	0	0	0	
FCh	FLAGS	U	U	U	U	U	U	U	U	

Note: *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 14 and the user must avoid bus contention on the port pins or it may affect device reliability.

Table 14. Z8 Control Registers Reset Values* (Continued)

		Reset Condition								
Address	**Register**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FBh	IMR	0	U	U	U	U	U	U	U	
FAh	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9h	IPR	U	U	U	U	U	U	U	U	
F8h*	P01M	U	U	U	0	U	U	0	1	
F7h*	P3M	U	U	U	U	U	U	0	0	
F6h*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5h	PRE0	U	U	U	U	U	U	U	0	
F4h	T0	U	U	U	U	U	U	U	U	
F3h	PRE1	U	U	U	U	U	U	0	0	
F2h	T1	U	U	U	U	U	U	U	U	
F1h	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 14 and the user must avoid bus contention on the port pins or it may affect device reliability.

A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

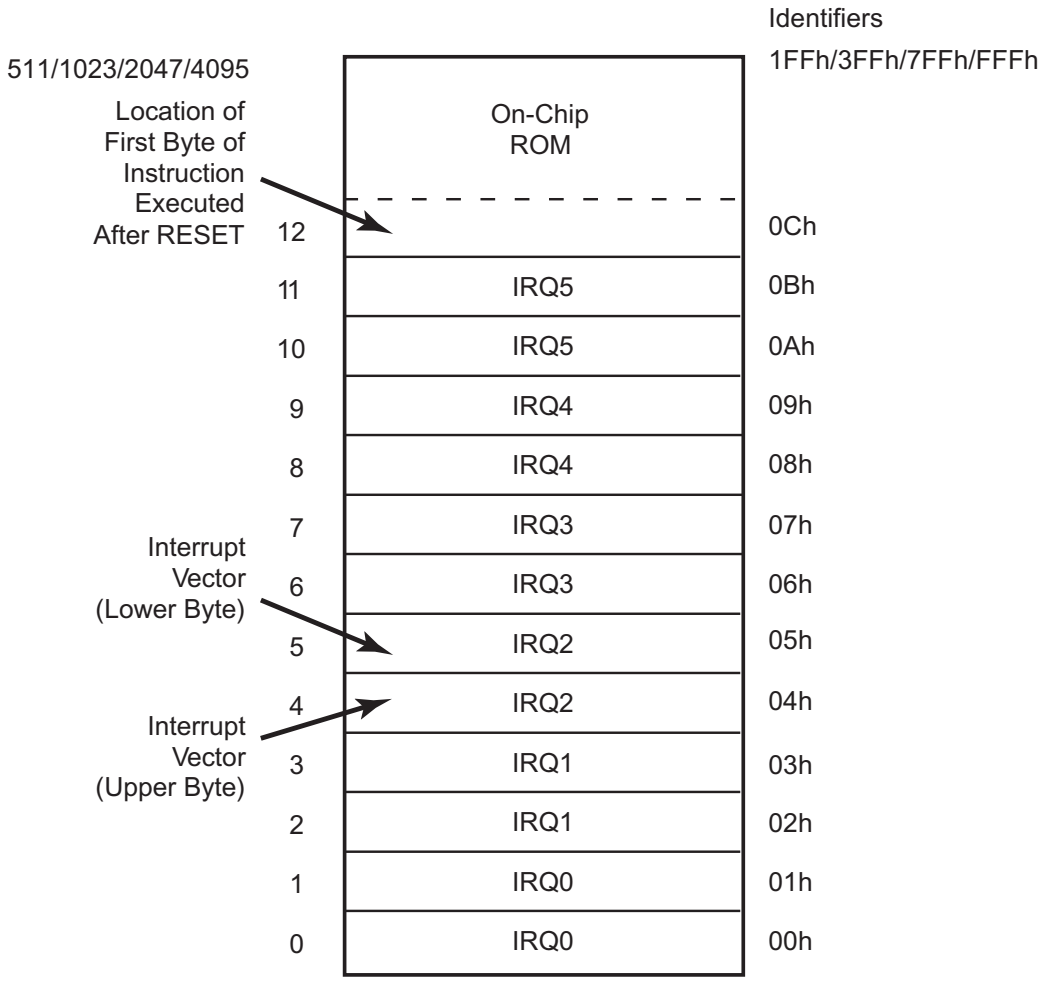
Watch-Dog Timer Reset

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Program Memory

The Z86E02/E04/E08/E09 addresses up to 0.5/1.0/2.0/4.0 kHz of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–511/1023/2047/4095 are on-chip one-time programmable ROM.

Figure 13. Program Memory Map



Register File

The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255,

respectively (Figure 14). General-purpose registers occupy the 04h to 7Fh address space. I/O ports are mapped as per the existing CMOS Z8.

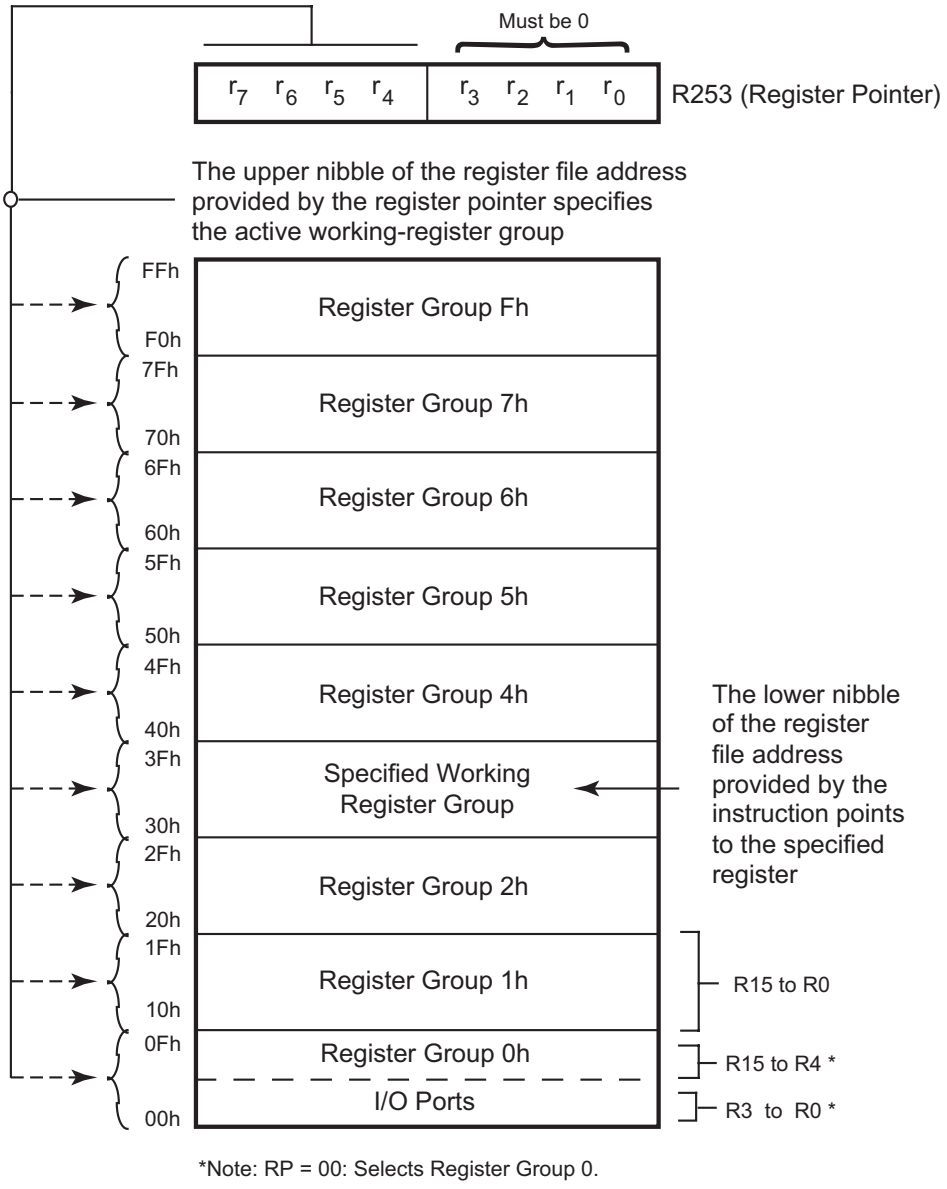
Figure 14. Register File

Location		Identifiers
255 (FFh)	Stack Pointer (Bits 7-0)	SPL
254 (FEh)	General-Purpose Register	GPR
253 (FDh)	Register Pointer	RP
252 (FCh)	Program Control Flags	FLAGS
251 (FBh)	Interrupt Mask Register	IMR
250 (FAh)	Interrupt Request Register	IRQ
249 (F9h)	Interrupt Priority Register	IPR
248 (F8h)	Ports 0–1 Mode	P01M
247 (F7h)	Port 3 Mode	P3M
246 (F6h)	Port 2 Mode	P2M
245 (F5h)	T0 Prescaler	PRE0
244 (F4h)	Timer/Counter0	T0
243 (F3h)	T1 Prescaler	PRE1
242 (F2h)	Timer/Counter1	T1
241 (F1h)	Timer Mode	TMR
240 (F0h) 128 (80h)	Not Implemented	
127 (7Fh) • • • 4 (04h)	General-Purpose Registers	
3 (03h)	Port 3	P3
2 (02h)	Port 2	P2
1 (01h)	Reserved	P1
0 (00h)	Port 0	P0

The Z8 instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing short 4-bit register addressing mode using the Register Pointer.

In the 4-bit address mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 15) addresses the starting location of the active working-register group.

Figure 15. Register Pointer



*Note: RP = 00: Selects Register Group 0.

Stack Pointer

The Z8 features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 120 general-purpose registers from 04h to 7Fh.

General-Purpose Registers (GPR)

These registers are undefined after the device is powered up. The registers keep their most recent value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range.

Note: Register R254 is designated as a general-purpose register and is set to 00h after any reset or Stop-Mode Recovery.

Counter/Timer

There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 16).

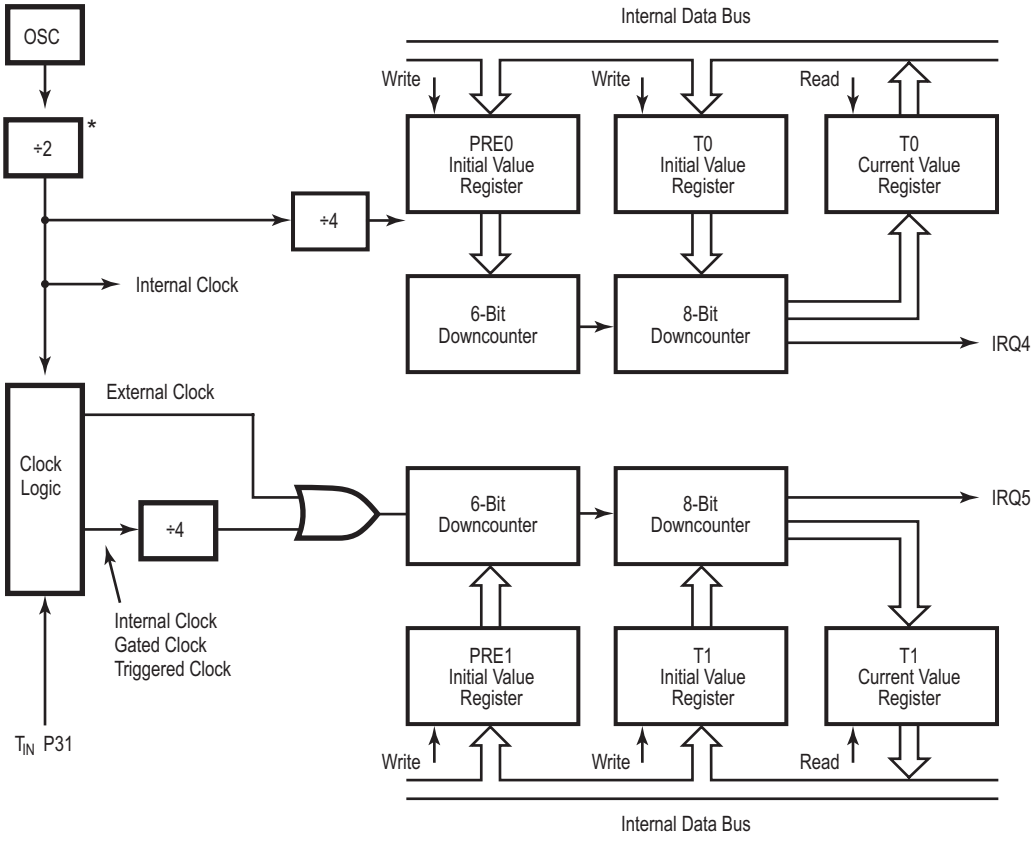
The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The TIMER mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or used as a gate input for the internal clock.

Note: This step is bypassed if LOW EMI mode is selected.

Figure 16. Counter/Timers Block Diagram



Interrupts

The Z8 features six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 15).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

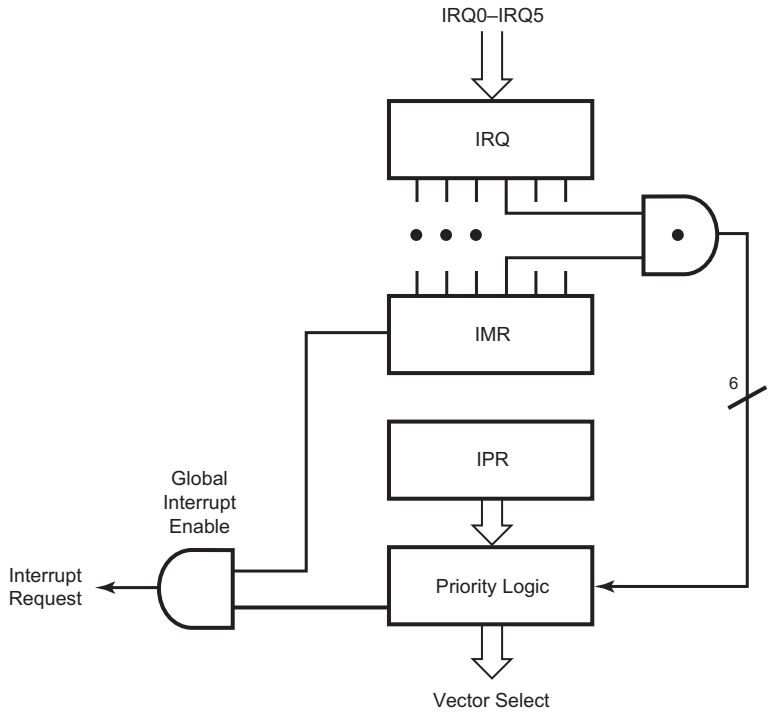
Note: The user must select any Z86E08 mode in ZiLOG's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1(P31)	4,5	External (F) Edge
IRQ3	AN2(P32)	6,7	External (R) Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Note: F = Falling edge triggered; R = Rising edge triggered.

Figure 17. Interrupt Block Diagram



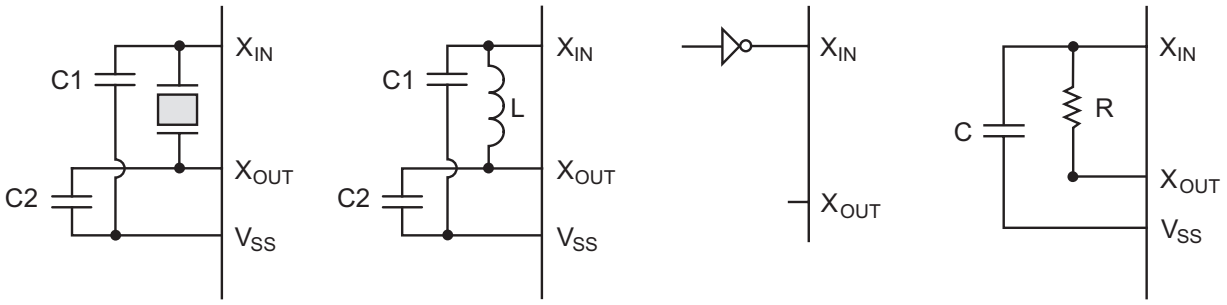
Clock

The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across X_{IN} and X_{OUT} using the vendor's crystal recommended capacitor values from each pin directly to device ground pin 14 (Figure 18).

Note: The crystal capacitor loads should be connected directly to the V_{SS} pin to reduce Ground noise injection. They should not connect to system Ground.

Figure 18. Oscillator Configuration



Ceramic Resonator or Crystal | LC Clock | External Clock | RC Clock

Table 16. Typical Frequency vs. RC Values—V_{CC} = 5.0 V @ 25°C

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
1.0 MΩ	33 kHz	31 kHz	20 kHz	20 kHz	12 kHz	11 kHz	1.4 kHz	1.4 kHz
560 KΩ	56 kHz	52 kHz	34 kHz	32 kHz	20 kHz	19 kHz	2.5 kHz	2.4 kHz
220 KΩ	144 kHz	130 kHz	84 kHz	78 kHz	48 kHz	45 kHz	6 kHz	6 kHz
100 KΩ	315 kHz	270 kHz	182 kHz	164 kHz	100 kHz	95 kHz	12 kHz	12 kHz

Notes:
A = STANDARD mode frequency.
B = LOW EMI mode frequency.

Table 16. Typical Frequency vs. RC Values—V_{CC} = 5.0 V @ 25°C (Continued)

	Load Capacitor							
56KΩ	552kHz	480kHz	330kHz	300kHz	185kHz	170kHz	23kHz	22kHz
20KΩ	1.4MHz	1MHz	884kHz	740kHz	500kHz	450kHz	65kHz	61kHz
10KΩ	2.6MHz	2MHz	1.6MHz	1.3MHz	980kHz	820kHz	130kHz	123kHz
5KΩ	4.4MHz	3MHz	2.8MHz	2MHz	1.7MHz	1.3MHz	245kHz	225kHz
2KΩ	8MHz	5MHz	6MHz	4MHz	3.8MHz	2.7MHz	600kHz	536kHz
1KΩ	12MHz	7MHz	8.8MHz	6MHz	6.3MHz	4.2MHz	1.0MHz	950kHz

Notes:
A = STANDARD mode frequency.
B = LOW EMI mode frequency.

Table 17. Typical Frequency vs. RC Values—V_{CC} = 3.3 V @ 25°C

Resistor (R)	Load Capacitor							
	33 pF		56 pF		100 pF		0.00 1µF	
	A	B	A	B	A	B	A	B
1.0MΩ	18kHz	18kHz	12kHz	12kHz	7.4kHz	7.7kHz	1kHz	1kHz
560KΩ	30kHz	30kHz	20kHz	20kHz	12kHz	12kHz	1.6kHz	1.6kHz
220KΩ	70kHz	70kHz	47kHz	47kHz	30kHz	30kHz	4kHz	4kHz
100KΩ	150kHz	148kHz	97kHz	96kHz	60kHz	60kHz	8kHz	8kHz
56KΩ	268kHz	250kHz	176kHz	170kHz	100kHz	100kHz	15kHz	15kHz
20KΩ	690MHz	600kHz	463kHz	416kHz	286kHz	266kHz	40kHz	40kHz
10KΩ	1.2MHz	1MHz	860kHz	730kHz	540kHz	480kHz	80kHz	76kHz
5KΩ	2MHz	1.7MHz	1.5MHz	1.2MHz	950kHz	820kHz	151kHz	138kHz
2KΩ	4.6MHz	3MHz	3.3MHz	2.4MHz	2.2MHz	1.6MHz	360kHz	316kHz
1KΩ	7MHz	4.6MHz	5MHz	3.6MHz	3.6MHz	2.6MHz	660kHz	565kHz

Notes:
A = STANDARD mode frequency.
B = LOW EMI MODE frequency.

HALT Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active.

The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT mode.

STOP Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A LOW INPUT condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release STOP mode, the I/O port mode registers are not reconfigured to their default POWER-ON conditions. Thus the I/O, configured as output when the STOP instruction was executed, is prevented from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

LD	P2M, #1XXX XXXXB
NOP	
STOP	

Note: X = Dependent on user's application.

Note: A Low level detected on pin P27 takes the device out of STOP mode, even if it is configured as an output.

To enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

FFh	NOP	; clear the pipeline
6Fh	STOP	; enter STOP mode
	or	
FFh	NOP	; clear the pipeline
7Fh	HALT	; enter HALT mode

Note: On the CCP emulator, a software workaround must be used to enable P27 as the Stop-Mode Recovery source.

Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 T_{WDT} period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

Op Code WDT (5Fh)

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 crystal clock cycles. The software enabled WDT does not run in STOP mode.

Op Code WDH (4Fh)

When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters—it just makes it possible to operate the WDT during HALT mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

Permanent WDT

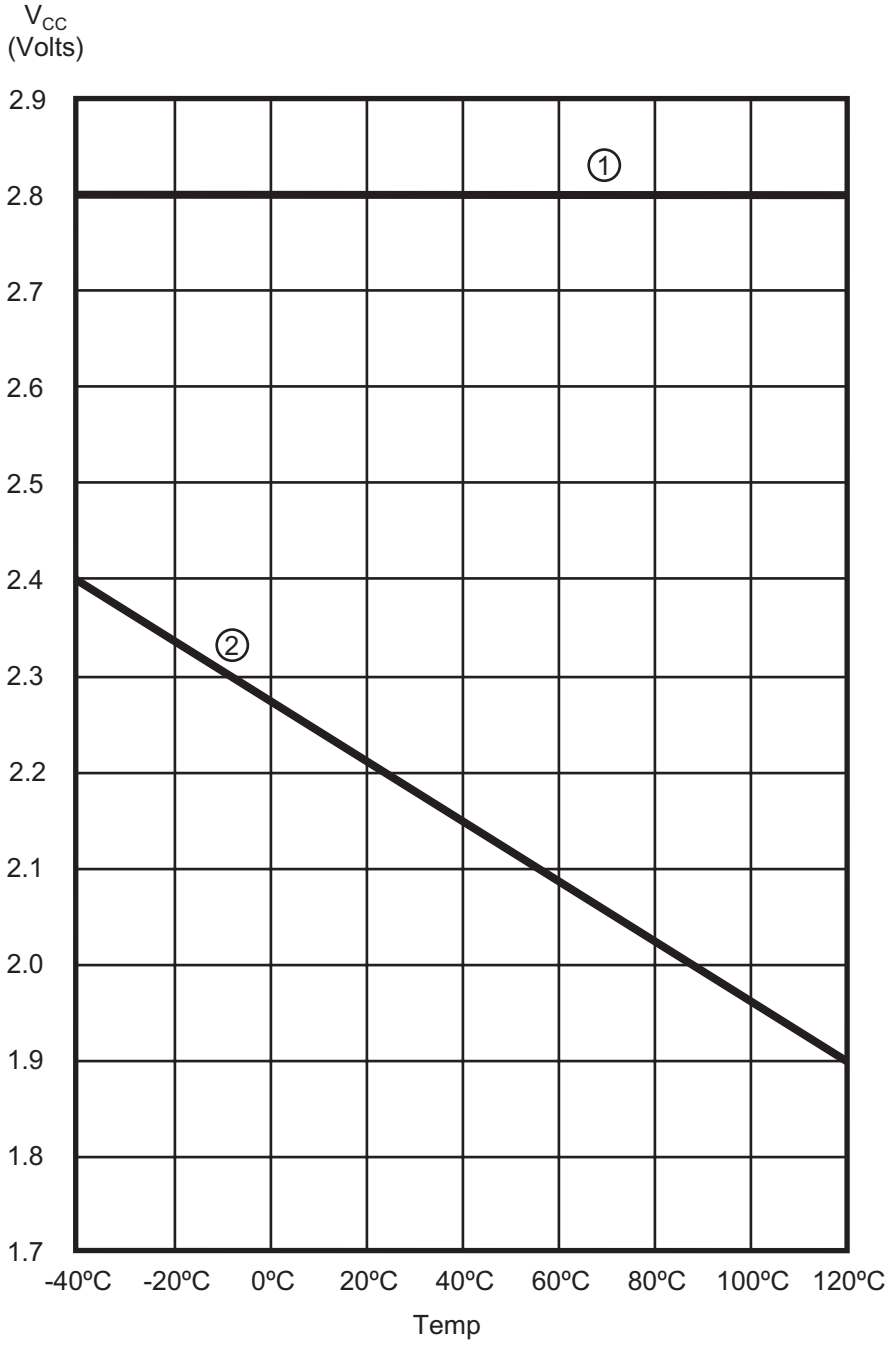
Selecting the hardware-enabled Permanent WDT option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in HALT mode and STOP mode, and it cannot be disabled.

Note: On the CCP emulator, a software workaround must be used to enable the software- or hardware-enabled WDT.

Auto Reset Voltage (V_{LV})

The Z8 features an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}. Figure 19 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the V_{CC} operating voltage range, the Z8 functions down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

Figure 19. Typical Auto Reset Voltage (V_{LV}) vs. Temperature



Note: (1) applies to V_{LV} in RUN and HALT modes. (2) applies to V_{LV} in STOP mode.

OTP Option Bit Description

One-Time Programmable EPROM option bits for the device are described in this section.

Low-EMI Emission. The Z8 can be programmed to operate in a low-EMI emission (low-noise) mode by means of an EPROM programmable bit option. Use of this feature results in:

- All drivers slew rates are typically reduced to 10ns
- Internal SCLK and TCLK = crystal operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 500 ohms
- Oscillator divide-by-two circuitry eliminated

RC Oscillator. The RC Oscillator option bit, when programmed, enables the internal RC oscillator to connect to the X_{OUT} and X_{IN} pins while disabling the internal crystal oscillator to X_{OUT} and X_{IN}.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI *are supported* (Z86E02/E04/E08/E09 and Z86C02/C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low-Noise feature is not automatically enabled.

Auto Latch Disable. Auto Latch Disable option bit, when programmed, globally disables all Auto Latches.

Permanent WDT Enable. The hardware-enabled permanent WDT Enable option bit, when programmed, enables the WDT permanently after exiting reset. Unlike software-enabled WDT, the hardware-enabled permanent WDT cannot be stopped in HALT or STOP modes.

32-kHz Enable. The 32-kHz Enable option bit enables the 32-kHz oscillator circuit and disables the high-frequency crystal oscillator circuit. This option bit is disabled if the RC oscillator option bit is programmed.

Control Registers

Table 18.Timer Mode Register—R241 TMR F1h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
7–6	Reserved	R/W	00	**Reserved—must be 0**
5–4	T_{IN} Mode	R/W	00	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (nonretriggerable) 11: Trigger Input (retriggerable)
3	T1 Count	R/W	0	**T1 Count** 0: Disable 1: Enable
2	T1	R/W	0	**T1** 0: No Function 1: Load T1
1	T0 Count	R/W	0	**T0 Count** 0: Disable 1: Enable
0	T0	R/W	0	**T0** 0: No Function 1: Load T0

Table 19.Counter/Timer 1 Register—R242 T1 F2h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

Note: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–0	T1	R	X	T1 Current Value
		W	X	T1 Initial Value Range = 1–256 decimal; 01h–00h

Table 20.Prescaler 1 Register—R243 PRE1 F3h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0

Note: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 00h–01h
1	Clock	W	0	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode 1: T1 Internal
0	Count	W	0	**T1 Count Mode** 0: Single Pass 1: Modulo N

Table 21.Counter/Timer 0 Register—R244 T0 F4h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

Note: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–0	T0	R	X	T0 Current Value
		W	X	T0 Initial Value Range = 1–256 decimal; 00h–01h

Table 22.Prescaler 0 Register—R245 PRE0 F5h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	0

Note: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 00h–01h
1	Reserved	W	X	Reserved—must be 0
0	Count	W	0	**T0 Count Mode** 0: Single Pass 1: Modulo N

Table 23.Port 2 Mode Register—R246 P2M F6h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

Note: W = Write.

Bit Position	Bit Field	R/W	Reset Value	Description
7–0	P20–P27	W	1	**P20–P27 I/O Definition** 0: Defines bit as Output 1: Defines bit as Input

Table 24.Port 3 Mode Register—R247 P3M F7h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0

Note: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–2	Reserved	W	X	Reserved—must be 0
1	Port 3	W	0	**Port 3 Inputs** 0: DIGITAL mode 1: ANALOG mode
0	Port 2	W	0	**Port 2 Outputs** 0: Open-Drain 1: Push-Pull

Table 25.Port 0 and 1 Mode Register—R248 P01M F8h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	X	X	0	1

Note: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–5, 3	Reserved	W	X	**Reserved—must be 0**
4	Reserved	W	0	**Reserved—must be 0**
2	Reserved	W	X	**Reserved—must be 1**
1–0	P02–P00	W	01	**P02–P00 Mode** 00: Output 01: Input

Table 26.Interrupt Priority Register—R249 IPR F9h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

Note: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7–6	Reserved	W	X	Reserved—must be 0
5	IRQ3, IRQ5	W	X	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 > IRQ5
4,3,0	Interrupt	W	X	**Interrupt Group Priority** 000: Reserved* 001: C > A > B 010: A > B > C 011: A > C > B 100: B > C > A 101: C > B > A 110: B > A > C 111: Reserved
2	IRQ0, IRQ2	W	X	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 > IRQ2
1	IRQ1, IRQ4	W	X	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 > IRQ1

Note: *Selecting a Reserved mode causes an undefined operation.

Table 27.Interrupt Request Register—R250 IRQ FAh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read, W = Write.

Bit Position	Bit Field	R/W	Reset Value	Description
7–6	Reserved	R/W	00	**Reserved—must be 0**
5	IRQ5	R/W	0	**Interrupt** IRQ5 = T1 1: Interrupt pending 0: No interrupt pending
4	IRQ4	R/W	0	**Interrupt** IRQ4 = T0 1: Interrupt pending 0: No interrupt pending
3	IRQ3	R/W	0	**Interrupt** IRQ3 = **P32** Input (rising edge) 1: Interrupt pending 0: No interrupt pending
2	IRQ2	R/W	0	**Interrupt** IRQ2 = P31 Input 1: Interrupt pending 0: No interrupt pending
1	IRQ1	R/W	0	**Interrupt** IRQ1 = P33 Input 1: Interrupt pending 0: No interrupt pending
0	IRQ0	R/W	0	**Interrupt** IRQ0 = P32 Input (falling edge) 1: Interrupt pending 0: No interrupt pending

Table 28.Interrupt Mask Register—R251 IMR FBh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	X	X	X	X	X	X	X

Note: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7	Master Interrupt Enable	R/W	0	1: Enables global interrupts
6	Reserved	R/W	X	Reserved—must be 0
5–0	IRQ0–IRQ5	R/W	X	1: Enables IRQ0–IRQ5 (D0 = IRQ0)

Table 29.Flag Register—R252 Flags FCh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

Note: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
7	Carry	R/W	X	Carry Flag
6	Zero	R/W	X	Zero Flag
5	Sign	R/W	X	Sign Flag
4	Overflow	R/W	X	Overflow Flag
3	Decimal Adjust	R/W	X	Decimal Adjust Flag
2	Half Carry	R/W	X	Half Carry Flag
1	User	R/W	X	User Flag F2*
0	User	R/W	X	User Flag F1*

Note: *Not affected by RESET.

Table 30.Register Pointer—R253 RP FDh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
7–4	Working Register Pointer	R/W	0	Working Register Pointer
3–0	Reserved	R/W	0	Must be 0

Table 31.General Purpose Register—R254 GPR FEh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
7–0	Stack	R/W	0	General Purpose Register

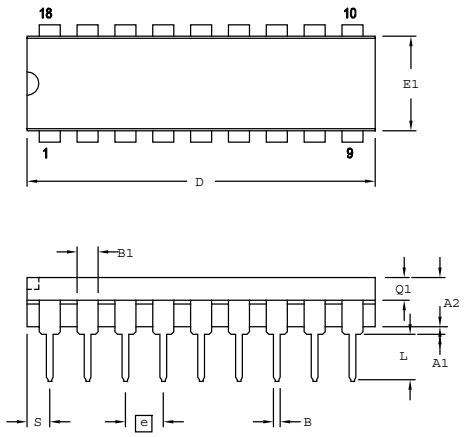
Table 32.Stack Pointer Low—R255 SPL FFh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
7–0	Stack	R/W	0	Stack Pointer Lower Byte (SP0–SP7)

Package Information

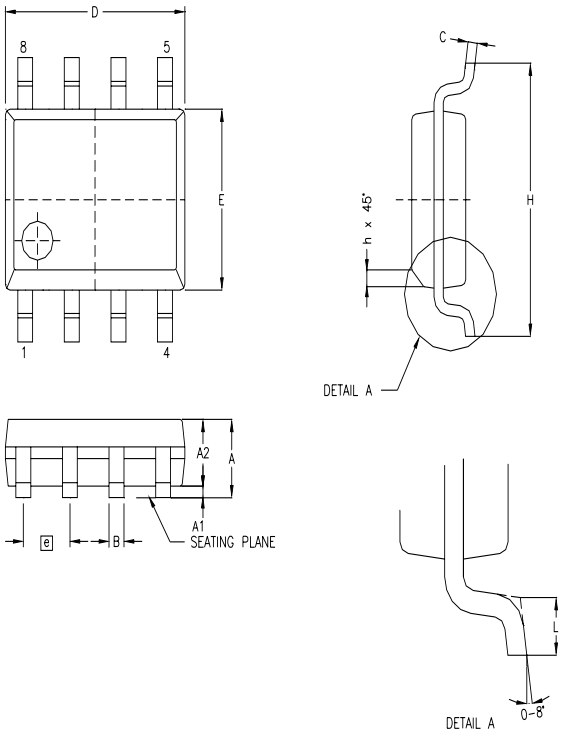
Figure 20. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 BSC		.100 BSC	
eA	7.87	9.40	.310	0.370
L	3.18	3.81	.125	.150
Q1	1.47	1.65	.058	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

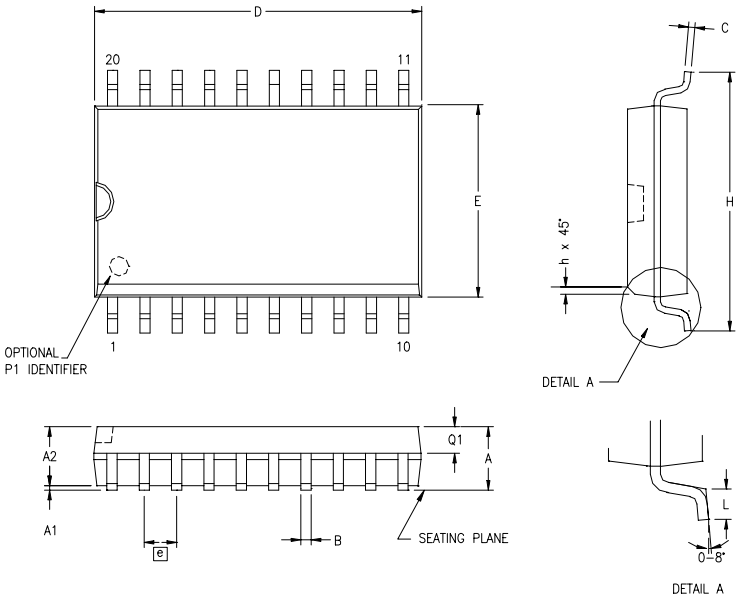
Figure 21. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.55	1.73	0.061	0.068
A1	0.10	0.25	0.004	0.010
A2	1.40	1.55	0.055	0.061
B	0.36	0.48	0.014	0.019
C	0.18	0.25	0.007	0.010
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.27 BSC		.050 BSC	
H	5.84	6.15	0.230	0.242
h	0.25	0.40	0.010	0.016
L	0.46	0.81	0.018	0.032

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 22. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Ordering Information

Table 33. Ordering Information

Pin Count	Package	Size (KB)	Description
18	DIP	0.5	Z86E0212PSC1995
			Z86E0212PEC1995
		1	Z86E0412PSC1995
			Z86E0412PEC1995
		2	Z86E0812PSC1995
			Z86E0812PEC1995
		4	Z86E0912PSC1995
			Z86E0912PEC1995
	SOIC	0.5	Z86E0212SSC1995
			Z86E0212SEC1995
		1	Z86E0412SSC1995
			Z86E0412SEC1995
		2	Z86E0812SSC1995
			Z86E0812SEC1995
		4	Z86E0912SSC1995
			Z86E0912SEC1995
20	SSOP	0.5	Z86E0212HSC1995
			Z86E0212HEC1995
		1	Z86E0412HSC1995
			Z86E0412HEC1995
		2	Z86E0812HSC1995
			Z86E0812HEC1995
		4	Z86E0912HSC1995
			Z86E0912HEC1995

Note: *The Standard temperature range is 0ºC to 70ºC. For parts that operate in the Extended temperature range of –40ºC to 105ºC, substitute the letter *E* for the letter *S*. For example, the PSI number for an 18-pin DIP operating at 1 KB in the extended temperature range is Z86E0412PEC1995.

For fast results, contact your local ZiLOG Sales offices for assistance in ordering the part(s) required. Contact your local ZiLOG Sales office by navigating to Sales Office on www.zilog.com.

Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86E0412PSC1995 is a 12-MHz 18-pin DIP that operates in the –0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86E0412PSC1995 part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
E	OTP Product
04	Product Number
12	Speed (MHz)
P	Dual In-line Processor
S	Standard Temperature
C	Environmental Flow

Z70 .35Tμ Process

The Z86E02/E04/E08/E09 family of parts are manufactured using ZiLOG's new advanced Z70 .35Tμ process. This process no longer requires the conventional 12.5VDC programming voltage—it operates with only 5VDC. Please refer to the Programming Specification for further information. Special consideration must be made in existing designs with this new process. Please contact the ZiLOG World Wide Customer Support Center for further information.

Precharacterization Product

The products represented by this document are newly introduced; hence ZiLOG has not completed a full characterization of the product. This document states what ZiLOG knows about this product at this time; however, additional features or nonconformance with some aspects of this document may be found, either by ZiLOG or its customers, in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0046	Unique Document Number
02	Revision Number
0401	Month and Year Published

Change Log

Rev	Date	Purpose	By
01	03/01	Original issue	K. Low, R. Beebe
02	04/01	Revise DC voltage specs	K. Low, R. Beebe

Index

Customer Feedback Form

Z86E02/E04/E08/E09 Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
910 E. Hamilton Avenue, Suite 110, MS 4–3
Campbell, CA 95008
Fax: (408) 558-8536
Email: tools@zilog.com

Problem Description or Suggestion

Please provide a complete description of the problem or suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.