MCP19061

Synchronous Four Switch Buck-Boost Analog Front End

Features

- AEC-Q100 Automotive Qualified, See Product Identification System
- 100W USB-PD/180W EPR with PPS Support
- 12-Bit Resolution for Voltage and Current Settings and Measurements Exceeding USB-PD PPS Requirements
- Accuracy of the Output Voltage Setting of 2% (Closed Loop) from Device to Device Over Output Voltage Range and Temperature
- Accuracy of the Output Current Setting of 3% (Closed Loop) from Device to Device Over Output Voltage Range and Temperature
- Input Voltage: +4.5V to +42V
- Fully Configurable:
  - Configurable protections: input and output over current, input over/under voltage, output over/under voltage, load dump, overtemperature, internal regulator fault
  - Configurable output: constant current operation, constant voltage operation
  - Adjustable frequency
  - Dynamically configurable by I^2C
- Synchronous 4-Switch Buck/Boost Architecture
  - Buck mode operation when $V_{OUT} < V_{IN}$
  - Boost mode operation when $V_{OUT} > V_{IN}$
  - Buck/Boost operation when $V_{OUT} \approx V_{IN}$
- Adjustable Output Range, 3V to 36V
- Internal LDOs and MOSFET Drivers
- High Accuracy Internal Divider to Set Full Range Output Voltage Without External Resistors
- Accuracy of Input and Output Voltage Measurement of 2% from Device to Device Over Output Voltage Range and Temperature
- Accuracy of the Output Current Measurement of 3% from Device to Device Over Output Voltage Range and Temperature
- Low Quiescent Current in Shutdown Mode
- Switching Frequency Range of 300 kHz to 500 kHz
- Tolerant in Nonoperating 42V Automotive Load Dump Condition
- USB Power Delivery Support:
  - High output impedance when stopped
  - Output discharge function
  - Output overcurrent, overload and short-circuit in accordance with USB power delivery
  - Regulation mode (voltage/current) detection

Device Overview

The MCP19061 is a highly integrated, mixed-signal four switch buck-boost controller that operates from +4.5V to +36V and can withstand up to +42V non-operating.

The MCP19061 features a digital PWM controller with a serial communication bus for external programmability and reporting.

Various enhancements were added to the MCP19061 to provide USB-PD compatibility with minimum external components along with improving calibration, increasing accuracy and providing greater flexibility.

Complete customization of device operating parameters, start-up or shutdown profiles, protection levels and fault handling procedures are accomplished by internal digital registers.

An integrated high accuracy reference voltage is used for setting output current or voltage. Internal input and output dividers facilitate the design while maintaining high accuracy. High accuracy CSA allows precision current regulation and measurement.

The MCP19061 device contains 3 internal LDOs. A 5V LDO (VDD) is used to power internal analog and gate driver circuits and provide 5V externally. A 4V LDO (AVDD) is used to power the internal analog circuitry. A 1.8V LDO is used to supply the internal logic circuitry.

The MCP19061 is packaged in a 32-lead 5 mm x 5 mm VQFN.

System designers have the ability to configure application-specific features allowing users of the MCP19061 device to save on costly board real estate and additional component costs.

A high speed (1 MHz) I^2C serial bus is used for device communications from the MCP19061 to the system controller.

Pin Diagram

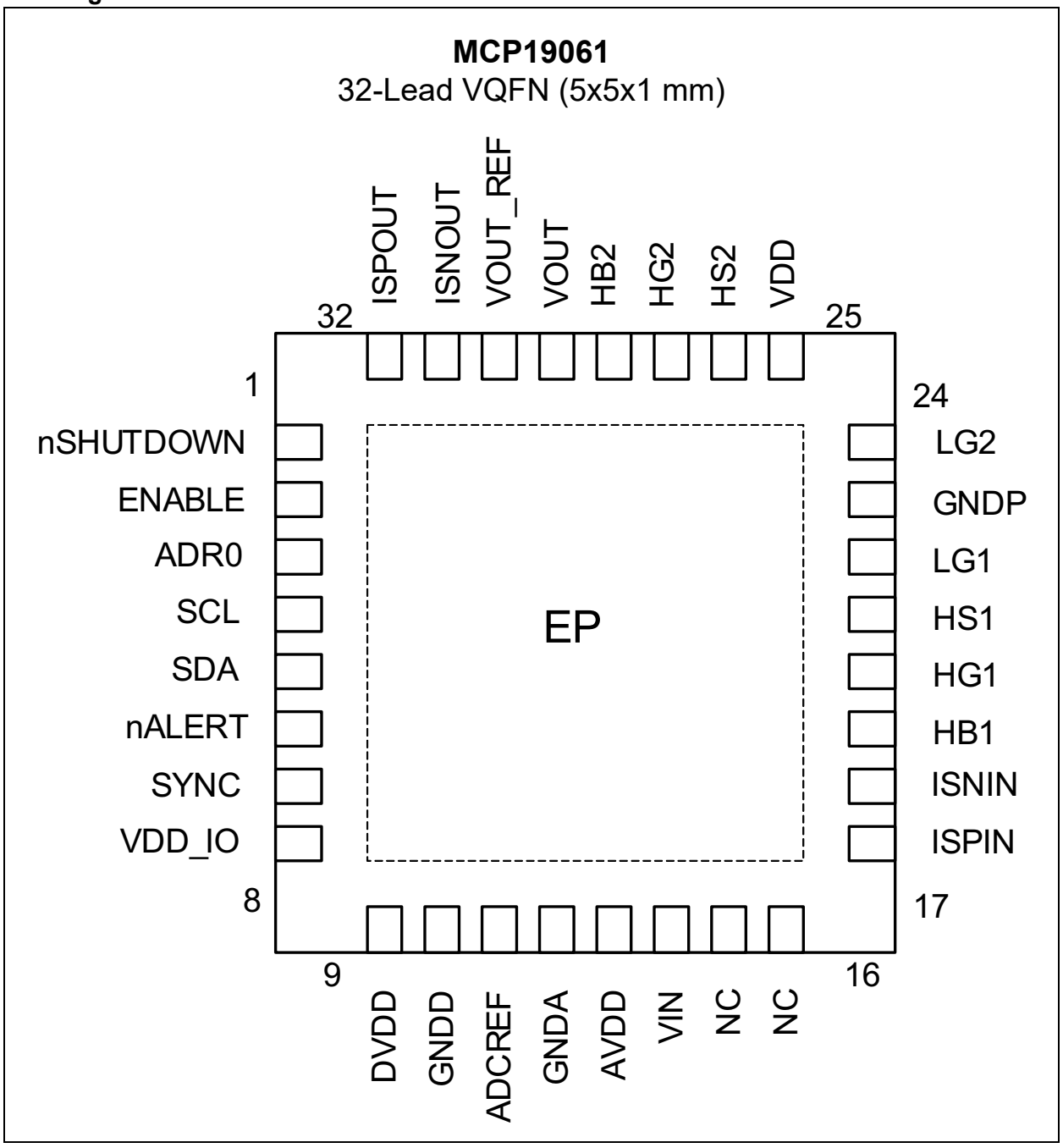
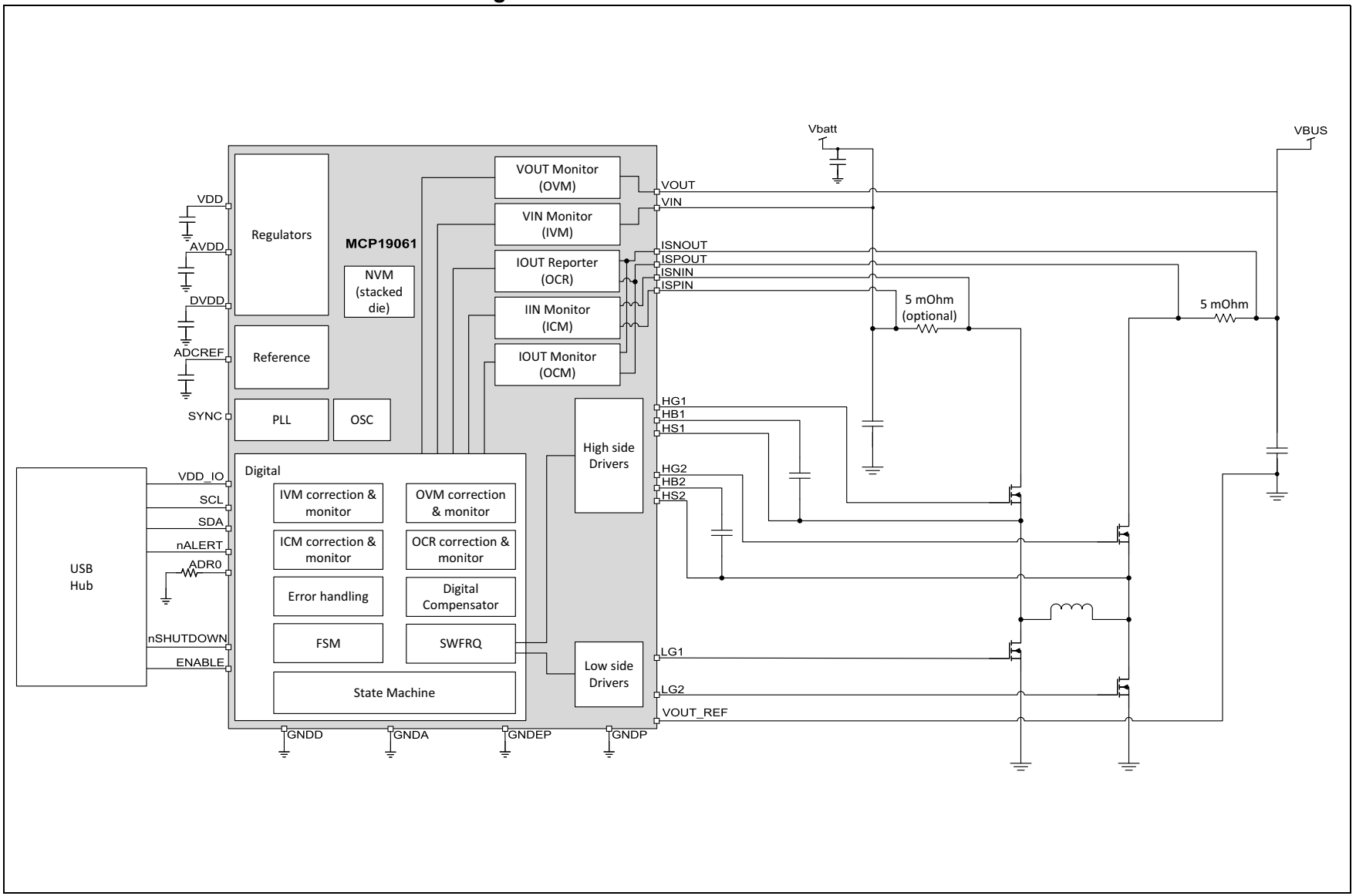


TABLE 1: MCP19061 PINOUT DESCRIPTION (SUMMARY)

Pin Number	Pin Name	Description
1	nSHUTDOWN	Shutdown pin. Pull low to put the device in low power mode
2	ENABLE	Enable pin. Starts the power train
3	ADR0	I^2C address setting pin. Connect a resistor to GNDA
4	SCL	I^2C clock
5	SDA	I^2C data
6	nALERT	Internal events detect pin
7	SYNC	Configurable input or output synchronization pin (if not used shall be configured as input and shall be grounded)
8	VDD_IO	Digital interface supply pin
9	DVDD	Output of the digital voltage regulator. Connect a capacitor to GNDD
10	GNDD	Digital ground
11	ADCREF	Analog to digital converters reference
12	GNDA	Analog ground
13	AVDD	Output of the analog voltage regulator. Connect a capacitor to GNDA
14	VIN	Chip supply input. Connect a capacitor to GNDP
15	NC	Not connected
16	NC	Not connected
17	ISPIN	Positive connection of the input current sense amplifier
18	ISNIN	Negative connection of the input current sense amplifier
19	HB1	Bootstrap supply 1. Connect a capacitor between this pin and HS1
20	HG1	Output of the high side driver 1
21	HS1	Connect to the source of the high side 1 MOS
22	LG1	Output of the low side driver 1
23	GNDP	Power ground
24	LG2	Output of the low side driver 2
25	VDD	Output of the internal regulator. Connect a capacitor to GNDP
26	HS2	Connect to the source of the high side 2 MOS
27	HG2	Output of the high side driver 2
28	HB2	Bootstrap supply 2. Connect a capacitor between this pin and HS2
29	VOUT	Output voltage sense
30	VOUT_REF	Output voltage reference
31	ISNOUT	Negative connection of the output current sense amplifier
32	ISPOUT	Positive connection of the output current sense amplifier
EP	EP	Exposed Thermal Pad: Heat slug, general device ground (shall be grounded)

MCP19061 Four Switch Buck Boost Block Diagram



MCP19061 Mode Control

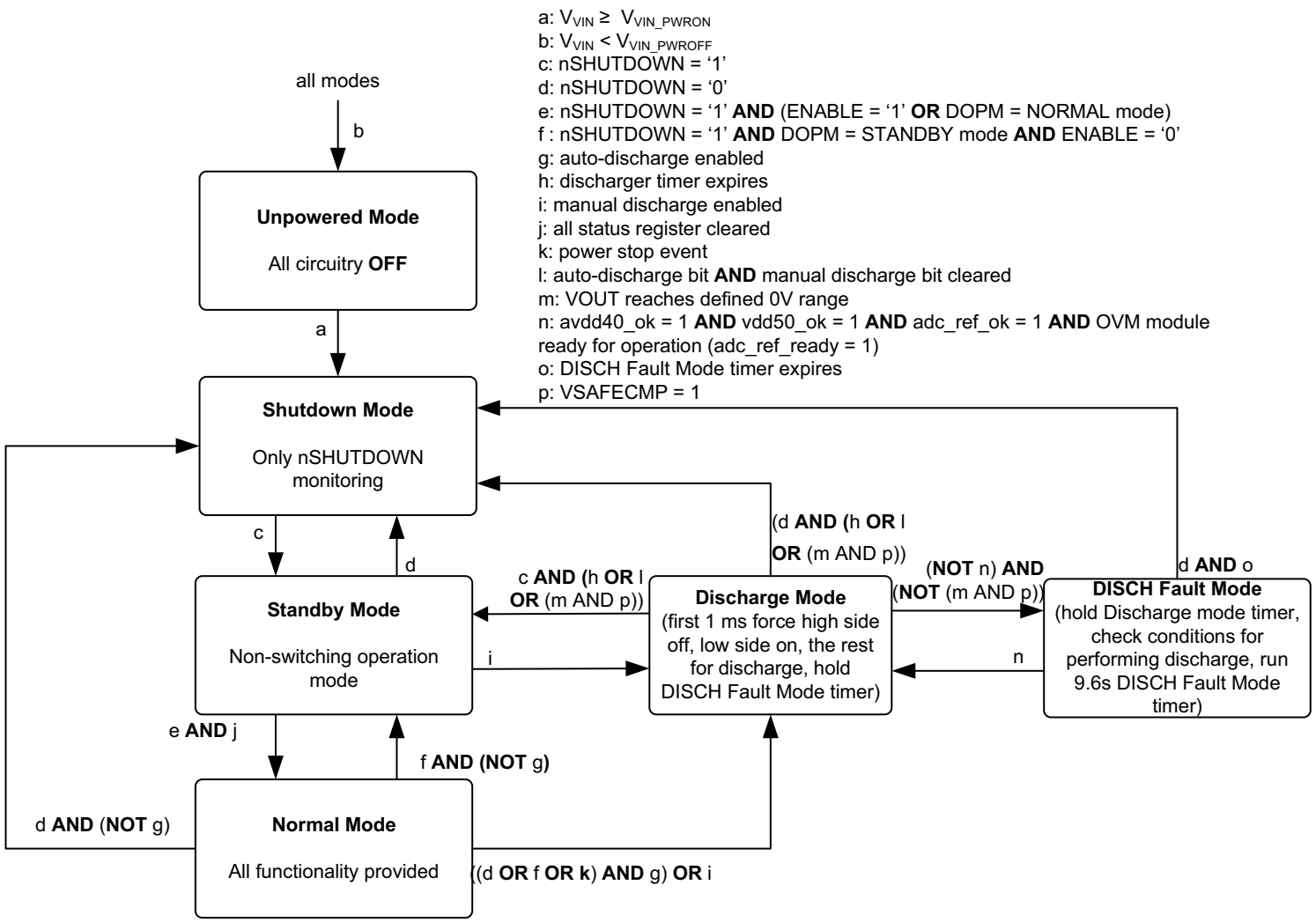


Table of Contents

1.0 PIN DESCRIPTION

The description of pins for the 32-Lead VQFN package (summary) is listed in Table 1. The location of the pins and pad are shown in the Pin Diagram. A detailed pin description can be found below.

1.1 Detailed Pin Functional Description

1.1.1 nSHUTDOWN PIN

nSHUTDOWN pin forces the device in low power shutdown mode when pulled down.

1.1.2 ENABLE PIN

ENABLE pin starts the power train when pulled high.

1.1.3 ADR0 PIN

ADR0 pin sets the I2C address of the device. Connect a resistor to GND.

1.1.4 SCL PIN

SCL pin is the clock of the I2C bus.

1.1.5 SDA PIN

SCL pin is the data of the I2C bus.

1.1.6 nALERT PIN

nALERT pin is an open drain pin. It is pulled low when an enabled internal event is detected.

1.1.7 SYNC PIN

SYNC pin, when enabled, is used to synchronize the switching frequency and phase of multiple devices. It may be configured as input or output.

1.1.8 VDD_IO PIN

VDD_IO is the digital interface supply pin. The voltage on this pin sets the logic levels on all digital pins. Connect a capacitor between this pin and the GNDD.

1.1.9 DVDD PIN

DVDD is the output of the digital voltage regulator. Connect a capacitor to GNDD.

1.1.10 GNDD PIN

GNDD is the digital ground connection pin.

This pin should be connected to the exposed pad on the bottom of the package.

1.1.11 ADCREF PIN

ADCREF is the output of the ADC reference. Connect a capacitor to GNDA.

1.1.12 GNDA PIN

GNDA is the small signal ground connection pin.

This pin should be connected to the exposed pad on the bottom of the package.

1.1.13 AVDD PIN

AVDD is the output of the analog voltage regulator. Connect a capacitor to GNDA.

1.1.14 VIN PIN

Input power connection pin of the device. It is recommended that capacitance be placed between this pin and the GND pin of the device.

1.1.15 NC PIN

Connect to GND.

1.1.16 NC PIN

Connect to GND.

1.1.17 ISPIN PIN

The noninverting input to internal input current-sense amplifier, typically used to differentially remote-sense the input current on a high side shunt.

1.1.18 ISNIN PIN

The inverting input to internal input current-sense amplifier, typically used to differentially remote-sense the input current on a high side shunt.

1.1.19 HB1 PIN

Connect the bootstrap capacitor between this pin and the HS1 pin. The PCB trace connecting the bootstrap capacitor must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.20 HG1 PIN

Connect the gate of the high-side 1 MOSFET to this pin. The PCB trace connecting HG1 to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.21 HS1 PIN

Connect the source of the high-side 1 MOSFET to this pin. The PCB trace connecting HS1 to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.22 LG1 PIN

Connect the gate of the low-side 1 MOSFET to this pin. The PCB trace connecting LG1 to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.23 GNDP PIN

Connect all large-signal level ground returns to GNDP. These large-signal level ground traces should have a small loop area and minimal length to prevent coupling of switching noise to sensitive traces.

This pin should be connected to the exposed pad on the bottom of the package.

1.1.24 LG2 PIN

Connect the gate of the low-side 2 MOSFET to this pin. The PCB trace connecting LG2 to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.25 VDD PIN

The output of the internal +5.0V regulator is connected to this pin. It is recommended that a 1.0 µF minimum/ 10 µF maximum bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be physically placed close to the device.

1.1.26 HS2 PIN

Connect the source of the high-side 2 MOSFET to this pin. The PCB trace connecting HS2 to the source must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.27 HG2 PIN

Connect the gate of the high-side 2 MOSFET to this pin. The PCB trace connecting HG2 to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.28 HB2 PIN

Connect the bootstrap capacitor between this pin and the HS2 pin. The PCB trace connecting the bootstrap capacitor must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

1.1.29 VOUT PIN

Output voltage sensing pin. Connect this pin to the output of the power supply.

1.1.30 VOUT_REF PIN

Output remote ground sensing pin. Connect this pin to the load GND.

1.1.31 ISNOUT PIN

The inverting input to the internal output current-sense amplifier, typically used to differentially remote-sense the output current on output high side shunt.

Caution: Do not filter this pin voltage, results may be unpredictable!

1.1.32 ISPOUT PIN

The noninverting input to the internal output current-sense amplifier, typically used to differentially remote-sense the output current on output high side shunt.

Caution: Do not filter this pin voltage, results may be unpredictable!

1.1.33 EXPOSED PAD (EP)

The exposed pad is used for GND connection and thermal dissipation. Connect the exposed pad to GND.

2.0 FUNCTIONAL DESCRIPTION

2.1 Linear Regulators

The operating input voltage for the MCP19061 ranges from +4.5V to +36V. The internal 5V LDO provides bias voltage for integrated MOSFET drivers and also can be used to bias additional external circuitry. Care should be exercised to avoid LDO overload. The output of the LDO is monitored and specific fault is generated in case of malfunction.

The internal 4V regulator provides bias voltage for the analog circuitry. The internal 1.8V regulator provides bias voltage for the digital core.

The bits that monitor the functionality of the LDOs are located in STASYS register. For each regulator, a decoupling capacitor must be connected between output pin and ground (4.7 µF/25V X7R ceramic capacitor).

2.2 ADCREF

An accurate reference voltage is internally provided for all voltage and current measurements and settings. A decoupling capacitor (recommended 1 µF/25V X7R, ceramic) must be connected to the ADCREF output pin.

2.3 Output Drive Circuitry

The MCP19061 integrates two low side and two high side drivers used to drive 4 external N-Channel power MOSFETs in a 4 switch buck-boost configuration. The floating MOSFET gate is connected to the HGx pin. The source of this MOSFET is connected to HSx pin. The low side MOSFET gate is connected to LGx pin and the source is connected to GNDP. The output drivers dead time is set with the DT<4:0> bits in the SWFRQCON1 Register, Register 6-20.

2.4 Current Sense

The input and output currents are differentially sensed by the MCP19061. The output current sense amplifier is optimized for 5 mΩ shunt resistors.

Caution: Do not insert differential or common mode filters in the input of the current sense amplifiers or unexpected behavior may occur. The traces connecting the CSA inputs with the shunts must be carefully differential routed to avoid noise coupling.

2.5 Voltage Sense

The MCP19061 measures both input and output voltages with fast ADCs. The values may be reported via the I^2C and are used by the internal state machine to control and protect.

The input voltage is measured on the VIN pin.

The output voltage is differentially measured between the VOUT and the VOUT_REF pins. It is recommended to route the VOUT and the VOUT_REF pins differentially to the output connections and to insert an RC filter between. Use 100Ω series resistor and compute the capacitor to have the same RC as the output bulk capacitor/ESR:

$$C = \frac{Output\ Cap \times ESR}{100}$$

2.6 Power Control Circuitry

The internal driver control of the MCP19061 is comprised of a digital control loop, four fast ADCs, several calibration circuits and several analog comparators.

The input and output voltages and currents are sampled by the four analog to digital converters. The digital converted values are corrected as offset and gain in digital blocks.

The corrected ADC values are compared to the target values by the digital modulator that generates the PWM signals accordingly.

The same corrected ADC values and several other digitized analog signals are used by the configurable digital protection circuit to alert the user and/or stop the power train if undesired events occur.

The control loop parameters are set in the following registers:

- BCKGPI Register 6-3 sets the buck control loop gain.
- BSTGPI Register 6-4 sets the boost control loop gain.
- SLOPCOMP Register 6-6 sets the factor for calculating the slope compensation value.
- SYSCAP Register 6-5 must be set in accordance to the used output capacitance and switching frequency.
- LC Register 6-23 must be set in accordance to the used inductor value.

Caution: Loop control registers can be written only when the power train is stopped!

Caution: Not using the recommended values for the loop parameters may lead to unpredictable results!

2.7 Output Regulation

The MCP19061 regulates both output voltage and output current. If both are enabled, the mode transition is seamless.

Output voltage set point must be written in the VREF<11:0> bits in the VREF Register 6-18.

Output current set point must be written in the IREF<11:0> in the IREF Register 6-19.

Output current regulation may be disabled by setting low the IREGEN bit in the COMPMODE Register 6-32.

2.8 PLL Control

The MCP19061 is internally clocked by a PLL (Phase Lock Loop) multiplied ring oscillator.

The source of this clock may be an internal 1.8 MHz oscillator or the SYNC pin. The selection is made in the PLLCON Register 6-35.

The ring oscillator optimum frequency is 36 MHz. The multiplication factor shall be set with the PLLPR bits in the PLLCON Register 6-35.

The recommended value of the ring oscillator is 36 MHz, therefore the PLLPR value shall be set to 0x4F, if the internal clock is selected, or to (36 MHz/SYNC frequency – 1), if external synchronization is needed.

The PLLCON Register 6-35 cannot be modified if any function needing the 36 MHz clock is enabled: power switching, discharge, ADC reading.

2.9 PWM Frequency

The switching frequency of the MCP19061 can be set in the SWFREQ2 Register 6-21.

To reduce EMI, the frequency may be user-selectable dithered. Dithering may be enabled by setting the DITHER bit in the SWFRQCON1 Register 6-20 and configured in the DITHER Register 6-22.

2.10 Synchronization

MCP19061 may output it's PWM frequency on the SYNC pin to allow the synchronization of other devices. To enable the sync function and set its direction the AUTORVB, CLKOUTEN and CLKSRC bits in the PLLCON Register 6-35 must be set.

MCP19061 may also synchronize it's PWM frequency to an external 300 kHz to 500 kHz input on SYNC pin. The PWM signal may have a programmable phase. The requested values to set the frequency parameters must be written in the PLLCON Register 6-35, SWFRQCON1 Register 6-20 and SWFRQCON2 Register 6-21.

Caution: All frequency related registers can be written only when the power train is stopped!

2.11 Temperature Management

To protect the MCP19061 from overtemperature conditions, a 150°C (min.) junction temperature thermal shutdown has been implemented. When the junction temperature reaches this limit, the device disables the output drivers. When the junction temperature is reduced by 20°C (typ.), output drive switching can be re-enabled after clearing the corresponding overtemperature flag.

2.12 USB Specific Circuits

2.12.1 OUTPUT DISCHARGE

The output discharge circuit will remove the charge stored in the output capacitor at each power stop. The output voltage of the power supply is reduced to VSafe0 in less than 600 ms. Once any of the above conditions is met the discharge stops. The function is automatic, occurring each time the device is disabled or shutdown if the AUTODSCH bit in the MODECON Register 6-34 is set. A discharge may be initiated at any moment, if the output power is stopped, setting high the MANUDSCH bit in the MODECON Register 6-34. If the discharge did not succeed to drop the output voltage below VSafe0 in 600 ms the DISCHFAIL flag in the STASYS Register 6-41 is set.

2.12.2 OVERLOAD DETECTION

The MCP19061 detects an overload condition in accordance with the USB-PD and Apple peripheral requirements allowing high peak currents to pass for a given time. The overload profile and maximum current can be set in the USBOLD Register 6-27. The overload detection will set the OCROC in the STABB Register 6-42.

2.12.3 SHORT CIRCUIT DETECTION

In accordance with the USB-PD requirements, MCP19061 detects short circuit by entering in the current regulation mode and checking if the output voltage dropped bellow 2V. The detection of the short will set the OCRSC flag in the STABB Register 6-42.

2.12.4 OUTPUT VOLTAGE RISE/FALL WITH CONTROLLED SPEED

MCP19061 controls the speed of all the changes in the output voltage. The maximum speed is 30 mV/µs in accordance with USB-PD, but can be set lower with the VRAMP<3:0> from the VREF Register 6-18.

2.12.5 OUTPUT RESISTANCE IN STAND-BY OR SHUTDOWN

If the power train is stopped, the impedance of the MCP19061 at the VOUT connections exceeds 200K, thus allowing the detection of released line without needing a disconnect switch.

3.0 ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM RATINGS†

V_{VIN}, V_{ISPIN},V_{ISNIN}, V_{HS1}(DC) ..... -0.3V to +42V
V_{HG1}, V_{HB1} (DC) ..... -0.3V to +47V
V_{VOUT},V_{ISPOUT},V_{ISNOUT}, V_{HS2} (DC) ..... -0.3V to +40V
V_{HB2}, V_{HG2} (DC) ..... -0.3V to +45.5V
V_{LG1}, V_{LG2} (DC) ..... -0.3V to +5.5V
V_{HGx}-V_{HSx}, V_{HBx}-V_{HSx} ..... -0.3V to +5.5V
V_{DVDD} (DC) ..... -0.3V to +2V
V_{VDD_IO}, V_{VDD},V_{AVDD},V_{ADCREF}, (DC) ..... -0.3V to +5.5V
V_{ISPIN}-V_{VIN}(DC) ..... -2V to +2V
V_{ISNIN}-V_{VIN}(DC) ..... -36.7V to +5.5V
V_{ISNIN}-V_{VIN},(Transient, <100 nsec) ..... -42V to +5.5V
V_{ISPOUT}-V_{VOUT}, ,V_{ISNOUT}-V_{VOUT},(DC) ..... -1V to +1V
Differential DC voltage among GNDD, GNDA, GNDP and GNDEP (exposed die pad)(DC) ..... -0.3V to +0.3V
V_{VOUT_REF}(DC) ..... -0.3V to +0.5V
nSHUTDOWN ..... -0.3V to V_{IN}
Maximum Voltage: Any Logic Pin ..... -0.3V to +5.5V
Storage Temperature ..... -55°C to +150°C
Operating Junction Temperature ..... -40°C to +125°C

ESD Protection on All Pins:
HBM ..... 2.0 kV
CDM 750V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2 Electrical Characteristics

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage	V_{IN}	**6**	—	**36**	V	
UVLO Release Level	—	**5.05**	5.3	**5.55**	V	Voltage rising
UVLO Reset Level	—	**4.05**	4.3	**4.55**	V	Voltage falling
Input Quiescent Current	I_Q	—	—	**15**	mA	Not switching
Shutdown Current	I_{SHDN}	—	—	**10**	µA	
Logic Interface Supply Input						
Peripheral Voltage	V_{VDD_IO}	**2.7**	—	**5.3**	V	
Peripheral Voltage Startup Threshold	—	**2.55**	—	**2.75**	V	Voltage rising
Peripheral Voltage Turnoff Threshold	—	**2.35**	—	**2.55**	V	Voltage falling

Note 1: V_{DD} is the voltage present at the VDD pin.
2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.
3: These parameters are characterized, but not production tested.

3.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Quiescent Current	$I_{Q\_VDD\_IO}$	—	6	10	µA	Not switching
Shutdown Current	$I_{SHDN\_VDD\_IO}$	—	—	**1**	µA	
Linear Regulator V_{DD}						
Decoupling Capacity	CV_{DD}	3.3	4.7	10	µF	
Internal Circuitry Bias Voltage	V_{DD}	**4.79**	5	**5.29**	V	V_{IN} = 6.0V to 36V, I_{OUT} = 65 mA
Maximum External V_{DD} Output Current	I_{DD_OUT}	—	—	**65**	mA	V_{IN} = 6.0V to 36V **(Note 1)**
Line Regulation	$\Delta V_{DD\text{-}OUT}/(V_{DD\text{-}OUT} * \Delta V_{IN})$	—	—	**0.5**	%/V	6.0V ≤ V_{IN} ≤ 36V **(Note 1)**
Load Regulation	$\Delta V_{DD\text{-}OUT}/V_{DD\text{-}OUT}$	—	—	**0.5**	%	I_{DD_OUT} = 1 mA to 65 mA **(Note 1)**
Output Short-Circuit Current	I_{DD_SC}	**70**	—	**130**	mA	V_{IN} = 6V to 36V **(Note 1)**
Dropout Voltage	$V_{IN} - V_{DD}$	—	—	**0.6**	V	I_{DD_OUT} = 20 mA, VDD = 4.5V **(Notes 1 and 2)**
Power Supply Rejection Ratio	$PSRR_{LDO}$	—	60	—	dB	f = 100 Hz, 10 KHz, 100 KHz I_{DD_OUT} = 5 mA, 20 mA, 60 mA
Analog Linear Regulator AV_{DD}						
Decoupling Capacity	CA_{DD}	3.3	4.7	10	µF	
Internal Analog Supply Voltage	AV_{DD}	**4.026**	4.096	**4.166**	V	
Line Regulation	—	—	—	**0.5**	%	
Load Regulation	—	—	—	**0.5**	%	
Digital Linear Regulator DV_{DD}						
Decoupling Capacity	CDV_{DD}	3.3	4.7	10	µF	
Internal Digital Supply Voltage	DV_{DD}	**1.824**	1.866	**1.907**	V	
Line Regulation	—	—	—	**0.5**	%	
Load Regulation	—	—	—	**0.5**	%	
Internal ADC Reference	ADCREF	2.033	2.048	2.062	V	
Output Voltage Monitor						
Resolution	nbits	—	12	—	bits	
Step Size	—	—	10	—	mV	
Full-scale Range	FSR	0	—	40	V	

Note 1: V_{DD} is the voltage present at the VDD pin.

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3: These parameters are characterized, but not production tested.

3.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Tolerance	OVM_TOL	-2	—	2	%	V_{OUT} = 3 to 36V
V_{OUT_REF} Range	—	-300	—	500	mV	
Output Current Monitor						
Resolution	nbits	—	12	—	bits	
Step size	—	—	5	—	mA	5 mΩ shunt
Full-scale range	FSR	**0**	—	**15**	A	5 mΩ shunt
Tolerance	OCM_TOL	-2.5	—	2.5	%	I_{OUT} = 3 to 5A
		-7.5/I_{OUT}	—	7.5/I_{OUT}	%	I_{OUT} = 1 to 3A
Input Voltage Monitor						
Resolution	nbits	—	12	—	bits	
Step Size	—	—	10	—	mV	
Full-scale Range	FSR	—	—	40	V	
Tolerance	IVM_TOL	-2	—	2	%	
Output Impedance						
Output Resistance	R_{OUT}	200	—	—	kΩ	Power train stopped
Output Current Sense Amplifier						
Input Offset Voltage	V_{OS}	**-3**	—	**3**	LSB	Digitally corrected
Gain Error	—	**-3**	—	**3**	LSB	Digitally corrected
Differential Sense Range	—	**-16**	—	**76.8**	mV	DC
Differential Sense Range	—	**-64**	—	**300**	mV	Peak
Input Differential Impedance	—	—	2K||12p	—	Ω||F	
Input Common Mode Impedance	—	—	5M||6p	—	Ω||F	
Gain-Bandwidth Product	GBWP	300	—	—	kHz	
Common-Mode Range	V_{CMR}	**-0.3**	—	**36**	V	
Common-Mode Rejection Ratio	CMRR	100	120	—	dB	
Amplifier PSRR	PSRR	60	80	—	dB	
Input Current Monitor						
Input Offset Voltage	V_{OS}	**-18**	—	**18**	mV	
Differential Sense Range	—	**0**	—	**1.218**	V	
Gain	—	**0.995**	—	**1.005**	—	
Input Differential Impedance	—	—	20K||6p	—	Ω||F	

Note 1: V_{DD} is the voltage present at the VDD pin.

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3.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Common Mode Impedance	—	—	5M||6p	—	Ω||F	
Gain-Bandwidth Product	GBWP	14.4	—	—	MHz	
Common-Mode Range	V_{CMR}	-0.3	—	42	V	
Common-Mode Rejection Ratio	CMRR	90	120	—	dB	
Amplifier PSRR	PSRR	59.9	80	—	dB	
Output Drivers						
Gate Drive Source Resistance	R_{DR-SRC}	—	—	**4**	Ω	V_{DR} = 4.5V, measured at 100 mA
Gate Drive Sink Resistance	$R_{DR-SINK}$	—	—	**2**	Ω	V_{DR} = 4.5V, measured at 200 mA
Rise Time	T_{RL}	—	—	50	ns	V_{DR} = 4.5V, C_{LOAD} = 3.3 nF
Fall Time	T_{FL}	—	—	50	ns	V_{DR} = 4.5V, C_{LOAD} = 3.3 nF
High Side Driver Minimum On Time	—	50	—	—	ns	V_{DR} = 4.5V
High Side Driver Leakage Current	—	—	—	15	µA	V_{DR} = 4.5V
Bootstrap Circuits						
Undervoltage High Threshold	V_{BTUVH}	**4.1**	—	**4.3**	V	
Undervoltage Low Threshold	V_{BTUVL}	**3.6**	—	**3.8**	V	
Bootstrap Switch Resistance	R_{BTSW}	—	—	10	Ω	
Dead-Time Adjustment						
Resolution	DT_{RES}	—	3.5	—	ns	
Dead-Time Adjustable Range	DT_{RANGE}	4	—	55	ns	
PWM						
Default Frequency	F_{SW}	**436**	450	**464**	kHz	Factory setting
Synchronization Range	F_{SW_SYNC}	300	—	600	kHz	±15% around internal set point
Synchronization Duty Cycle		10	—	90	%	
Spread Spectrum Range	F_{SS}	-7	—	7	%	

Note 1: V_{DD} is the voltage present at the VDD pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: These parameters are characterized, but not production tested.

3.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Discharge						
Output Discharge Current	I_{DIS}	**90**	—	**150**	mA	2V to 36V
VSafe0 Threshold	VSafe0	**0.581**	—	**0.712**	V	
SYNC, ENABLE, nALERT, nSHUTDOWN Pins						
Input High Threshold	$V_{LOGIC\_HI\_IN}$	0.7*VDDIO	—	—	V	
Input Low Threshold	$V_{LOGIC\_LO\_IN}$	—	—	0.3*VDDIO	V	
nSHUTDOWN Input High Threshold	$V_{LOGIC\_HI\_IN}$	1.2	—	—	V	
nSHUTDOWN Input Low Threshold	$V_{LOGIC\_LO\_IN}$	—	—	0.4	V	
Output Low Voltage	$V_{LOGIC\_LO\_OUT}$	—	—	**0.4**	V	I_{OL} = 3 mA
SYNC Output High Voltage	V_{GPIO_OH}	V_{DD} – 0.4	—	—	V	I_{OH} = 3 mA
nSHUTDOWN and ENABLE Deglitch Time	GPIO_I_{IL}	**1**	2	**4.5**	µs	
I^2C						
I^2C Input High Threshold	$V_{I2C\_H\_IN}$	0.7*VDD_IO	—	—	V	
I^2C Input Low Threshold	$V_{I2C\_L\_IN}$	-0.5	—	0.3*VDD_IO	V	
SCL Clock Frequency	f_{SCL}	100	—	1000	kHz	**(Note 3)**
I^2C Output Low Voltage	$V_{I2C\_L\_OUT\_1}$	0	—	0.4	V	(Open-drain) at 3 mA sink current; VDD_IO > 2.7V **(Note 3)**
Bus Free Time between a STOP and START Condition	t_{BUF}	0.5	—	—	µs	**(Note 3)**
Hold Time (Repeated) START Condition	$t_{HD(STA)}$	260	—	—	ns	**(Note 3)**
Low Period of the SCL Clock	t_{LOW}	0.5	—	—	µs	**(Note 3)**
High Period of the SCL Clock	t_{HIGH}	260	—	—	ns	**(Note 3)**
Setup Time for a Repeated START Condition	$t_{SU(STA)}$	260	—	—	ns	**(Note 3)**
Data Setup Time	$t_{SU(DAT)}$	50	—	—	ns	**(Note 3)**
Data Hold Time	$t_{HD(DAT)}$	0	—	—	µs	**(Note 3)**
Rise Time of SCL Signal	t_{RCL}	—	—	120	ns	**(Note 3)**

Note 1: V_{DD} is the voltage present at the VDD pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: These parameters are characterized, but not production tested.

3.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 13V, F_{SW} = 450 kHz, T_J = +25°C. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fall Time of SCL Signal	t_{FCL}	—	—	120	ns	**(Note 3)**
Rise Time of SDA Signal	t_{RDA}	—	—	120	ns	**(Note 3)**
Fall Time of SDA Signal	t_{FDA}	—	—	120	ns	**(Note 3)**
Setup Time of STOP Condition	$t_{SU(STO)}$	260	—	—	ns	**(Note 3)**
Capacitive Load for SDA and SCL	C_B	—	—	550	pF	**(Note 3)**
Constant Current Source (ADR0 Pin)	I_{ADR0}	49	50	51	µA	Current source on communication address set pin. Max pin voltage = 2.0V.
Data Valid Time	$t_{VD;DAT}$	—	—	0.45	µs	The maximum $t_{HD(DAT)}$ must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. **(Note 3)**
Low-level Output Current	I_{OL}	20	—	—	mA	VOL = 0.4V
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}	0	—	50	ns	**(Note 3)**
Input Current Each I/O Pin	Ii	-10		10	µA	
Thermal Shutdown						
Thermal Shutdown Set Threshold	T_{SHD_SD}	150	160	170	°C	
Thermal Shutdown Release Threshold	T_{SHD_REL}	117	—	145	°C	

Note 1: V_{DD} is the voltage present at the VDD pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: These parameters are characterized, but not production tested.

3.3 Thermal Specifications

Parameters	Sym.	Min.	Typ.	Max.	Units
Temperature Ranges					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Maximum Junction Temperature	T_J	—	—	+150	°C
Storage Temperature Range	T_A	-65	—	+150	°C
Thermal Package Resistances					
Thermal Resistance, 32L-QFN 5x5	θ_{JC}	—	—	30	°C/W

4.0 TYPICAL PERFORMANCE CURVES

Note: Unless otherwise indicated, V_{in} = 13V, F_{sw} = 450 kHz

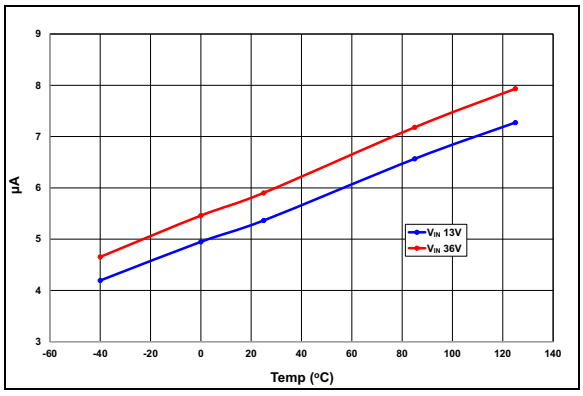


FIGURE 4-1: *Input Current Consumption in Shutdown Mode (ENABLE = 0, nSHUTDOWN = 0).*

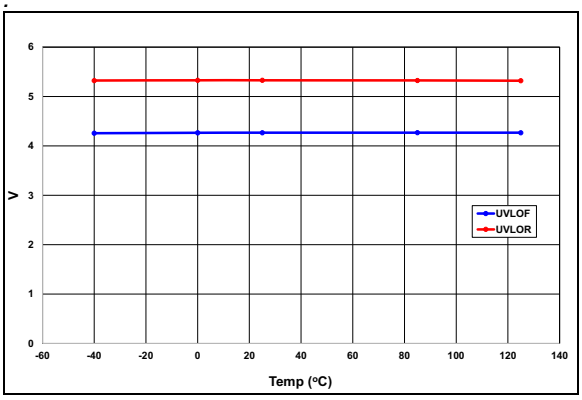


FIGURE 4-4: *V_{IN} UVLO Hardware.*

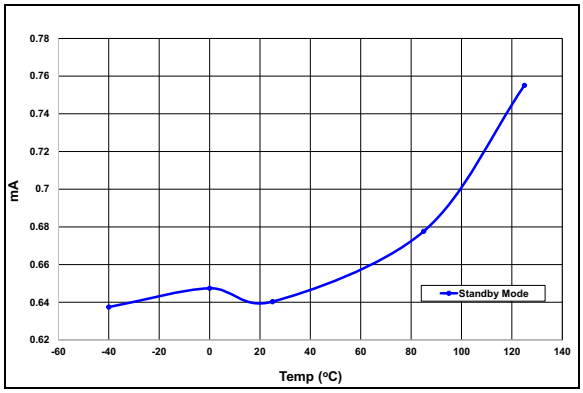


FIGURE 4-2: *Input Current Consumption in Standby Mode (ENABLE = 0, nSHUTDOWN = 1).*

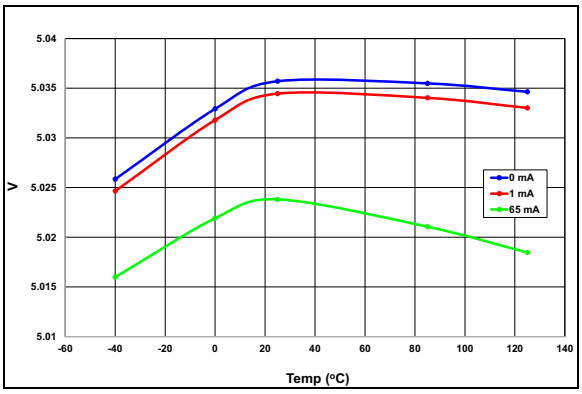


FIGURE 4-5: *VDD50 vs. Temperature.*

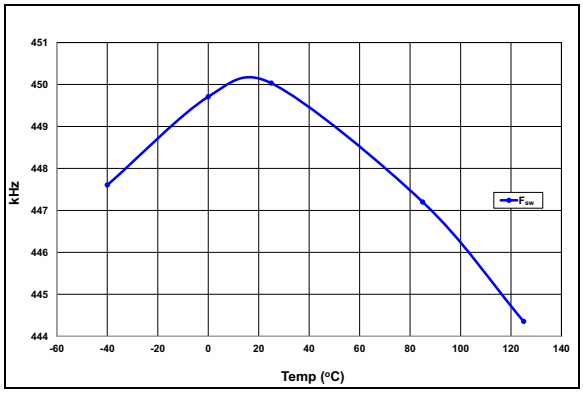


FIGURE 4-3: *Switching Frequency vs. Temperature*

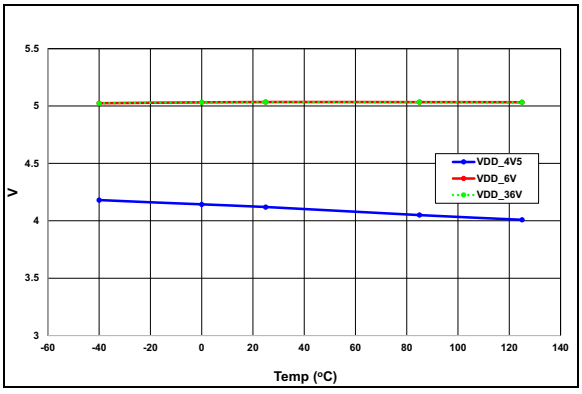


FIGURE 4-6: *VDD50 vs. V_{in}.*

Note: Unless otherwise indicated, V_{in} = 13V, F_{sw} = 450 kHz

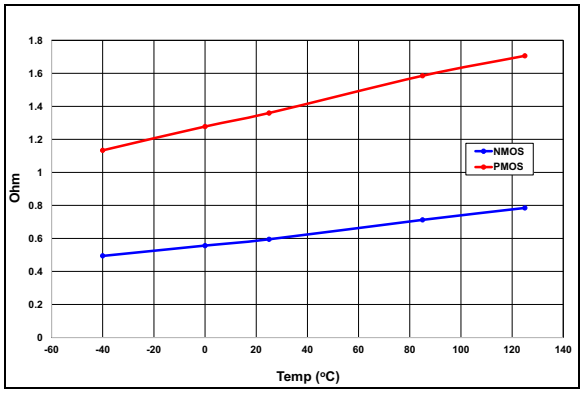


FIGURE 4-7: *Low Side Gate Drive Resistance on Buck Leg vs. Temperature.*

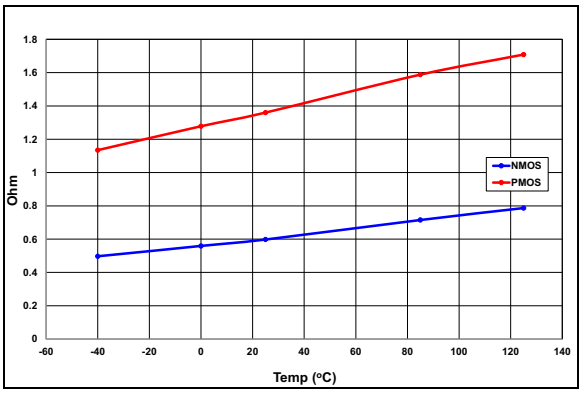


FIGURE 4-9: *High Side Gate Drive Resistance on Buck Leg vs. Temperature.*

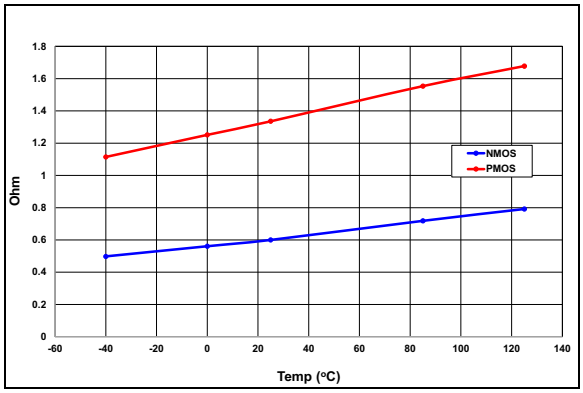


FIGURE 4-8: *Low Side Gate Drive Resistance on Boost Leg vs. Temperature.*

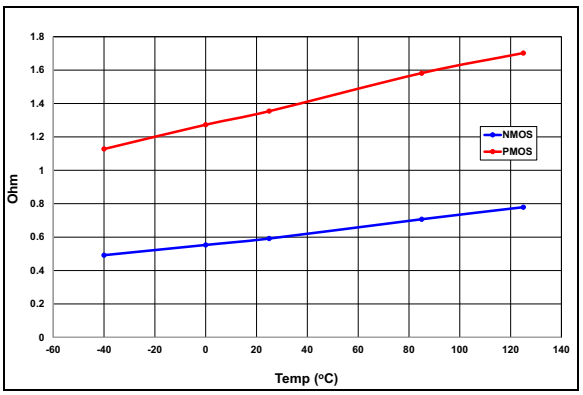


FIGURE 4-10: *High Side Gate Drive Resistance on Boost Leg vs. Temperature.*

5.0 CONFIGURING THE MCP19061

The MCP19061 device is a digital power controller. The device configuration is handled through register settings instead of adding external components.

The following sections detail how to set the control registers for all the configurable parameters.

5.1 I²C Communication

The I²C module is digital except for the address setting pin interface. It accepts commands and responds with internal information when requested by an external initiator.

The I²C speeds are 100 kHz, 400 kHz and 1 MHz.

The address can be externally set using a pin on the device.

The protocol is similar to simplified SMBUS, 16-bit word only, with PEC. The MCP19061 is not SMBus compatible in all requirements.

An open drain nALERT pin is provided. The MCP19061 pulls down this pin when a non-masked event is detected.

There are only 2 command types, “READ” and “WRITE”. Both are initiated by an external device.

All commands are in fact the addresses of the registers inside the MCP19061 that must be read or written.

A write command looks like in the Figure 5-1.

A read command looks like in Figure 5-2

The default I²C chip address is set by external resistor connected between ADR0 pin and GND. See Register 6-36 (I²C Address Setting Register) and Table 6-2 (I²C Address Resistor Selection).

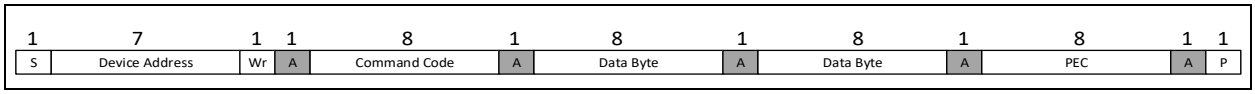


FIGURE 5-1: *Write Command.*

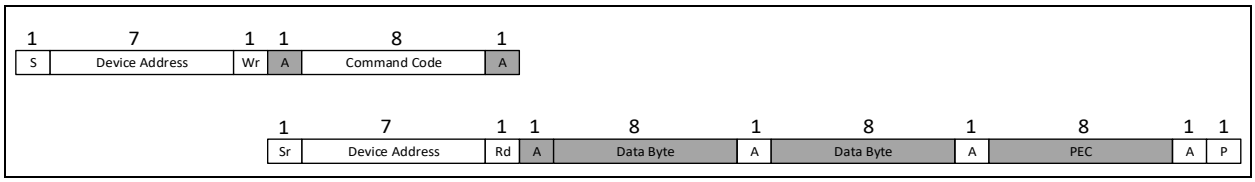


FIGURE 5-2: *Read Command.*

6.0 REGISTER ORGANIZATION

There are several types of registers in the MCP19061:

- Identification register
- Configuration setting registers
- Reporting registers
  - Measurement result registers
  - Status registers
- User registers
- Save/restore register

6.1 Identification Register

The identification Register 6-1 CHIP_REV_ID contains the chip ID and revisions version. The information is read-only.

The address of Register 6-1 CHIP_REV_ID is 01h.

6.2 Configuration Setting Registers

The configuration setting registers are readable and writable. The addresses range is 04h to 27h.

The content of these registers may be saved and restored in the NVM.

They are used to configure:

- communication
- operation mode of the power supply
- startup
- protections behavior and detection levels
- output parameters
- feedback loop parameters
- USB-PD features

6.3 Reporting registers

There are 2 types of reporting registers:

6.3.1 RESULT REGISTERS

6.3.1.1 Measurement Result Registers

These registers are read only and contain the results of different measurements and detections. Both raw and corrected results are available.

The measurement result registers are located at addresses from 60h to 67h.

6.3.1.2 Error Comparators Result Registers

IVMOUT Register 6-45 (address 5Ch), OOUT1 Register 6-46 (address 5Dh) and OOUT2 Register 6-47 (address 5Eh) contains the unlatched outputs of the error comparators.

These registers are read-only.

6.3.2 STATUS REGISTERS

STASYS Register 6-41 (address 58h) and STABB Register 6-42 (address 59h) contain the error and event flags.

The NVMSTAT Register 6-43 (address 5Ah) contains the NVM relevant status bits.

The RFLAG Register 6-44 (address 5Bh) contains the regulation mode flags.

The CRC Register 6-2 (address 03h) displays the CRC for the calibration and configuration sections of the NVM.

The status registers, with the exception of the CRC register, are readable and erasable. The CRC register is only readable.

6.4 User Registers

The MCP19061 includes 4 general purpose registers, the GPRA Register 6-37 (address 28h), GPRB Register 6-38 (address 29h), GPRC Register 6-39 (address 2Ah), GPRD Register 6-40 (address 2Bh).

The user may store arbitrary information inside these registers and read it back.

These registers are volatile and not stored in the NVM.

6.5 Save/restore register

The save/restore NVMCTRL Register 6-52 address is 70h.

The user may save all the configuration registers in NVM to avoid re-writing them at the power up. To do this, the WSTART bit in the NVMCTRL Register 6-52 shall be set high. The bit will automatically reset when the operation is completed. The save operation can be done only in standby mode.

The configuration will be automatically reloaded at power up.

User may also restore the saved configuration any time by setting high the RSTART bit in the NVMCTRL Register 6-52. The bit will automatically reset when the operation is completed.

6.6 List of Registers

The complete list of registers can be found below.

TABLE 6-1: MCP19061 REGISTERS SUMMARY

Addr.	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	CHIP_REV_ID Register 6-1	CHIP_CODE [7:0]								ANA_REV_ID [3:0]				DIG_REV_ID [3:0]			
03h	CRC Register 6-2	CRCCONF [7:0]								CRCCAL [7:0]							
04h	BCKGPI Register 6-3	—	—	—	—	BCKGPI [11:0]											
05h	BSTGPI Register 6-4	—	—	—	—	BSTGPI [11:0]											
06h	SYSCAP Register 6-5	—	—	—	—	SYSCAP [11:0]											
07h	SLOPCOMP Register 6-6	SLOPCOMP [15:0]															
08h	IVMUVR Register 6-7	IVMUVR [9:0]										—	—	—	—	—	—
09h	IVMUVF Register 6-8	IVMUVF [9:0]										—	—	—	—	—	—
0Ah	IVMOVR Register 6-9	IVMOVR [9:0]										—	—	—	—	—	—
0Bh	IVMOVF Register 6-10	IVMOVF [9:0]										—	—	—	—	—	—
0Ch	IVMLDR Register 6-11	IVMLDR [9:0]										—	—	—	—	—	—
0Dh	IVMLDF Register 6-12	IVMLDF [9:0]										—	—	—	—	—	—
0Eh	OVMUV Register 6-13	OVMUVHY [7:0]								OVMUVF [7:0]							
0Fh	OVMOV Register 6-14	OVMOVHY [7:0]								OVMOVR [7:0]							
10h	OCROCR Register 6-15	OCROCR [9:0]										—	—	—	—	—	—
11h	OCROCF Register 6-16	OCROCF [9:0]										—	—	—	—	—	—
12h	VSAFECMP Register 6-17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSAFECMP
13h	VREF Register 6-18	VREF [11:0]												VRAMP[3:0]			
14h	IREF Register 6-19	IREF [11:0]												—	—	—	—
15h	SWFRQCON1 Register 6-20	SWFRQON	DITHER	—	DT [4:0]					—	—	—	—	—	—	—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

TABLE 6-1: MCP19061 REGISTERS SUMMARY (CONTINUED)

Addr.	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16h	SWFRQCON2 Register 6-21	PHASHIF [7:0]								SWFRQPR [7:0]							
17h	DITHER Register 6-22	—	DPS [2:0]			DOWNSLOP [2:0]			DIT-WAVE	MAXDC [7:0]							
18h	LC Register 6-23	—	—	—	—	LC [11:0]											
19h	IMSYS Register 6-24	VDDI-OUVM	ADCRE-FUVM	VDD50UVM	AVDD40UVM	LOSE-CLKSYSM	LOSE-CLK-PLLM	LOS-ESYNCM	DIS-CHFAILM	UOLDM	—	—	—	—	ITRDLE [2:0]		
1Ah	IMBB Register 6-25	ICMOCM	OCROCM	OCRREVCM	OCRSCM	VBSTUVM	OVTG-DRM	OVT-VDD50M	OVTA-VDD40M	IVMOVM	IVMUVM	IVMLDM	OVMOVM	OVMUVM	OVMZVM	PLL-PRFM	CRCERRM
1Bh	ADCON Register 6-26	ADCMANDLY [7:0]								—	—	—	—	OCRAD-CON	OCMAD-CON	OVMAD-CON	IVMAD-CON
1Ch	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1Dh	USBOLD Register 6-27	USB_CLASS [1:0]		USB_FACTOR[6:0]						USB_BASE [6:0]							
1Eh	IVMCNT Register 6-28	IVMUVCNT [2:0]			—	—	IVMLDCNT [2:0]			IVMOVCNT [2:0]			—	—	—	—	—
1Fh	OVMVCNT1 Register 6-29	OVMUVCNT [2:0]			—	—	—	—	—	OVMOVCNT [2:0]			—	—	—	—	—
20h	OVMVCNT2 Register 6-30	OVM2VCNT [2:0]			—	—	—	—	—	OVMSFCNT [2:0]			—	—	—	—	—
21h	CCNT Register 6-31	ICMOCCNT [2:0]			ICMOCSEL [4:0]					OCROCCNT [2:0]			—	—	OCRREVCCNT [2:0]		
22h	COMPMODE Register 6-32	HIDIS	LODIS	—	—	—	—	DRVMODE [1:0]		—	—	—	—	—	—	VREGEN	IREGEN
23h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
24h	EVSTOP Register 6-33	—	—	—	—	—	—	—	ORCST	IOVST	IUVST	OOVST	OUVST	IOCST	OOCST	OSHCST	UOLDST
25h	MODECON Register 6-34	—	—	—	—	—	—	MANUDSCH	AUTODSCH	—	—	—	—	—	—	DOPM [1:0]	
26h	PLLCON Register 6-35	—	—	—	—	—	AUTORVB	CLK-OUTEN	CLKSRC	PLLPR [7:0]							
27h	DEVID Register 6-36	—	—	—	—	—	—	—	ADR0EN	—	1	0	1	DEVID [3:0]			
28h	GPRA Register 6-37	GPRA [15:0]															
29h	GPRB Register 6-38	GPRB [15:0]															
2Ah	GPRC Register 6-39	GPRC [15:0]															

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

TABLE 6-1: MCP19061 REGISTERS SUMMARY (CONTINUED)

Addr.	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Bh	GPRD Register 6-40	GPRD [15:0]															
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58h	STASYS Register 6-41	VDDI-OUV	ADCRE-FUV	VDD50UV	AVDD40UV	LOSE-CLKSYS	LOSE-CLKPLL	LOS-ESYNC	DIS-CHFAIL	UOLD	—	—	SUFAIL	ACDONE	SUDONE	—	—
59h	STABB Register 6-42	ICMOC	OCROC	OCRREVC	OCRSC	VBSTUV	OVT-GDR	OVT-VDD50	OVTA-VDD40	IVMOV	IVMUV	IVMLD	OVMOV	OVMUV	OVMZV	PLLPRF	CRCERR
5Ah	NVMSTAT Register 6-43	—	—	—	—	—	—	—	—	—	—	NVM-FAIL	BUSY	CRC-CALOK	CRC-CALF	CRCCO-NFOK	CRCCO-NFF
5Bh	RFLAG Register 6-44	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VRFALG	IRFLAG
5Ch	IVMOUT Register 6-45	—	—	SIVMLD	—	MIVM-LDR	MIVM-LDF	—	—	—	—	SIVMOV	SIVMUV	MIVMOVR	MIVMOVF	MIVMUVR	MIVMUVF
5Dh	OOUT1 Register 6-46	—	—	SOC-ROC	SOC-RREVC	MOCROCR	MOCROCF	—	—	—	—	SOVMOV	SOVMUV	MOVMOVR	MOVMOVF	MOVMUVR	MOVMUVF
5Eh	OOUT2 Register 6-47	—	—	SOVM2V	—	—	—	MOVM2VR	MOVM2VF	—	—	SOVMSF	—	—	—	MOVMSFR	MOVMSFF
5Fh	OVTSTAT Register 6-48	—	—	—	—	—	—	—	—	—	—	—	OVTSDGDR [1:0]		OVTS-DVDD	OVTS-DAVDD	OVTS-DDVDD
64h	IVMCORRES Register 6-49	IVMCORRES [11:0]												—	—	—	—
65h	OVMCORRES Register 6-50	OVMCORRES [11:0]												—	—	—	—
67h	OCRCORRES Register 6-51	OCRCORRES [11:0]												—	—	—	—
70h	NVMCTRL Register 6-52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSTART	WSTART
71h	ADCGO Register 6-53	—	—	—	—	—	—	—	—	ASSEL[2:0]			—	—	—	CTS	GO

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

6.6.1 CHIP_REV_ID REGISTER

The CHIP_REV_ID register is a readable register, which contains chip code and the revision codes of the analog and digital sections. The address is 01h.

REGISTER 6-1: CHIP_REV_ID: CHIP REVISION ID

R-0	R-1	R-1	R-0	R-0	R-0	R-0	R-1
CHIP_CODE <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	x = Bit is unknown	‘0’ = Bit is cleared
‘1’ = Bit is set		

bit 15-8 **CHIP_CODE <7:0>:** Chip code

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ANA_REV_ID <3:0>				DIG_REV_ID <3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **ANA_REV_ID <3:0>:** Analog circuit revision

bit 3-0 **DIG_REV_ID <3:0>:** Digital circuit revision

6.6.2 CRC REGISTER

The CRC register is a readable register, which contains CRC codes for accessing the two register sections.

REGISTER 6-2: CRC: CRC REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CRCCONF <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **CRCCONF<7:0>:** CRC of the configuration register section

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CRCCAL <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **CRCCAL<7:0>:** CRC of the calibration register section

6.6.3 BCKGPI REGISTER

The BCKGPI register is a readable and writable register containing the buck gain compensation parameter. This register can’t be modified while the MCP19061 is enabled.

The default and recommended value is: 0x0400.

Caution: Modifying this value affects the regulation loop stability!

REGISTER 6-3: BCKGPI: BUCK GAIN COMPENSATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	—	—	BCKGPI <11:8>			
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **BCKGPI<11:8>:** MSB of the buck gain value

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BCKGPI <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **BCKGPI<7:0>:** LSB of the buck gain value

6.6.4 BSTGPI REGISTER

The BSTGPI register is a readable and writable register containing the boost gain compensation parameter. This register can't be modified while the MCP19061 is enabled.

The default and recommended value is: 0x300.

Caution: Modifying this value affects the regulation loop stability!

REGISTER 6-4: BSTGPI: BOOST GAIN COMPENSATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	—	BSTGPI <11:8>			
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BSTGPI<11:8>:** MSB of the boost gain value

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BSTGPI <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **BSTGPI<7:0>:** LSB of the boost gain value

6.6.5 SYSCAP REGISTER

The SYSCAP register is a readable and writable register containing the output capacitance multiplied by the switching frequency. This register can't be modified while the MCP19061 is enabled.

Default value: 0x164

Recommended value: Output capacitance in µF multiplied by the switching frequency in KHz.

Caution: Modifying this value affects the regulation loop stability!

REGISTER 6-5: SYSCAP: OUTPUT CAPACITOR COMPENSATION REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	SYSCAP <11:8>			
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SYSCAP<11:8>:** MSB of the output capacitor multiplied by the frequency value

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SYSCAP <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SYSCAP<7:0>:** LSB of the output capacitor multiplied by the frequency value

EQUATION 6-1: SYSCAP FORMULA

$$SYSCAP\ <11:0> = HEX(2 \times F_{sw}(\mathrm{MHz}) \times C_{out}(\mu\mathrm{F}))$$

Where:

F_{sw} = the selected switching frequency

Example:

For a value of 356 µF, the value is
HEX(2 × 0.5 × 356) = `0x164`

6.6.6 SLOPCOMP REGISTER

The SLOPCOMP register is a readable and writable register containing the value of the slope compensation parameter. This register can’t be modified while the MCP19061 is enabled.

Default and recommended value: 0x0FDC.

Caution: Modifying this value affects the regulation loop stability!

REGISTER 6-6: SLOPCOMP: SLOPE COMPENSATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
SLOPCOMP <15:8>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **SLOPCOMP<15:8>:** MSB of the slope compensation value

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
SLOPCOMP <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SLOPCOMP<7:0>:** LSB of the slope compensation value

6.6.7 IVMUVR REGISTER

Default value: 0x2500

The IVMUVR register is a readable and writable register containing the value of the input undervoltage rising threshold.

REGISTER 6-7: IVMUVR: INPUT UNDERVOLTAGE RISING REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
IVMUVR <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IVMUVR<9:2>:** MSB of the input undervoltage rising threshold

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMUVR <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IVMUVR<1:0>:** LSB of the of the input undervoltage rising threshold

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-2: IVMUVR FORMULA

$$IVMUVR\ <9:0> = HEX\left(\frac{1024 \times Input\ undervoltage\ rising\ threshold}{40.96}\right)$$

6.6.8 IVMUVF REGISTER

Default value: 0x2280

The IVMUVF register is a readable and writable register containing the value of the input undervoltage falling threshold.

REGISTER 6-8: IVMUVF: INPUT UNDERVOLTAGE FALLING REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
IVMUVF <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IVMUVF<9:2>:** MSB of the input undervoltage falling threshold

R/W-1	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMUVF <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IVMUVF<1:0>:** LSB of the of the input undervoltage falling threshold. It is calculated using Equation 6-3.

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-3: IVMUVF FORMULA

$$IVMUFV\ <9:0> = HEX\left(\frac{1024 \times Input\ undervoltage\ falling\ threshold}{40.96}\right)$$

6.6.9 IVMOVR REGISTER

Default value: 0xFC80

The IVMOVR register is a readable and writable register containing the value of the input overvoltage rising threshold.

REGISTER 6-9: IVMOVR: INPUT OVERVOLTAGE RISING REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
IVMOVR <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IVMOVR<9:2>:** MSB of the input overvoltage rising threshold

R/W-1	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMOVR <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IVMOVR<1:0>:** LSB of the of the input undervoltage rising threshold (see Equation 6-4)

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-4: IVMOVR FORMULA

$$IVMOVR\ <9:0> = HEX\left(\frac{1024 \times Input\ overvoltage\ rising\ threshold}{40.96}\right)$$

6.6.10 IVMOVF REGISTER

Default value: 0xFA00

The IVMOVF register is a readable and writable register containing the value of the input overvoltage falling threshold.

REGISTER 6-10: IVMOVF: INPUT OVERVOLTAGE FALLING REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0
IVMOVF <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IVMOVF<9:2>:** MSB of the input undervoltage falling threshold

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMOVF <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IVMOVF<1:0>:** LSB of the of the input undervoltage falling threshold

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-5: IVMOVF FORMULA

$$IVMOVF\ <9:0> = HEX\left(\frac{1024 \times Input\ overvoltage\ falling\ threshold}{40.96}\right)$$

6.6.11 IVMLDR REGISTER

Default value: 0xFC80

The IVMLDR register is a readable and writable register containing the value of the input load dump rising threshold.

REGISTER 6-11: IVMLDR: INPUT LOAD DUMP RISING REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
IVMLDR <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **IVMLDR<9:2>:** MSB of the input load dump rising threshold

R/W-1	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMLDR <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **IVMLDR<1:0>:** LSB of the of the input load dump threshold.

bit 5-0 **Unimplemented:** Read as ‘0’

EQUATION 6-6: IVMLDR FORMULA

$$IVMLDR\ \langle 9{:}0\rangle\ =\ HEX\left(\frac{1024 \times Input\ load\ dump\ rising\ threshold}{40.96}\right)$$

6.6.12 IVMLDF REGISTER

Default value: 0xFA00

The IVMUVF register is a readable and writable register containing the value of the input load dump falling threshold.

REGISTER 6-12: IVMLDF: INPUT LOAD DUMP FALLING REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0
IVMLDF <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IVMLDF<9:2>:** MSB of the input load dump falling threshold

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
IVMLDF <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IVMLDF<1:0>:** LSB of the of the input load dump falling threshold

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-7: IVMLDF FORMULA

$$IVMLDF\ \langle 9{:}0\rangle\ =\ HEX\left(\frac{1024 \times Input\ load\ dump\ falling\ threshold}{40.96}\right)$$

6.6.13 OVMUV REGISTER

Default value: 0x0A0F

The OVMUV register is a readable and writable register containing the value of the output undervoltage hysteresis and falling thresholds.

REGISTER 6-13: OVMUV: OUTPUT UNDERVOLTAGE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
OVMUVHY <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **OVMUVHY<7:0>:** Under voltage detection threshold hysteresis

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
OVMUVF <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **OVMUVF<7:0>:** Output undervoltage falling threshold.

EQUATION 6-8: OVMUVF FORMULA

$$OVMUVF\ \langle 7{:}0\rangle\ =\ HEX\left(\frac{VREF\ \langle 11{:}0\rangle - Output\ Undervoltage(\mathrm{V}) \times 100}{4}\right)$$

Example:
For the default value of 0x0A0F, output undervoltage is VREF – 0.6V.
0.6V = DEC(0x0F) × 4 × 10 mV

EQUATION 6-9: OVMUVHY FORMULA

$$OVMUVHY\ \langle 7{:}0\rangle\ =\ HEX\left(\frac{Output\ Undervoltage(\mathrm{V}) - Output\ Undervoltage\ Clear(\mathrm{V})}{4} \times 100\right)$$

Example:
For the default value of 0x0A0F, output undervoltage hysteresis is
0.4V = DEC(0x0A) × 4 × 10 mV

6.6.14 OVMOV REGISTER

Default value: 0x0AFE

The OVMOV register is a readable and writable register containing the value of the output overvoltage rising and hysteresis thresholds.

REGISTER 6-14: OVMOV: OUTPUT OVERVOLTAGE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
OVMOVHY <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **OVMOVHY<7:0>:** Overvoltage detection threshold hysteresis

R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
OVMOV <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **OVMOV<7:0>:** Over voltage detection set (rising) threshold.

EQUATION 6-10: OVMOV FORMULA

$$OVMOVR\ \langle 7{:}0\rangle\ =\ HEX\left(\frac{Output\ Overvoltage(\mathrm{V}) \times 100 - VREF\ \langle 11{:}0\rangle}{4}\right)$$

Example:
For the default value of `0xAFE`, output overvoltage is 10.16V + VREF.
10.16V = DEC(`0xFE`) × 4 × 10 mV

EQUATION 6-11: OVMOVHY FORMULA

$$OVMOVHY\ \langle 7{:}0\rangle\ =\ HEX\left(\frac{Output\ Overvoltage(\mathrm{V}) - Output\ Overvoltage\ Clear(\mathrm{V})}{4} \times 100\right)$$

Example:
For the default value of `0xAFE`, output overvoltage hysteresis is
0.4V = DEC(`0x0A`) × 4 × 10 mV

6.6.15 OCROCR REGISTER

Default value: 0xBE00

The OCROCR register is a readable and writable register containing the value of the output overcurrent rising threshold.

REGISTER 6-15: OCROCR: OUTPUT OVERCURRENT RISING THRESHOLD REGISTER

R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
OCROCR <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **OCROCR<9:2>:** MSB of the output overcurrent rising threshold

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
OCROCR <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **OCROCR<1:0>:** LSB of the of the output overcurrent rising threshold

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-12: OCROCR FORMULA

$$OCROCR\ \langle 9{:}0\rangle = HEX\left(I_{ocr}(\mathrm{mA}) \times \frac{R_{shunt}}{100(\mu\mathrm{V})}\right)$$

Example:

`0x2F8` = HEX(15200 mA × (5 mΩ/100 µV))

Resulting OCROCR register will be `0x2F8` << 6 = `0xBE00`

6.6.16 OCROCF REGISTER

Default value: 0xB900

The OCROCF register is a readable and writable register containing the value of the output overcurrent falling threshold.

REGISTER 6-16: OCROCF: OUTPUT OVERCURRENT FALLING THRESHOLD REGISTER

R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1
OCROCF <9:2>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **OCROCF<9:2>:** MSB of the output overcurrent falling threshold

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
OCROCF <1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **OCROCF<1:0>:** LSB of the of the output overcurrent falling threshold

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-13: OCROCF FORMULA

$$OCROCF\ \langle 9{:}0\rangle\ =\ HEX\left(I_{ocf}\,(\mathrm{mA}) \times \frac{R_{shunt}}{100(\mu\mathrm{V})}\right)$$

Example:

`0x2E4` = HEX(14800 mA × (5 mΩ/100 µV))

Resulting OCROCF register will be `0x2E4` << 6 = `0xB900`

6.6.17 VSAFECMP REGISTER

Default value: 0x0000

The VSAFECMP register is a readable and writable register for configuring the output discharge behavior.

REGISTER 6-17: VSAFECMP: VSAFE CMP EN REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **Unimplemented:** Read as ‘0’.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	VSAFECMP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **Unimplemented:** Read as ‘0’.

bit 0 **VSAFECMP:** Output discharge behavior
‘0’ = Output capacitors will be discharged for 600 ms, then discharge will stop
‘1’ = Output capacitors will be discharged down to VSAFE = 0.8V, then discharge will stop

6.6.18 VREF REGISTER

Default value: 0x1F43

The VREF register is a readable and writable register containing the value of the output voltage in 10 mV steps and the slope speed control bits.

REGISTER 6-18: VREF: OUTPUT VOLTAGE SETTING REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
VREF<11:4>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **VREF<11:4>:** MSB of the set output voltage in 10 mV resolution.

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
VREF <3:0>				VRAMP <3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **VREF<3:0>:** LSB of the of the output set voltage in 10mV resolution

bit 5-0 **VRAMP<3:0>:** Voltage ramp speed = number of PWM cycles to increase the output voltage by 10 mV

EQUATION 6-14: VREF FORMULA

$$VREF\ <11:0> = HEX(V_{out}\ (\mathrm{V}) \times 100)$$

Example:
For a value of 5V, HEX(5V × 100) = `0x1F4`.
Resulting VREF register will be `0x1F4X`, where X is the voltage ramp.

6.6.19 IREF REGISTER

Default value: 0xBB80

The IREF register is a readable and writable register containing the value of the output current in 5 mA steps for a shunt of 5 mΩ or 25 µV shunt voltage drop.

REGISTER 6-19: IREF: OUTPUT CURRENT SETTING REGISTER

R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1
IREF<11:4>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **IREF<11:4>:** MSB of the set output current

R/W-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
IREF <3:0>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IREF<3:0>:** LSB of the of the output set current (see Equation 6-15)

bit 5-0 **Unimplemented:** Read as '0'

EQUATION 6-15: IREF FORMULA

$$IREF\ <11:0> = HEX\left(I_{out}\ (\text{mA}) \times \frac{R_{shunt}\ (\text{m}\Omega)}{25(\mu\text{V})}\right)$$

Example:
For a value of 15A, HEX(15000 mA × (5 mΩ/25 µV)) = `0xBB8`.
Resulting IREF register will be `0xBB8` << 4 = `0xBB80`.

6.6.20 SWFRQCON1 REGISTER

Default value: 0x9200

The SWFRQCON1 is a readable and writable register used to program several parameters. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-20: SWFRQCON1: CONTROL REGISTER

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
SWFRQON	DITHER	—	DT<4:0>				
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15 **SWFRQON:** Switching frequency enable bit
`1` = Switching is enabled
`0` = All internal circuits are in reset state

bit 14 **DITHER:** Dither enable bit
`1` = Dithering is enabled
`0` = Dithering is disabled

bit 13 **Unimplemented:** Read as '`0`'

bit 12-8 **DT<4:0>:** Dead time in 3.5 ns steps

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Reserved							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **Reserved for future use**

6.6.21 SWFRQCON2 REGISTER

Default value: 0x004F

The SWFRQCON2 is a readable and writable register used to program the frequency and the phase of the switching. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-21: SWFRQCON2: FREQUENCY AND PHASE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASHIF <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **PHASHIF <7:0>:** Phase shift value bits (see Equation 6-16)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
SWFRQPR <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SWFRQPR <7:0>:** Switching period setting bits (see Equation 6-17)

EQUATION 6-16: PHASHIF FORMULA

$$PHASHIF\ <7:0> = HEX\left(\frac{Phase\ shift}{360°}\right) \times DEC(PLL\_PR + 1)$$

EQUATION 6-17: SWFRQPR FORMULA

$$SWFRQPR\ <7:0> = HEX\left(\frac{Switching\ period}{TCLK\ (\mathrm{ns})} - 1\right)$$

Where:

TCLK = the period of 36 MHz clock, 1/36 MHz = 27 ns

6.6.22 DITHER REGISTER

Default value: 0x003C.

The DITHER is a readable and writable register used to program the dithering and maximum duty cycle parameters. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-22: DITHER: DITHERING CONTROL REGISTER

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	DPS <2:0>			DOWNSLOP<2:0>			DITWAVE
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **DPS <2:0>:** Dithering postscaler counter setting. The postscaler values are:

000 = 1
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

bit 11-9 **DOWNSLOP <2:0>:** Downslope/upslope ratio, available only when the DITHWAVE = 1. The ratio is described in Equation 6-18.

bit 8 **DITWAVE:** Dithering wave selection bit:

0 = Triangular dithering wave
1 = Pseudo sawtooth dithering wave

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MAXDC <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **MAXDC<7:0>:** Maximum on time of duty cycle, can be calculated as shown in Equation 6-19.

EQUATION 6-18: DOWNSLOP FORMULA

$$DOWNSLOP\ <2:0>\ =\ HEX\left(\frac{down\_slope}{up\_slope} - 1\right)$$

EQUATION 6-19: MAXDC FORMULA

$$MAXDC\ <7:0> = HEX(Duty\ ratio \times (SWFRQPR + 1) \times TCLK(\text{ns}))$$

Where:

TCLK = the period of 36 MHz clock, 1/36 MHz = 27 ns

6.6.23 LC REGISTER

The LC register is a readable and writable register containing loop compensation LC parameter. This register cannot be modified while the MCP19061 is enabled.

Default value: 0x00A9.

Caution: Modifying this value affects the regulation loop stability!

REGISTER 6-23: LC

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	LC <11:8>			
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **LC<11:8>:** MSB of the LC loop compensation parameter

R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
LC <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LC<7:0>:** LSB of the of the LC loop compensation parameter

EQUATION 6-20: LC FORMULA

$$LC\ <11:0> = HEX(Inductor\ value(\mu\text{H}) \times 36)$$

Example:

For an inductor value of 4.7 µH, HEX(4.7 × 36) = 0xA9

6.6.24 IMSYS REGISTER

The IMSYS register is a readable and writable register containing the masks for the alert pin and the minimum alert interval set bits. A detected event will set the ALERT pin only if it is not masked. If two consecutive non-masked events are detected, the second one will set the ALERT pin only after the programmed interval after the previous alert. This register can't be modified while the MCP19061 is enabled.

Default value: 0x0000.

REGISTER 6-24: IMSYS

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VDDIOUVM	ADCREFUVM	VDD50UVM	AVDD40UVM	LOSECLKSYSM	LOSECLKPLLM	LOSESYNCM	DISCHFAILM
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15 **VDDIOUVM:** VDDIO undervoltage mask bit:
- 0 = ALERT will be set by the VDDIO undervoltage detection
- 1 = ALERT will not be set by the VDDIO undervoltage detection

bit 14 **ADCREFUVM:** ADC reference undervoltage mask bit
- 0 = ALERT will be set by the ADC reference undervoltage detection
- 1 = ALERT will not be set by the ADC reference undervoltage detection

bit 13 **VDD50UVM:** VDD undervoltage mask bit:
- 0 = ALERT will be set by the VDD undervoltage detection
- 1 = ALERT will not be set by the VDD undervoltage detection

bit 12 **AVDD40UVM:** Analog VDD undervoltage mask bit:
- 0 = ALERT will be set by the analog VDD undervoltage detection
- 1 = ALERT will not be set by the analog VDD undervoltage detection

bit 11 **LOSECLKSYSM:** 1.8 MHz clock lost mask bit
- 0 = ALERT will be set by the 1.8MHz clock lost detection
- 1 = ALERT will not be set by the 1.8MHz clock lost detection

bit 10 **LOSECLKPLLM:** 36 MHz clock lost mask bit
- 0 = ALERT will be set by the 36MHz clock lost detection
- 1 = ALERT will not be set by the 36MHz clock lost detection

bit 9 **LOSESYNCM:** External sync lost mask bit - only in sync mode
- 0 = ALERT will be set by the lost sync detection
- 1 = ALERT will not be set by the lost sync detection

bit 8 **DISCHFAILM:** Discharge failed mask bit
- 0 = ALERT will be set by the failed discharge detection
- 1 = ALERT will not be set by the failed discharge detection

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
UOLDM	—	—	—	—	ITRDLE <2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **UOLDM:** USB Overload Mask bit.

bit 6-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ITRDLE<2:0>:** ALERT minimum interval bits. Set the minimum value between two alerts in PWM cycles:

000 = 1
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

6.6.25 IMBB REGISTER

Default value: 0x0000.

The IMBB register is a readable and writable register containing the masks for the alert pin set bits. A detected event will set the ALERT pin only if it is not masked. This register cannot be modified while the MCP19061 is enabled.

REGISTER 6-25: IMBB: REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICMOCM	OCROCM	OCRREVCM	OCRSCM	VBSTUVM	OVTGDRM	OVTVDD50M	OVTAVDD40M
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15 **ICMOCM:** Input overcurrent mask bit
0 = ALERT will be set by the input overcurrent detection
1 = ALERT will not be set by the input overcurrent detection

bit 14 **OCROCM:** Output overcurrent mask bit
0 = ALERT will be set by the output overcurrent detection
1 = ALERT will not be set by the output overcurrent detection

bit 13 **OCRREVCM:** Output reverse current mask bit
0 = ALERT will be set by the output reverse current detection
1 = ALERT will not be set by the output reverse current detection

REGISTER 6-25: IMBB: REGISTER (CONTINUED)

bit 12 **OCRSCM:** Output short circuit mask bit
0 = ALERT will be set by the output short circuit detection
1 = ALERT will not be set by the output short circuit detection

bit 11 **VBSTUVM:** Bootstrap supplies undervoltage mask bit
0 = ALERT will be set by the bootstrap supplies undervoltage detection
1 = ALERT will not be set by the bootstrap supplies undervoltage detection

bit 10 **OVTGDRM:** Drivers overtemperature mask bit
0 = ALERT will be set by the drivers overtemperature detection
1 = ALERT will not be set by the drivers overtemperature detection

bit 9 **OVTVDD50M:** VDD regulator overtemperature mask bit
0 = ALERT will be set by the VDD regulator overtemperature detection
1 = ALERT will not be set by the VDD regulator overtemperature detection

bit 8 **OVTAVDD40M:** AVDD regulator overtemperature mask bit
0 = ALERT will be set by the AVDD regulator overtemperature detection
1 = ALERT will not be set by the AVDD regulator overtemperature detection

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IVMOVM	IVMUVM	IVMLDM	OVMOVM	OVMUVM	OVMZVM	PLLPRFM	CRCERRM
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **IVMOVM:** Input overvoltage mask bit
0 = ALERT will be set by the input overvoltage detection
1 = ALERT will not be set by the input overvoltage detection

bit 6 **IVMUVM**: Input undervoltage mask bit
0 = ALERT will be set by the input undervoltage detection
1 = ALERT will not be set by the input undervoltage detection

bit 5 **IVMLDM:** Input load dump mask bit
0 = ALERT will be set by the input load dump detection
1 = ALERT will not be set by the input load dump detection

bit 4 **OVMOVM:** Output overvoltage mask bit
0 = ALERT will be set by the output overvoltage detection
1 = ALERT will not be set by the output overvoltage detection

bit 3 **OVMUVM:** Output undervoltage mask bit
0 = ALERT will be set by the output undervoltage detection
1 = ALERT will not be set by the output undervoltage detection

bit 2 **OVMZVM:** Output vsafe0 mask bit
0 = ALERT will be set by the output vsafe0 detection
1 = ALERT will not be set by the output vsafe0 detection

bit 1 **PLLPRFM:** PLL PR counter fail mask bit
0 = ALERT will be set by the PLL PR counter fail detection
1 = ALERT will not be set by the PLL PR counter fail detection

bit 0 **CRCERRM:** NVM CRC check fail
0 = ALERT will be set by the NVM CRC check fail detection
1 = ALERT will not be set by the NVM CRC check fail detection

6.6.26 ADCON REGISTER

Default value: 0x3700.

The ADCON register is a readable and writable register containing voltage conversion control bits. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-26: ADCON: VOLTAGES CONVERSION CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ADCMANDLY <7:0>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-18 **ADCMANDLY <7:0>:** Output voltage errors detection latency bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = Reserved
111 = Reserved

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	OCRADCON	OCMADCON	OVMADCON	IVMADCON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OCRADCON:** Output current reporter ADC control bit
0 = Output current reporter ADC disabled
1 = Output current reporter ADC enabled

bit 2 **OCMADCON:** Output current monitor ADC control bit
0 = Output current monitor ADC disabled
1 = Output current monitor ADC enabled

bit 1 **OVMADCON:** Output voltage monitor ADC control bit
0 = Output voltage monitor ADC disabled
1 = Output voltage monitor ADC enabled

bit 0 I**VMADCON:** Input voltage monitor ADC control bit
0 = Input voltage monitor ADC disabled
1 = Input voltage monitor ADC enabled

6.6.27 USBOLD REGISTER

The USBOLD register is a readable and writable register containing overload setting bits.

USBOLD register can be calculated as follows:

- For 1A overload condition,
  USBOLD = CA0Ah = 11 0010100 0001010 b,
  with factor = 20 multiplied by base = 50 mA.
- For 3A overload condition,
  USBOLD = DE0Ah = 11 0111100 0001010 b, with factor = 60 multiplied by base = 50 mA

Default value: 0x0000

REGISTER 6-27: USBOLD: OVERLOAD CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
USB_CLASS <1:0>		USB_FACTOR <6:1>					
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-14 **USB_CLASS <1:0>:** USB PD overload class set bits
00 = class 0 (no overload)
01 = class 1
10 = class 2
11 = class 3

bit 13-8 **USB_FACTOR <6:1>:** Set current in USB_BASE steps; most significant bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
USB_FACTOR <0>	USB_BASE <6:0>						
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **USB_FACTOR <0>:** Set current in USB_BASE steps; least significant bit

bit 6-0 **USB_BASE <6:0>:** Set USB overload current resolution in 25 µV output shunt voltage steps

6.6.28 IVMCNT REGISTER

Default value: 0x0000

The IVMCNT register is a readable and writable register containing the input voltage errors persistence control bits. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-28: IVMCNT: INPUT VOLTAGE ERROR PERSISTENCE REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
IVMUVCNT <2:0>			—	—	IVMLDCNT <2:0>		
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-13 **IVMUVCNT <2:0>:** Input undervoltage error detection latency bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **IVMLDCNT <2:0>:** Load dump error detection latency bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
IVMOVCNT <2:0>			—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 7-5 **IVMOVCNT <2:0>:** Input overvoltage error detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 4-0 **Unimplemented:** Read as '0'

6.6.29 OVMVCNT1 REGISTER

Default value: 0x0000

The OVMVCNT1 register is a readable and writable register containing the output under / overvoltage detection latency counter setting bits. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-29: OVMVCNT1: OUTPUT VOLTAGE ERROR PERSISTENCE REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
OVMUVCNT <2:0>			—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-13 **OVMUVCNT <2:0>:** Output undervoltage error detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 12-8 **Unimplemented:** Read as '0'

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
OVMOVCNT <2:0>			—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **OVMOVCNT <2:0>:** Output overvoltage error detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 4-0 **Unimplemented:** Read as '0'

6.6.30 OVMVCNT2 REGISTER

Default value: 0x0000

The OVMVCNT2 register is a readable and writable register containing output voltage detection persistence counters setting bits. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-30: OVMVCNT2: OUTPUT VOLTAGE PERSISTENCE REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
OVM2VCNT <2:0>			—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-13 **OVM2VCNT <2:0>:** Output 2V short circuit threshold detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 12-8 **Unimplemented:** Read as '0'

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
OVMSFCNT <2:0>			—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **OVMSFCNT <2:0>:** Output vsafe0 detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 4-0 **Unimplemented:** Read as '0'

6.6.31 CCNT REGISTER

Default value: 0x1007

The CCNT register is a readable and writable register containing current errors detection set bits. This register cannot be modified while the MCP19061 is enabled.

REGISTER 6-31: CCNT: CURRENT ERRORS REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ICMOCCNT <2:0>			ICMOCSEL <4:0>				
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 15-13 **ICMOCCNT <2:0>:** Input overcurrent detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 12-8 **ICMOCSEL <4:0>:** Input overcurrent detection threshold bits**.** Current detection threshold is calculated as shown in Equation 6-21.

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-1	R/W-1	R/W-0
OCROCCNT <2:0>			—	—	OCRREVCCNT <2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 7-5 **OCROCCNT <2:0>:** Output overcurrent detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **OCRREVCCNT <2:0>:** Output reverse current detection persistence bits
000 = 1 conversion
001 = 2 conversions
010 = 4 conversions
011 = 8 conversions
100 = 16 conversions
101 = 32 conversions
110 = reserved
111 = reserved

EQUATION 6-21: ICMOCSEL FORMULA

$$ICMOCSEL\ <4:0> = HEX\left(\frac{Input\ Overcurrent\ Threshold\ (\mathrm{A}) \times 32 \times R_{shunt}\ (\mathrm{m\Omega})}{1218\ (\mathrm{mA})}\right)$$

Note: In the formula, 1LSB = 7.6A when R_{shunt} = 5 mΩ.

6.6.32 COMPMODE REGISTER

Default value: 0x0307

The COMPMODE register is a readable and writable register containing several driver setting bits. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-32: COMPMODE: DRIVING REGISTER

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
HIDIS	LODIS	—	—	—	—	Reserved	
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15 **HIDIS:** High side drivers disable bit
0 = High side drivers are enabled
1 = High side drivers are disabled (high impedance)

bit 14 **LODIS:** Low side drivers disable bit
0 = Low side drivers are enabled
1 = Low side drivers are disabled (high impedance)

bit 13-10 **Unimplemented:** Read as '0'

bit 9-8 **Reserved:** Read as '1'; **Do not clear these bits!**

U-0	U-0	U-0	U-0	U-0	R/W-1	R-1	R/W-1
—	—	—	—	—	Reserved	VREGEN	IREGEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **RESERVED:** Read as '1'; **Do not clear this bit!**

bit 1 **VREGEN:** Voltage regulation bit
1 = Read as '1'; Voltage regulation is always enabled

bit 0 **IREGEN:** Current regulation enable bit
0 = Current regulation is disabled
1 = Current regulation is enabled

6.6.33 EVSTOP REGISTER

Default value: 0x0000

The EVSTOP register is a readable and writable register containing the bits defining what events will stop the power train. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-33: EVSTOP: EVENT STOP REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ORCST
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **ORCST:** Output reverse current stop enable bit
0 = Reverse current event will not stop the power train
1 = Reverse current event will stop the power train

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOVST	IUVST	OOVST	OUVST	IOCST	OOCST	OSHCST	UOLDST
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n = Value at POR

bit 7 **IOVST:** Input overvoltage stop enable bit
0 = Input overvoltage event will not stop the power train
1 = input overvoltage event will stop the power train

bit 6 **IUVST:** Input undervoltage stop enable bit
0 = Input undervoltage event will not stop the power train
1 = Input undervoltage event will stop the power train

bit 5 **OOVST:** Output overvoltage stop enable bit
0 = Output overvoltage event will not stop the power train
1 = Output overvoltage event will stop the power train

bit 4 **OUVST:** Output undervoltage stop enable bit
0 = Output undervoltage event will not stop the power train
1 = Output undervoltage event will stop the power train

bit 3 **IOCST:** Input overcurreent stop enable bit
0 = Input overcurrent event will not stop the power train
1 = Input overcurrent event will stop the power train

bit 2 **OOCST:** Output overcurrent stop enable bit
0 = Output overcurrent event will not stop the power train
1 = Output overcurrent event will stop the power train

bit 1 **OSHCST:** Output short-circuit stop enable bit
0 = Output short-circuit event will not stop the power train
1 = Output short-circuit event will stop the power train

bit 0 **UOLDST:** Overload stop enable bit
0 = Overload event will not stop the power train
1 = Overload event will stop the power train

6.6.34 MODECON REGISTER

Default value: 0x0101

The MODECON register is a readable and writable register containing several configuration bits.

REGISTER 6-34: MODECON: MODE SET REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	MANUDSCH	AUTODSCH
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **MANUDSCH:** Manual discharge bit. Set high to start a discharge cycle. The bit will automatically reset when the discharge is finished. It is available only if AUTODSCH bit = 0.

bit 8 **AUTODSCH:** Automatic discharge bit
0 = Stopping the power train will not initiate an output capacitor discharge
1 = Stopping the power train will initiate an output capacitor discharge

U-0	U-0	U-0	U-0	U-0	U-0	R-0	R/W-0
—	—	—	—	—	—	DOPM <1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **DOPM <1:0>:** Device operating mode bits
00 = Discharge Fault mode (read only)
01 = Standby mode
10 = Normal mode
11 = Discharge mode (read only)

Note: If the **ENABLE** pin is set to high, **DOPM** bits will read 02 (Normal mode) and writing 01 will have no effect.

6.6.35 PLLCON REGISTER

The PLLCON register is a readable and writable register containing switching clock configuration. This register can't be modified while the MCP19061 is enabled or any time dependent function is activated.

To modify it, the SYNC pin shall not be configured as output and the ADC reading in disable state must be deactivated.

Default value: 0x014F.

REGISTER 6-35: PLLCON: PLL CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
—	—	—	—	—	AUTORVB	CLKOUTEN	CLKSRC
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **AUTORVB:** Clock auto-revert bit
0 = The device will not revert to internal clock if synchronization is lost
1 = The device will revert to internal clock if synchronization is lost

bit 9 **CLKOUTEN:** Clock output enable bit.
0 = The SYNC pin is disabled
1 = The switching frequency is output on the SYNC pin. Available only if CLKSRC = 1.

bit 8 **CLKSRC:** PLL input selection pin.
0 = The PLL input is the SYNC pin
1 = The PLL input is the internal 450KHz

R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
PLLPR <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PLLPR <7:0>:** Switching period counter.

6.6.36 DEVID REGISTER

Default value: 0x0151

The DEVID register is a readable and writable register containing the device I^2C settings. This register can't be modified while the MCP19061 is enabled.

REGISTER 6-36: DEVID: I2C ADDRESS SETTING REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ADR0EN
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **ADR0EN:** I2C address selection pin.
'0' = The I2C address is set internally using DEVID<4:0>.
'1' = The I2C address is set via the ADR0 pin

U-0	R-1	R-0	R-1	R/W-0	R/W-0	R/W-0	R/W-0
—	1	0	1	DEVID <3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **Read only:** Read as '1'

bit 5 **Read only:** Read as '0'

bit 4 **Read only:** Read as '1'

bit 3-0 **DEVID <3:0>:** Together with the previous two bits, this will be the I2C address of the chip.

TABLE 6-2: I^2C ADDRESS RESISTOR SELECTION

R address (kΩ) MIN	R address (kΩ) MAX	DEVID <3:0> 4LSB (hex)	I2C Addr (hex)
0	2.56	0	50
2.56	5.12	1	51
5.12	7.68	2	52
7.68	10.24	3	53
10.24	12.8	4	54
12.8	15.36	5	55
15.36	17.92	6	56
17.92	20.48	7	57
20.48	23.04	8	58
23.04	25.6	9	59
25.6	28.16	A	5A
28.16	30.72	B	5B

TABLE 6-2: I²C ADDRESS RESISTOR SELECTION (CONTINUED)

30.72	33.28	C	5C
33.28	35.84	D	5D
35.84	38.4	E	5E
38.4	40.96	F	5F

6.6.37 GPRA REGISTER

Default value: 0x0000

The GPRA register is a readable and writable register. The user may store the desired information in this register. The GPRA register content is not saved in the NVM.

REGISTER 6-37: GPRA: USER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRA <15:8>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **GPRA <15:8>:** General purpose user register A

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRA <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **GPRA <7:0>:** General purpose user register A

6.6.38 GPRB REGISTER

Default value: 0x0000

The GPRB register is a readable and writable register. The user may store the desired information in this register. The GPRB register content is not saved in the NVM.

REGISTER 6-38: GPRB: USER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRB <15:8>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **GPRB <15:8>:** General purpose user register B

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRB <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **GPRB <7:0>:** General purpose user register B

6.6.39 GPRC REGISTER

Default value: 0x0000

The GPRC register is a readable and writable register. The user may store the desired information in this register. The GPRC register content is not saved in the NVM.

REGISTER 6-39: GPRC: USER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRC <15:8>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **GPRC <15:8>:** General purpose user register C

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRC <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **GPRC <7:0>:** General purpose user register C

6.6.40 GPRD REGISTER

Default value: 0x0000

The GPRD register is a readable and writable register. The user may store the desired information in this register. The GPRD register content is not saved in the NVM.

REGISTER 6-40: GPRD: USER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRD <15:8>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **GPRD <15:8>:** General purpose user register D

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPRD <7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **GPRD <7:0>:** General purpose user register D

6.6.41 STASYS REGISTER

The STASYS register is a readable and deletable register containing the system status bits. The status bits are set by the event detect state machine and can be cleared by the user. To clear a status bit, the user must write “1” in it’s location.

REGISTER 6-41: STASYS: SYSTEM STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VDDIOUV	ADCREFUV	VDD50UV	AVDD40UV	LOSECLKSYS	LOSECLKPLL	LOSESYNC	DISCHFAIL
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15 **VDDIOUV:** VDD_IO undervoltage bit
0 = No VDD_IO undervoltage was detected
1 = VDD_IO undervoltage was detected

bit 14 **ADCREFUV:** AD reference undervoltage bit
0 = No AD reference undervoltage was detected
1 = AD reference undervoltage was detected

bit 13 **VDD50UV:** VDD 5V undervoltage bit
0 = No 5V VDD undervoltage was detected
1 = 5V VDD undervoltage was detected

bit 12 **AVDD40UV:** Analog 4V supply undervoltage bit
0 = No analog 4V supply undervoltage was detected
1 = Analog 4V supply undervoltage was detected

bit 11 **LOSECLKSYS:** System clock fail bit
0 = No clock lost was detected
1 = System clock lost was detected

bit 10 **LOSECLKPLL:** PLL fail bit
0 = No PLL clock lost was detected
1 = PLL lost clock was detected

bit 9 **LOSESYNC:** Synchronization lost bit
0 = No synchronization lost was detected
1 = Synchronization lost was detected

bit 8 **DISCHFAIL:** Output discharge failed bit
0 = No output discharge fail was detected
1 = Output discharge fail was detected

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0
UOLD	—	—	SUFAIL	ACDONE	SUDONE	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **UOLD:** USB overload detected bit
0 = No USB overload was detected
1 = USB overload was detected

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **SUFAIL:** Startup fail bit
0 = Startup succeeded
1 = Startup was not properly completed

bit 3 **ACDONE:** AD conversion done bit
0 = The AD conversion is in process
1 = The AD conversion is completed

bit 2 **SUDONE:** Startup completed bit
0 = Startup not completed
1 = Startup completed

bit 1-0 **Unimplemented:** Read as ‘0’

6.6.42 STABB REGISTER

The STABB register is a readable and deletable register containing buck-boost related status bits. The status bits are set by the event detect state machine and can be cleared by the user. To clear a status bit, the user must write “1” to that location.

REGISTER 6-42: STABB: BUCK-BOOST STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICMOC	OCROC	OCRREVC	OCRSC	VBSTUV	OVTGDR	OVTVDD50	OVTAVDD40
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15 **ICMOC:** Input overcurrent detected bit
0 = No input overcurrent was detected
1 = Input overcurrent was detected

bit 14 **OCROC:** Output overcurrent detected bit
0 = No output overcurrent was detected
1 = Output overcurrent was detected

bit 13 **OCRREVC:** Output reverse current detected bit
0 = No output reverse current was detected
1 = Output reverse current was detected

REGISTER 6-42: STABB: BUCK-BOOST STATUS REGISTER (CONTINUED)

bit 12 **OCRSC:** Output short circuit detected bit
0 = No output short circuit was detected
1 = Output short circuit was detected

bit 11 **VBSTUV:** Bootstrap supplies undervoltage detected bit
0 = No bootstrap supplies undervoltage was detected
1 = Bootstrap supplies undervoltage was detected

bit 10 **OVTGDR:** Gate drivers overtemperature detect bit
0 = No gate drivers overtemperature was detected
1 = Gate drivers overtemperature was detected

bit 9 **OVTVDD50:** VDD regulator overtemperature detect bit
0 = No 5V VDD regulator overtemperature was detected
1 = 5V VDD regulator overtemperature was detected

bit 8 **OVTAVDD40:** Analog VDD regulator overtemperature detect bit
0 = No 4V analog VDD regulator overtemperature was detected
1 = 4V analog VDD regulator overtemperature was detected

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IVMOV	IVMUV	IVMLD	OVMOV	OVMUV	OVMZV	PLLPRF	CRCERR
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **IVMOV:** Input overvoltage detected bit
0 = No input overvoltage was detected
1 = Input overvoltage was detected

bit 6 **IVMUV:** Input undervoltage detected bit
0 = No input undervoltage was detected
1 = Input undervoltage was detected

bit 5 **IVMLD:** Input load dump detected bit
0 = No input load dump was detected
1 = Input load dump was detected

bit 4 **OVMOV:** Output overvoltage detected bit
0 = No output overvoltage was detected
1 = Output overvoltage was detected

bit 3 **OVMUV:** Output undervoltage detected bit
0 = No output undervoltage was detected
1 = Output undervoltage was detected

bit 2 **OVMZV:** Output vsafe0 detected bit
0 = No output vsafe0 was detected
1 = Output vsafe0 was detected

bit 1 **PLLPRF:** PLL PR register changed bit
0 = No attempt to modify the PLL PR register while running detected
1 = PLL PR register was modified while running

bit 0 **CRCERR:** NVM CRC error bit
0 = No NVM CRC error was detected
1 = NVM CRC is wrong

6.6.43 NVMSTAT REGISTER

The NVMSTAT register is a readable and deletable register containing the NVM status bits. The status bits are set by the event detect state machine and can be cleared by the user. To clear a status bit, the user must write "1" to that location.

REGISTER 6-43: NVMSTAT: NVM STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-8 **Unimplemented:** Read as '0'

U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	NVMFAIL	BUSY	CRCCALOK	CRCCALF	CRCCONFOK	CRCCONFF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **NVMFAIL:** NVM fail bit
0 = NVM OK
1 = NVM is faulty

bit 4 **BUSY:** Device busy bit
0 = NVM can be accessed
1 = NVM is busy

bit 3 **CRCCALOK:** Calibration registers CRC good bit
0 = Calibration CRC is wrong
1 = Calibration CRC is correct

bit 2 **CRCCALF:** Calibration registers CRC failed bit
0 = Calibration CRC is correct
1 = Calibration CRC is wrong

bit 1 **CRCCONFOK:** Configuration registers CRC good bit
0 = Configuration CRC is wrong
1 = Configuration CRC is correct

bit 0 **CRCCONFF:** Configuration registers CRC failed bit
0 = Configuration CRC is correct
1 = Configuration CRC is wrong

6.6.44 RFLAG REGISTER

The RFLAG register is a readable and deletable register containing regulation mode status bits.

REGISTER 6-44: RFLAG: REGULATION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **Unimplemented:** Read as ‘0’

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	VRFLAG	IRFLAG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **VRFLAG:** Voltage regulation bit
- 0 = The device is not regulating the voltage
- 1 = Voltage regulation loop is closed

bit 0 **IRFLAG:** Current regulation bit
- 0 = The device is not regulating the current
- 1 = Current regulation loop is closed

6.6.45 IVMOUT REGISTER

The IVMOUT register is a readable register containing voltage error comparator bits.

REGISTER 6-45: IVMOUT: VOLTAGE COMPARATORS REGISTER

U-0	U-0	R-x	U-0	R-x	R-x	U-0	U-0
—	—	SIVMLD	—	MIVMLDR	MIVMLDF	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **SIVMLD:** Load dump not latched detected bit
0 = Not latched load dump event not detected
1 = Not latched load dump event detected

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **MIVMLDR:** Mirrored load dump rising threshold bit
0 = Input corrected measured voltage is below the load dump rising detection threshold
1 = Input corrected measured voltage is above the load dump rising detection threshold

bit 10 **MIVMLDF:** Mirrored load dump falling threshold bit
0 = Input corrected measured voltage is above the load dump falling detection threshold
1 = Input corrected measured voltage is below the load dump falling detection threshold

bit 9-8 **Unimplemented:** Read as ‘0’

U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
—	—	SIVMOV	SIVMUV	MIVMOVR	MIVMOVF	MIVMUVR	MIVMUVF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **SIVMOV:** Input overvoltage not latched detected bit
0 = Not latched input overvoltage event not detected
1 = Not latched input overvoltage event detected

bit 4 **SIVMUV:** Input undervoltage not latched detected bit
0 = Not latched input undervoltage event not detected
1 = Not latched input undervoltage event detected

bit 3 **MIVMOVR:** Mirrored input overvoltage rising threshold bit
0 = Input corrected measured voltage is below the input overvoltage rising detection threshold
1 = Input corrected measured voltage is above the input overvoltage rising detection threshold

bit 2 **MIVMOVF:** Mirrored input overvoltage falling threshold bit
0 = Input corrected measured voltage is above the input overvoltage falling detection threshold
1 = Input corrected measured voltage is below the input overvoltage falling detection threshold

IVMOUT: Voltage comparators register (Continued)

bit 1 **MIVMUVR:** Mirrored input undervoltage rising threshold bit
0 = Input corrected measured voltage is below the input undervoltage rising detection threshold
1 = Input corrected measured voltage is above the input undervoltage rising detection threshold

bit 0 **MIVMUVF:** Mirrored input undervoltage falling threshold bit
0 = Input corrected measured voltage is above the input undervoltage falling detection threshold
1 = Input corrected measured voltage is below the input undervoltage falling detection threshold

6.6.46 OOUT1 REGISTER

The OOUT1 register is a readable register containing the output voltage and current comparators bits.

REGISTER 6-46: OOUT1: OUTPUT VOLTAGE AND CURRENT COMPARATORS REGISTER

U-0	U-0	R-x	R-x	R-x	R-x	U-0	U-0
—	—	SOCROC	SOCRREVC	MOCROCR	MOCROCF	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SOCROC:** Output overcurrent not latched detected bit
0 = Not latched output overcurrent event not detected
1 = Not latched output overcurrent event detected

bit 12 **SOCRREVC:** Output reverse current not latched detected bit
0 = Not latched output reverse current event not detected
1 = Not latched output reverse current event detected

bit 11 **MOCROCR:** Mirrored output overcurrent rising threshold bit
0 = Output corrected measured current is below the output overcurrent rising detection threshold
1 = Output corrected measured current is above the output overcurrent rising detection threshold

bit 10 **MOCROCF:** Mirrored output overcurrent falling threshold bit
0 = Output corrected measured current is above the output overcurrent falling detection threshold
1 = Output corrected measured current is below the output overcurrent falling detection threshold

bit 9-8 **Unimplemented:** Read as '0'

U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
—	—	SOVMOV	SOVMUV	MOVMOVR	MOVMOVF	MOVMUVR	MOVMUVF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **SOVMOV:** Output overvoltage not latched detected bit
0 = Not latched output overvoltage event not detected
1 = Not latched output overvoltage event detected

OOUT1: Output voltage and current comparators register (Continued)

bit 4 **SOVMUV:** Output undervoltage not latched detected bit
0 = Not latched output undervoltage event not detected
1 = Not latched output undervoltage event detected

bit 3 **MOVMOVR:** Mirrored output overvoltage rising threshold bit
0 = Output corrected measured voltage is below the output overvoltage rising detection threshold
1 = Output corrected measured voltage is above the output overvoltage rising detection threshold

bit 2 **MOVMOVF:** Mirrored output overvoltage falling threshold bit
0 = Output corrected measured voltage is above the output overvoltage falling detection threshold
1 = Output corrected measured voltage is below the output overvoltage falling detection threshold

bit 1 **MOVMUVR:** Mirrored output undervoltage rising threshold bit
0 = Output corrected measured voltage is below the output undervoltage rising detection threshold
1 = Output corrected measured voltage is above the output undervoltage rising detection threshold

bit 0 **MOVMUVF:** Mirrored output undervoltage falling threshold bit
0 = Output corrected measured voltage is above the output undervoltage falling detection threshold
1 = Output corrected measured voltage is below the output undervoltage falling detection threshold

6.6.47 OOUT2 REGISTER

The OOUT2 register is a readable register containing several output voltage level comparators bits.

REGISTER 6-47: OOUT2: OUTPUT VOLTAGE COMPARATORS REGISTER

U-0	U-0	R-x	U-0	U-0	U-0	R-x	R-x
—	—	SOVM2V	—	—	—	MOVM2VR	MOVM2VF
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **SOVM2V:** Output under 2V not latched detected bit
0 = Not latched output voltage below 2V event not detected
1 = Not latched output voltage below 2V event detected

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **MOVM2VR:** Mirrored output voltage below 2V rising threshold bit
0 = Output corrected measured voltage is above the 2V rising detection threshold
1 = Output corrected measured voltage is below the 2V rising detection threshold

bit 8 **MOVM2VF:** Mirrored output voltage below 2V falling threshold bit
0 = Output corrected measured voltage is above the 2V falling detection threshold
1 = Output corrected measured voltage is below the 2V falling detection threshold

U-0	U-0	R-x	U-0	U-0	U-0	R-x	R-x
—	—	SOVMSF	—	—	—	MOVMSFR	MOVMSFF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **SOVMSF:** Output vsafe0 not latched detected bit
0 = Not latched output vsafe0 event not detected
1 = Not latched output vsafe0 event detected

bit 4-2 **Unimplemented:** Read as ‘0’

bit 1 **MOVMSFR:** Mirrored output voltage below vsafe0 rising threshold bit
0 = Output corrected measured voltage is below the vsafe0 rising detection threshold
1 = Output corrected measured voltage is above the vsafe0 rising detection threshold

bit 0 **MOVMSFF:** Mirrored output voltage below vsafe0 falling threshold bit
0 = Output corrected measured voltage is above the vsafe0 falling detection threshold
1 = Output corrected measured voltage is below the vsafe0 falling detection threshold

6.6.48 OVTSTAT REGISTER

The OVTSTAT register is a readable register containing the status of the overtemperature shutdown flags. These flags are set by the overtemperature detection and are reset by setting the corresponding bit to ‘1’ in the STABB Register 6-42.

REGISTER 6-48: OVTSTAT: OVERTEMPERATURE SHUTDOWN STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **Unimplemented:** Read as ‘0’

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	OVTSDGDR <1:0>		OVTSDVDD	OVTSDAVDD	OVTSDDVDD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **OVTSDGD_BST:** Boost leg gate driver overtemperature shutdown status

bit 3 **OVTSDGD_BCK:** Buck leg gate driver overtemperature shutdown status

bit 2 **OVTSDVDD:** VDD50 regulator overtemperature shutdown status

bit 1 **OVTSDAVDD:** AVDD40 regulator overtemperature shutdown status

bit 0 **OVTSDDVDD:** DVDD18 regulator overtemperature shutdown status

6.6.49 IVMCORRES REGISTER

The IVMCORRES register is a readable register containing corrected input voltage measured value.

REGISTER 6-49: IVMCORRES: CORRECTED INPUT VOLTAGE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
IVMCORRES <11:4>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **IVMCORRES <11:4>:** Most significant bits of the corrected input voltage

R-x	R-x	R-x	R-x	U-0	U-0	U-0	U-0
IVMCORRES <3:0>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **IVMCORRES <3:0>:** Least significant bits of the corrected input voltage

bit 3-0 **Unimplemented:** Read as ‘0’

EQUATION 6-22: V_{IN} FORMULA

$$V_{in}\,(\mathrm{V}) = \frac{DEC(IVMCORRES\,\langle 11{:}0\rangle)}{100}$$

6.6.50 OVMCORRES REGISTER

The OVMCORRES register is a readable register containing corrected output voltage measured value.

REGISTER 6-50: OVMCORRES: CORRECTED OUTPUT VOLTAGE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
OVMCORRES <11:4>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **OVMCORRES <11:4>:** Most significant bits of the corrected output voltage

R-x	R-x	R-x	R-x	U-0	U-0	U-0	U-0
OVMCORRES <3:0>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **OVMCORRES <3:0>:** Least significant bits of the corrected output voltage

bit 3-0 **Unimplemented:** Read as ‘0’

EQUATION 6-23: V_{OUT} FORMULA

$$V_{out}\,(\mathrm{V}) = \frac{DEC(OVMCORRES\,\langle 11{:}0\rangle)}{100}$$

6.6.51 OCRCORRES REGISTER

The OCRCORRES register is a readable register containing the corrected value of output current.

REGISTER 6-51: OCRCORRES: CORRECTED OUTPUT CURRENT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
OCRCORRES <11:4>							
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 15-8 **OCRCORRES <11:4>:** Most significant 8 bits of the corrected output current

R-x	R-x	R-x	R-x	U-0	U-0	U-0	U-0
OCRCORRES <3:0>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **OCRCORRES <3:0>:** Least significant 8 bits of the corrected output current

bit 3-0 **Unimplemented:** Read as ‘0’

EQUATION 6-24: I_{OUT} FORMULA

$$I_{out}\,(\mathrm{mA}) = (DEC(OCRCORRES\,\langle 11{:}0\rangle) - 1024) \times \frac{25(\mu\mathrm{V})}{R_{shunt}\,(\mathrm{m}\Omega)}$$

6.6.52 NVMCTRL REGISTER

The NVMCTRL register is a readable and writable register, which contains several bits used to control the NVM access.

REGISTER 6-52: NVMCTRL: NVM CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	x = Bit is unknown	‘0’ = Bit is cleared
‘1’ = Bit is set		

bit 15-8 **Unimplemented:** Read as ‘0’

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RSTART	WSTART
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **RSTART:** Set to initiate configuration restore from NVM bit. Self resets after the operation is completed.

bit 0 **WSTART:** Set to initiate save configuration in NVM bit. Self resets after the operation is completed.

6.6.53 ADCGO REGISTER

The ADCGO register is a readable and writable register containing the ADC start parameters. Starting a conversion is done as follows:

- ensure the power train is stopped (**MODECON.DOPM** is 01)
- configure **ADCON**
- configure **ADCGO**
- start power train (**MODECON.DOPM** is 02)
- start the conversion by reading the register set with **ADCGO.ASSEL** bits
- read any of the configured ADC register (**IVMCORRES**, **OVMCORRES**, **OCMCORRES**, **OCRCORRES**)

Note: The first reading, used in triggering the conversion should be discarded.

REGISTER 6-53: ADCGO: ADC START PARAMETERS

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	x = Bit is unknown	'0' = Bit is cleared
'1' = Bit is set		

bit 15-8 **Unimplemented:** Read as '0'

U-1	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
—	ASSEL <1:0>		—	—	—	CTS	GO
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '1'

bit 6-5 **ASSEL<1:0>:** Automatic sampling select
- 00 = IVMCORRES
- 01 = OVMCORRES
- 10 = OCMCORRES
- 11 = OCRCORRES

bit 4-2 **Unimplemented:** Read as '0'

bit 1 **CTS:** Conversion Trigger Configuration bit
- 1 = Manual trigger
- 0 = Automatic trigger

bit 0 **GO:** Conversion Status bit
- 0 = Conversion not in progress
- 1 = Conversion in progress

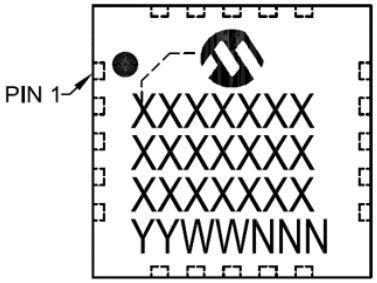
TABLE 6-3: EXAMPLE OF ADC READING SEQUENCE

Register	Command	Value	Observations
MODECON	WRITE	101	*# Stop switching*
ADCON	WRITE	370F	*# Enable all ADCs*
ADCGO	WRITE	81	*# Select IVMCORRES as trigger*
MODECON	WRITE	102	*# Start switching*
IVMCORRES	READ	0x00	*# Discard first reading*
IVMCORRES	READ	0x4F50	*# Input Voltage = 12.6V*
IVMCORRES	READ	0x4F40	
OVMCORRES	READ	0x1F30	*# Output Voltage = 5V*
OVMCORRES	READ	0x1F30	
OCRCORRES	READ	0x4B60	*# Output current ~1A*
OCRCORRES	READ	0x4B60	

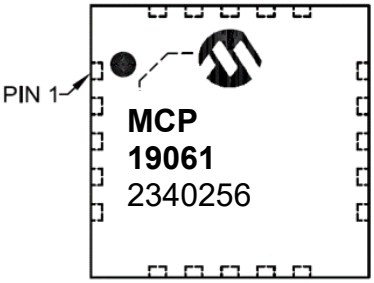
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

32-Lead VQFN (5x5x1 mm)



Example

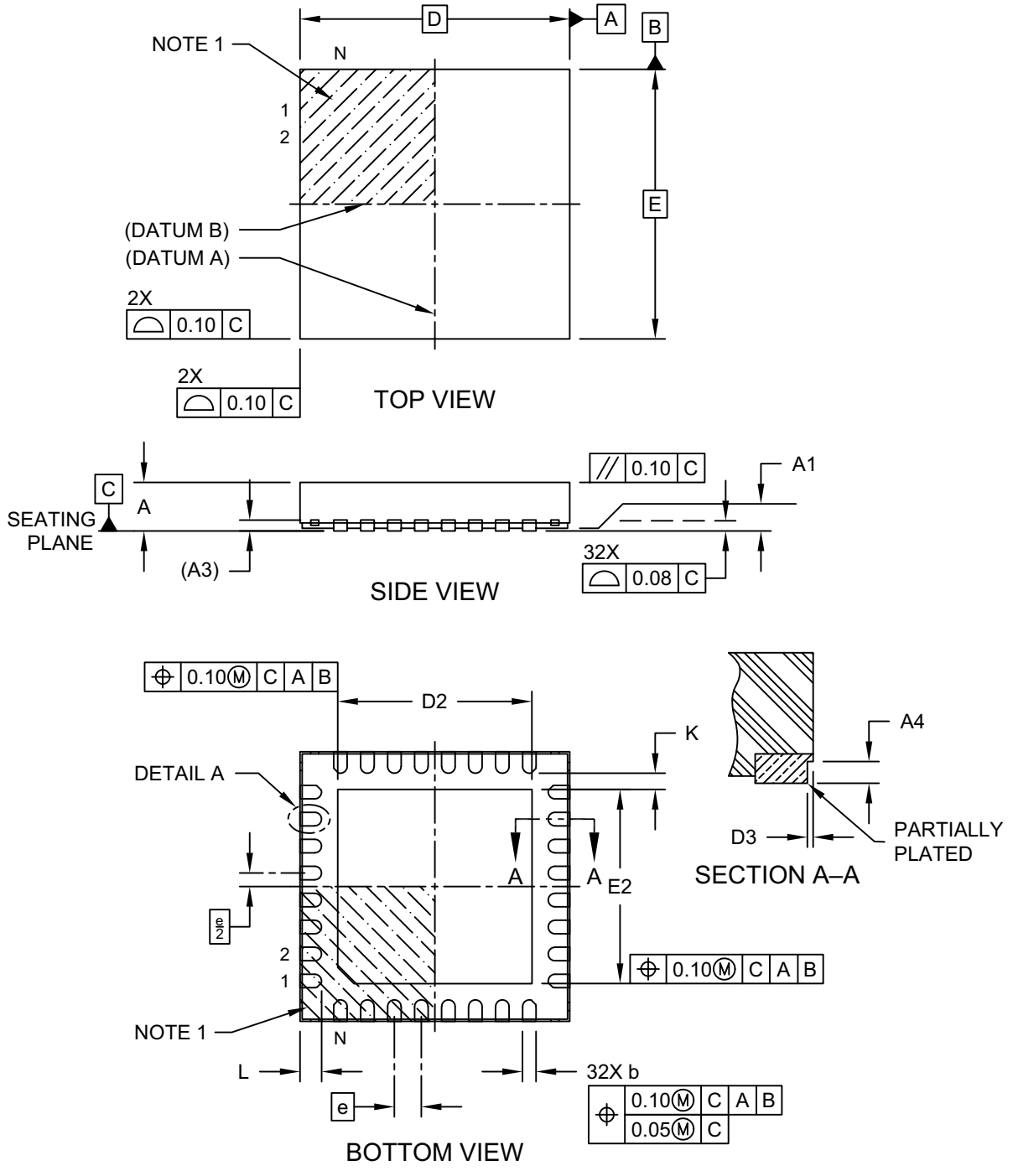


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks

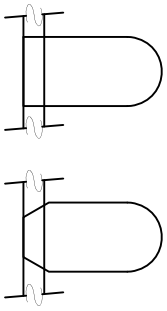
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



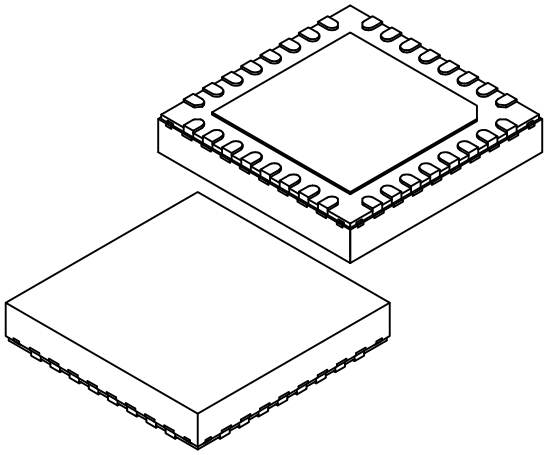
Microchip Technology Drawing C04-21391 Rev H Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Width	D3	-	-	0.085
Wettable Flank Step Cut Depth	A4	0.10	-	0.19

Dimensions D3 and A4 above apply to all new products released after November 1, and all products shipped after January 1, 2019, and supersede dimensions D3 and A4 below.
No physical changes are being made to any package; this update is to align cosmetic and tolerance variations from existing suppliers.

Wettable Flank Step Length	D3	0.035	0.06	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

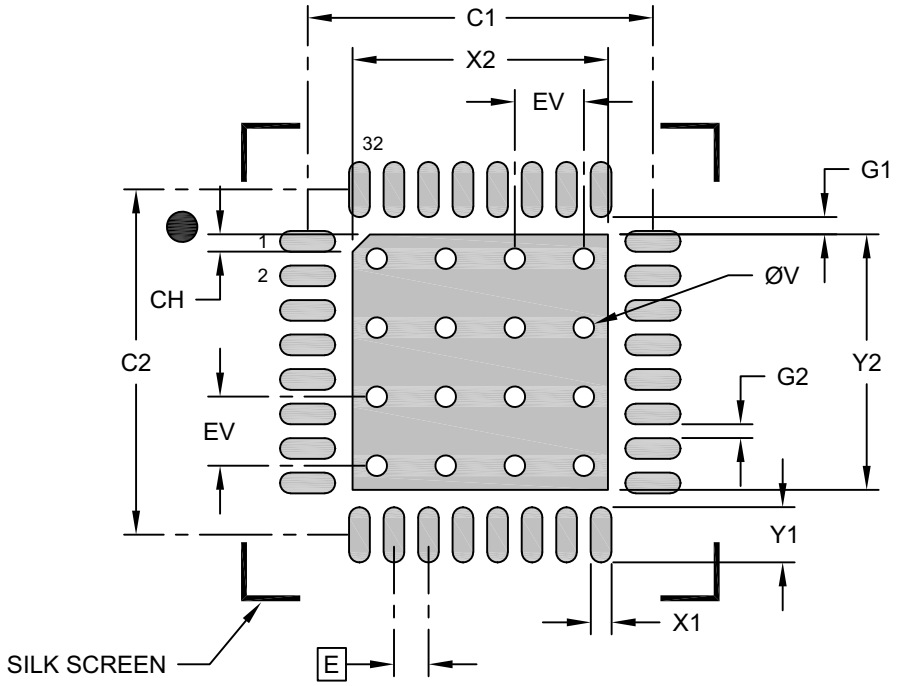
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21391 Rev H Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Exposed Pad 45° Corner Chamfer	CH		0.25	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.25		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23391 Rev H

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (October 2024)

- Updated document title to more accurately describe the device.

Revision A (March 2024)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] (1)	-X	/XXX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP19061: Four Switch Buck-Boost Analog Front End
Tape and Reel Option:	Blank = Standard packaging (73/tube) T = Tape and Reel (1) (3300/reel)
Temperature Range:	E = -40°C to +125°C (Extended)
Package:	RTB = 32-Lead Plastic Quad Flat, No Lead Package – 5x5x1 mm Body [VQFN]

Examples:

a) MCP19061-E/RTB: Tube, Extended temperature, 32LD VQFN 5x5 package

b) MCP19061T-E/RTB: Tape and Reel, Extended Temperature, 32LD VQFN 5x5 package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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