

FEATURES

Hermetic package offers excellent long-term stability

0 g offset vs. temperature (all axes): 0.75 mg/°C maximum

Ultralow noise density (all axes): 80 $\mu\text{g}/\sqrt{\text{Hz}}$

Low power, V_{SUPPLY} (LDO enabled)

ADXL356 in measurement mode: 150 μA

ADXL357 in measurement mode: 200 μA

ADXL356/ADXL357 in standby mode: 21 μA

ADXL356 has user adjustable analog output bandwidth

ADXL357 digital output features

Digital serial peripheral interface (SPI)/limited I²C interfaces supported

20-bit analog-to-digital converter (ADC)

Data interpolation routine for synchronous sampling

Programmable high- and low-pass digital filters

Integrated temperature sensor

Voltage range options

V_{SUPPLY} with internal regulators: 2.25 V to 3.6 V

V_{1P8ANA} , V_{1P8DIG} with internal low dropout (LDO) regulator bypassed: 1.8 V typical \pm 10%

Operating temperature range: -40°C to $+125^{\circ}\text{C}$

14-terminal, 6 mm \times 5.6 mm \times 2.05 mm, LCC package, 0.26 g

APPLICATIONS

Inertial measurement units (IMUs)/altitude and heading reference systems (AHRSS)

Platform stabilization systems

Structural health monitoring

Seismic imaging

Tilt sensing

Robotics

Condition monitoring

GENERAL DESCRIPTION

The analog output **ADXL356** and the digital output **ADXL357** are low noise density, low 0 g offset drift, low power, 3-axis accelerometers with selectable measurement ranges. The **ADXL356B** supports the ± 10 g and ± 20 g ranges, the **ADXL356C** supports the ± 10 g and ± 40 g ranges, and the **ADXL357** supports the ± 10.24 g, ± 20.48 g, and ± 40.96 g ranges.

The **ADXL356/ADXL357** offer industry leading noise, minimal offset drift over temperature, and long-term stability, enabling precision applications with minimal calibration.

FUNCTIONAL BLOCK DIAGRAMS

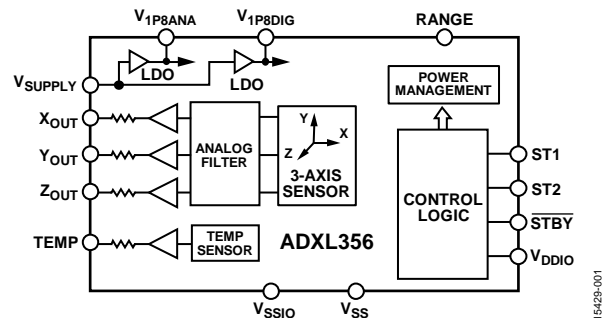


Figure 1. ADXL356

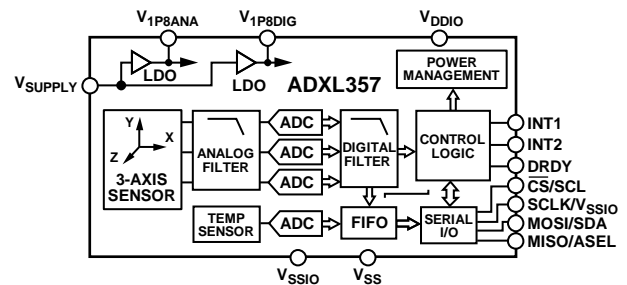


Figure 2. ADXL357

The low drift, low noise, and low power **ADXL357** enables accurate tilt measurement in an environment with high vibration, such as airborne IMUs. The low noise of the **ADXL356** over higher frequencies is ideal for wireless condition monitoring.

The **ADXL357** multifunction pin names may be referenced only by their relevant function for either the SPI or limited I²C interface.

¹ Protected by U.S. Patents 8,472,270; 9,041,462; 8,665,627; 8,917,099; 6,892,576; 9,297,825; and 7,956,621.

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REVISION HISTORY

2/2017—Revision 0: Initial Version

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Output at 25°C			892.2		mV
Scale Factor			3.0		mV/°C
TEMPERATURE					
Operating Temperature Range		-40		+125	°C

¹ The resonant frequency is a sensor characteristic. An integrated analog 1.5 kHz (-6 dB) sinc low-pass filter that cannot be bypassed limits the actual output response.

² The temperature change is -40°C to +25°C or +25°C to +125°C.

³ The VRE measurement is the shift in dc offset while the device is subject to 12.5 g rms of random vibration from 50 Hz to 2 kHz. The device under test (DUT) is configured for the ±10 g range and an output data rate of 4 kHz. The VRE scales with the range setting.

⁴ When V_{1PBANA} and V_{1PBDIG} are generated internally, V_{SUPPLY} is valid. To disable the LDO and drive V_{1PBANA} and V_{1PBDIG} externally, connect V_{SUPPLY} to V_{SS} .

⁵ Standby to measurement mode; valid when the output is within 5 mg of the final value.

DIGITAL OUTPUT FOR THE ADXL357

$T_A = 25^\circ\text{C}$, $V_{SUPPLY} = 3.3\text{ V}$, x-axis acceleration and y-axis acceleration = 0 g, z-axis acceleration = 1 g, full-scale range = ±10.24 g, and output data rate (ODR) = 500 Hz, unless otherwise noted. Note that multifunction pin names may be referenced only by their relevant function.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Output Full Scale Range (FSR)	User selectable		±10.24 ±20.48 ±40.96		g g g
Nonlinearity	±10 g		0.1		% FSR
Cross Axis Sensitivity			1		%
SENSITIVITY	Each axis				
X-Axis, Y-Axis, and Z-Axis Sensitivity	±10 g	47,104	51,200	55,296	LSB/g
	±20 g	23,552	25,600	27,648	LSB/g
	±40 g	11,776	12,800	13,824	LSB/g
X-Axis, Y-Axis, and Z-Axis Scale Factor	±10 g		19.5		μg/LSB
	±20 g		39		μg/LSB
	±40 g		78		μg/LSB
Sensitivity Change due to Temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		±0.01		%/°C
0 g OFFSET	Each axis, ±10 g				
X-Axis, Y-Axis, and Z-Axis 0 g Output		-375	±125	+375	mg
0 g Offset vs. Temperature (X-Axis, Y-Axis, and Z-Axis) ¹	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-0.75	±0.50	+0.75	mg/°C
Vibration Rectification Error (VRE) ²	Offset due to 7.5 g rms vibration, ±10 g range, in a 1 g orientation		<0.1		g
NOISE DENSITY	±10 g				
X-Axis, Y-Axis, and Z-Axis			80		μg/√Hz
Velocity Random Walk	X-axis and y-axis		45		μm/sec/√Hr
	Z-axis		65		μm/sec/√Hr
OUTPUT DATA RATE AND BANDWIDTH					
ADC Resolution			20		bits
Low-Pass Filter Passband Frequency	User programmable, Register 0x28	1		1000	Hz
High-Pass Filter Passband Frequency When Enabled (Disabled by Default)	User programmable, Register 0x28 for 4 kHz ODR	0.0095		10	Hz
SELF TEST					
Output Change					
Z-Axis	±10 g range		1.25		g

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Voltage Range					
V_{SUPPLY} Operating ³	$V_{\text{SUPPLY}} = 0 \text{ V}$	2.25	2.5	3.6	V
V_{DDIO}		V_{1PB8DIG}	2.5	3.6	V
V_{1PB8ANA} and V_{1PB8DIG} with Internal LDO Bypassed			1.62	1.8	1.98
Current					
Measurement Mode					
V_{SUPPLY} (LDO Enabled)			200		μA
V_{1PB8ANA} (LDO Disabled)			160		μA
V_{1PB8DIG} (LDO Disabled)			35.5		μA
Standby Mode					
V_{SUPPLY} (LDO Enabled)			21		μA
V_{1PB8ANA} (LDO Disabled)			7		μA
V_{1PB8DIG} (LDO Disabled)			10		μA
Turn On Time ⁴	$\pm 10 \text{ g}$ range		<10		ms
	Power-off to standby		<10		ms
TEMPERATURE SENSOR					
Output at 25°C			1852		LSB
Scale Factor			-9.05		LSB/°C
TEMPERATURE					
Operating Temperature Range		-40		+125	°C

¹ The temperature change is -40°C to +25°C or +25°C to +125°C.

² The VRE measurement is the shift in dc offset while the device is subject to 12.5 g rms random vibration from 50 Hz to 2 kHz. The DUT is configured for the $\pm 2 \text{ g}$ range and an output data rate of 4 kHz. The VRE scales with the range setting.

³ When V_{1PB8ANA} and V_{1PB8DIG} are generated internally, V_{SUPPLY} is valid. To disable the LDO and drive V_{1PB8ANA} and V_{1PB8DIG} externally, connect V_{SUPPLY} to V_{SS} .

⁴ Standby to measurement mode; valid when the output is within 1 mg of final value.

SPI DIGITAL INTERFACE CHARACTERISTICS FOR THE ADXL357

Note that multifunction pin names may be referenced by their relevant function only.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC INPUT LEVELS						
Input Voltage						
Low Level	V_{IL}				$0.3 \times V_{DDIO}$	V
High Level	V_{IH}		$0.7 \times V_{DDIO}$			V
Input Current						
Low Level	I_{IL}	$V_{IN} = 0V$	-0.1			μA
High Level	I_{IH}	$V_{IN} = V_{DDIO}$			0.1	μA
DC OUTPUT LEVELS						
Output Voltage						
Low Level	V_{OL}	$I_{OL} = I_{OL, MIN}$			$0.2 \times V_{DDIO}$	V
High Level	V_{OH}	$I_{OH} = I_{OH, MAX}$	$0.8 \times V_{DDIO}$			V
Output Current						
Low Level	I_{OL}	$V_{OL} = V_{OL, MAX}$	-10			mA
High Level	I_{OH}	$V_{OH} = V_{OH, MIN}$			4	mA
AC INPUT LEVELS						
SCLK Frequency			0.1		10	MHz
SCLK High Time	t_{HIGH}		40			ns
SCLK Low Time	t_{LOW}		40			ns
\overline{CS} Setup Time	t_{CSS}		20			ns
\overline{CS} Hold Time	t_{CSH}		20			ns
\overline{CS} Disable Time	t_{CSD}		40			ns
Rising SCLK Setup Time	t_{SCLKS}		20			ns
MOSI Setup Time	t_{SU}		20			ns
MOSI Hold Time	t_{HD}		20			ns
AC OUTPUT LEVELS						
Propagation Delay	t_P	$C_{LOAD} = 30\text{ pF}$			30	ns
Enable MISO Time	t_{EN}		30			ns
Disable MISO Time	t_{DIS}				20	ns

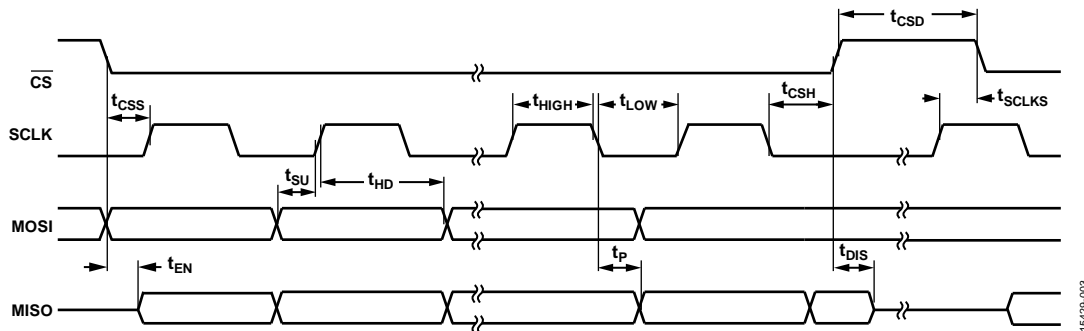


Figure 3. SPI Interface Timing Diagram

I²C DIGITAL INTERFACE CHARACTERISTICS FOR THE ADXL357

Note that multifunction pin names may be referenced only by their relevant function.

Table 4.

Parameter	Symbol	Test Conditions/ Comments	I2C_HS = 0 (Fast Mode)			I2C_HS = 1 (High Speed Mode)			Unit
			Min	Typ	Max	Min	Typ	Max	
DC INPUT LEVELS									
Input Voltage									
Low Level	V _{IL}				0.3 × V _{DDIO}		0.3 × V _{DDIO}		V
High Level	V _{IH}		0.7 × V _{DDIO}			0.7 × V _{DDIO}			V
Hysteresis of Schmitt Triggered Inputs	V _{HYS}		0.05 × V _{DDIO}			0.1 × V _{DDIO}			μA
Input Current	I _{IL}	0.1 × V _{DDIO} < V _{IN} < 0.9 × V _{DDIO}	-10		+10				μA
DC OUTPUT LEVELS									
Output Voltage									
Low Level	V _{OL1}	I _{OL} = 3 mA			0.4				V
	V _{OL2}	V _{DDIO} > 2 V			0.2 × V _{DDIO}				V
Output Current		V _{DDIO} ≤ 2 V							
Low Level	I _{OL}	V _{OL} = 0.4 V	20						mA
		V _{OL} = 0.6 V	6						mA
AC INPUT LEVELS									
SCL Frequency			0		1	0		3.4	MHz
SCL High Time	t _{HIGH}		260			60			ns
SCL Low Time	t _{LOW}		500			160			ns
Start Setup Time	t _{SUSTA}		260			160			ns
Start Hold Time	t _{HDSTA}		260			160			ns
SDA Setup Time	t _{SUDAT}		50			10			ns
SDA Hold Time	t _{HDDAT}		0			0			ns
Stop Setup Time	t _{SUSTO}		260			160			ns
Bus Free Time	t _{BUF}		500						ns
SCL Input Rise Time	t _{RCL}				120		80		ns
SCL Input Fall Time	t _{FCL}				120		80		ns
SDA Input Rise Time	t _{RDA}				120		160		ns
SDA Input Fall Time	t _{FDA}				120		160		ns
Width of Spikes to Suppress	t _{SP}	Not shown in Figure 4			50		10		ns
AC OUTPUT LEVELS									
Propagation Delay		C _{LOAD} = 500 pF							
Data	t _{VDDAT}		97		450	27		135	ns
Acknowledge	t _{VDACK}				450				ns
Output Fall Time	t _F	Not shown in Figure 4	20 × (V _{DDIO} /5.5)		120				ns

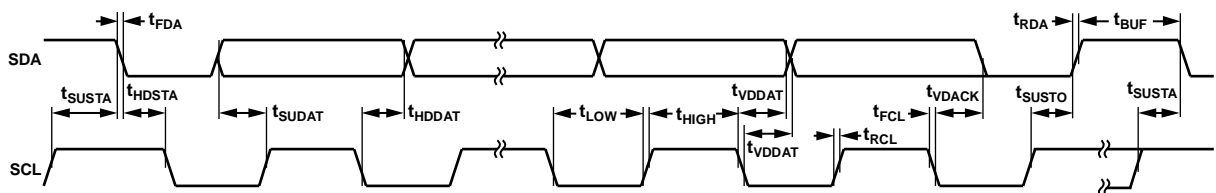


Figure 4. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Acceleration (Any Axis, 0.1 ms)	5000 g
V_{SUPPLY} , V_{DDIO}	5.4 V
V_{1PBANA} , V_{1PBDIG} Configured as Inputs	1.98 V
ADXL356	
Digital Inputs (RANGE, ST1, ST2, STBY)	-0.3 V to $V_{DDIO} + 0.3$ V
Analog Outputs (X_{OUT} , Y_{OUT} , Z_{OUT} , TEMP)	-0.3 V to $V_{1PBANA} + 0.3$ V
ADXL357	
Digital Pins (\overline{CS}/SCL , $SCLK/V_{SSIO}$, MOSI/SDA, MISO/ASEL, INT1, INT2, DRDY)	-0.3 V to $V_{DDIO} + 0.3$ V
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-55°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
E-14-1 ¹	42	°C/W

¹ Thermal impedance simulated values are based on a JEDEC 252P thermal test board with four thermal vias. See JEDEC JESD51.

RECOMMENDED SOLDERING PROFILE

Figure 5 and Table 7 provide details about the recommended soldering profile.

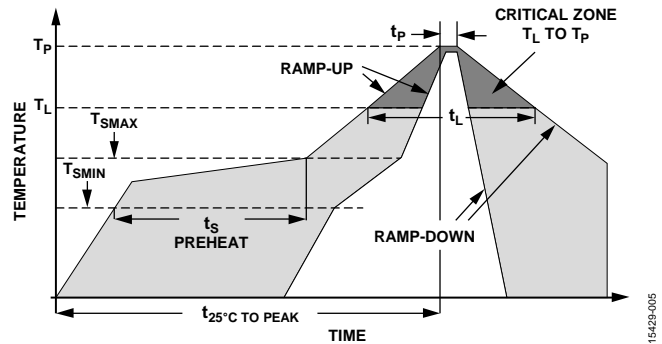


Figure 5. Recommended Soldering Profile

Table 7. Recommended Soldering Profile

Profile Feature	Condition	
	Sn63/Pb37	Pb-Free
Average Ramp Rate from Liquid Temperature (T_L) to Peak Temperature (T_p)	3°C/sec maximum	3°C/sec maximum
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time from T_{SMIN} to T_{SMAX} (t_s)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum	3°C/sec maximum
Liquid Temperature (T_L)	183°C	217°C
Time Maintained Above T_L (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_p)	240°C + 0°C/-5°C	260°C + 0°C/-5°C
Time of Actual $T_p - 5^\circ\text{C}$ (t_p)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec maximum	6°C/sec maximum
Time from 25°C to Peak Temperature ($t_{25^\circ\text{C TO PEAK}}$)	6 minutes maximum	8 minutes maximum

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

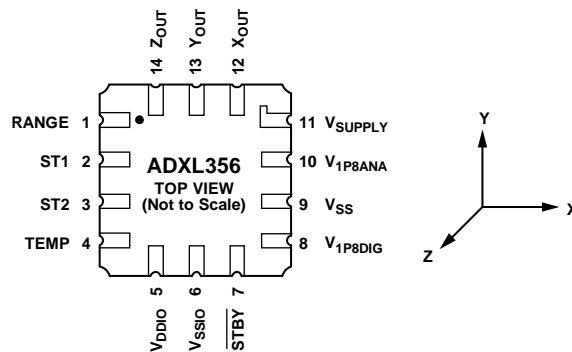


Figure 6. ADXL356 Pin Configuration

Table 8. ADXL356 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RANGE	Range Selection Pin. Set this pin to ground to select the $\pm 10 g$ range, or set this pin to V_{DDIO} to select the $\pm 20 g$ or $\pm 40 g$ range. This pin is model dependent (see the Ordering Guide section).
2	ST1	Self Test Pin 1. This pin enables self test mode.
3	ST2	Self Test Pin 2. This pin activates the electromechanical self test actuation.
4	TEMP	Temperature Sensor Output.
5	V_{DDIO}	Digital Interface Supply Voltage.
6	V_{SSIO}	Digital Ground.
7	\overline{STBY}	Standby or Measurement Mode Selection Pin. Set this pin to ground to enter standby mode, or set this pin to V_{DDIO} to enter measurement mode.
8	V_{1P8DIG}	Digital Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS} , supply the voltage to this pin externally.
9	V_{SS}	Analog Ground.
10	V_{1P8ANA}	Analog Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS} , supply the voltage to this pin externally.
11	V_{SUPPLY}	Supply Voltage. When V_{SUPPLY} equals 2.25 V to 3.6 V, V_{SUPPLY} enables the internal LDO regulators to generate V_{1P8DIG} and V_{1P8ANA} . For $V_{SUPPLY} = V_{SS}$, V_{1P8DIG} and V_{1P8ANA} are externally supplied.
12	X_{OUT}	X-Axis Output.
13	Y_{OUT}	Y-Axis Output.
14	Z_{OUT}	Z-Axis Output.

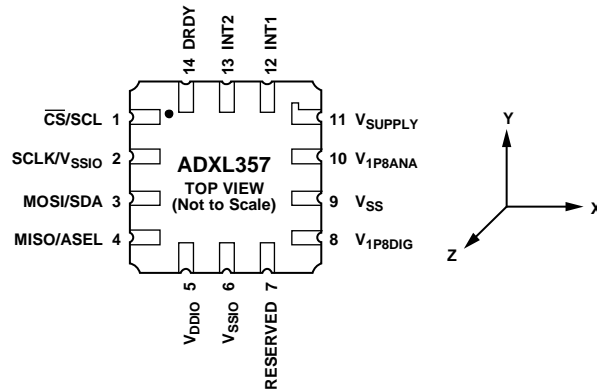


Figure 7. ADXL357 Pin Configuration (SPI/I²C)

Table 9. ADXL357 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CS/SCL	Chip Select for SPI (CS).
2	SCLK/V _{SSIO}	Serial Communications Clock for I ² C (SCL). Serial Communications Clock for SPI (SCLK).
3	MOSI/SDA	I ² C Mode Enable (V _{SSIO}). Connect this pin to Pin 6 (V _{SSIO}) to enable I ² C mode. Master Output, Slave Input for SPI (MOSI).
4	MISO/ASEL	Serial Data for I ² C (SDA). Master Input, Slave Output for SPI (MISO). Alternate I ² C Address Select for I ² C (ASEL).
5	V _{DDIO}	Digital Interface Supply Voltage.
6	V _{SSIO}	Digital Ground.
7	RESERVED	Reserved. This pin can be connected to ground or left open.
8	V _{1P8DIG}	Digital Supply. This pin requires a decoupling capacitor. If V _{SUPPLY} connects to V _{SS} , supply the voltage to this pin externally.
9	V _{SS}	Analog Ground.
10	V _{1P8ANA}	Analog Supply. This pin requires a decoupling capacitor. If V _{SUPPLY} connects to V _{SS} , supply the voltage to this pin externally.
11	V _{SUPPLY}	Supply Voltage. When V _{SUPPLY} equals 2.25 V to 3.6 V, V _{SUPPLY} enables the internal LDOs to generate V _{1P8DIG} and V _{1P8ANA} . For V _{SUPPLY} = V _{SS} , V _{1P8DIG} and V _{1P8ANA} are externally supplied.
12	INT1	Interrupt Pin 1.
13	INT2	Interrupt Pin 2.
14	DRDY	Data Ready Pin.

TYPICAL PERFORMANCE CHARACTERISTICS

All figures include data for multiple devices and multiple lots, and they were taken in the $\pm 10\text{ g}$ range, unless otherwise noted.

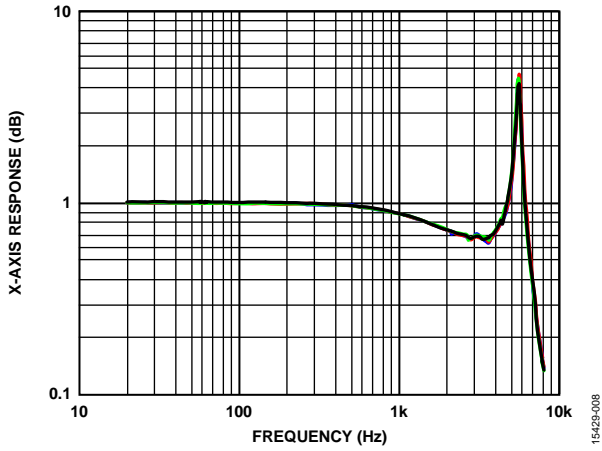


Figure 8. ADXL356 Frequency Response for X-Axis

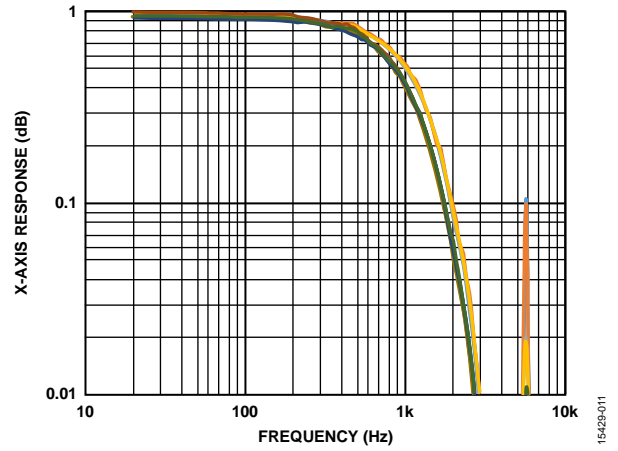


Figure 11. ADXL357 Normalized Frequency Response for X-Axis at 4 kHz ODR

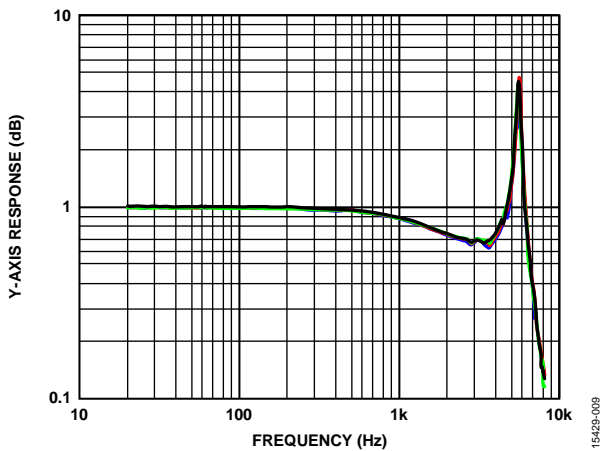


Figure 9. ADXL356 Frequency Response for Y-Axis

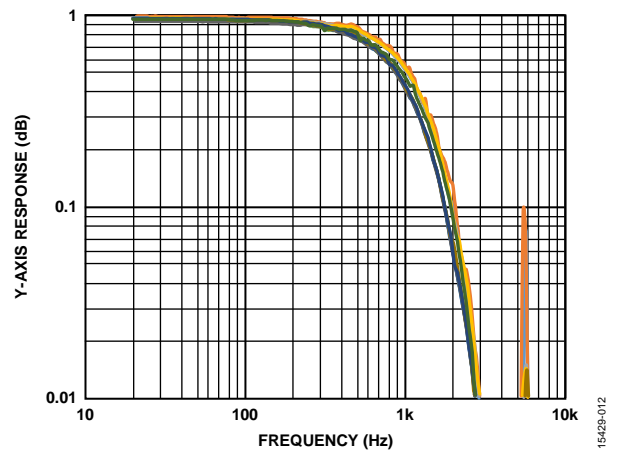


Figure 12. ADXL357 Normalized Frequency Response for Y-Axis at 4 kHz ODR

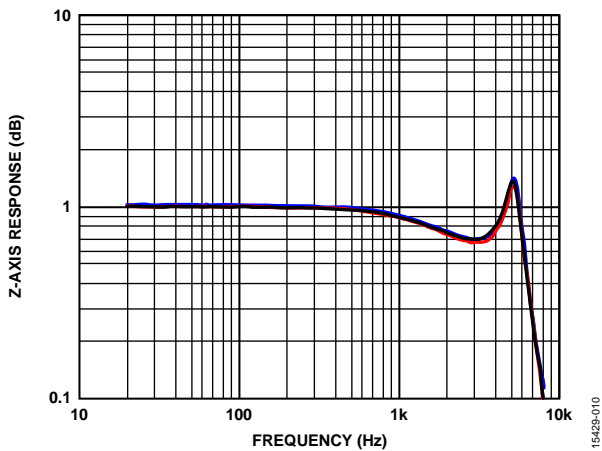


Figure 10. ADXL356 Frequency Response for Z-Axis

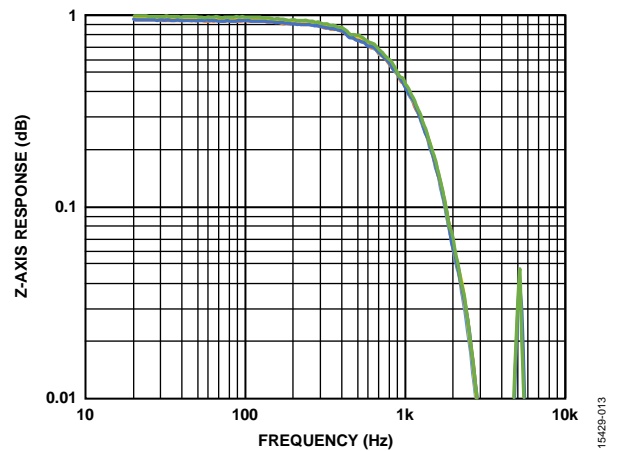
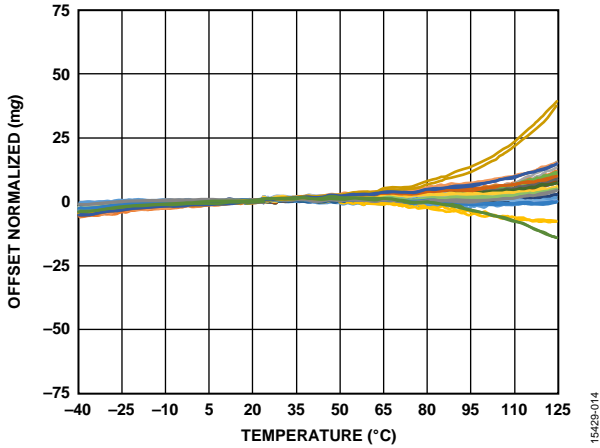
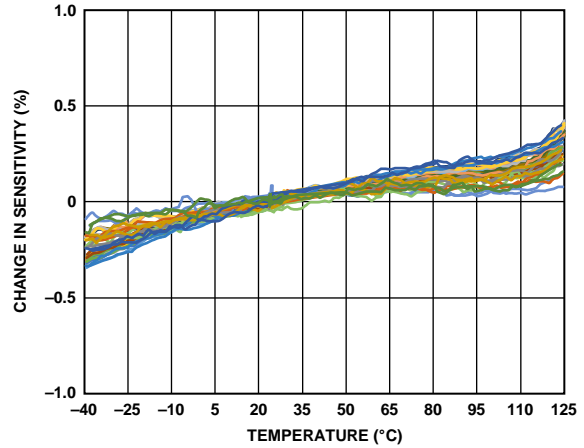


Figure 13. ADXL357 Normalized Frequency Response for Z-Axis at 4 kHz ODR



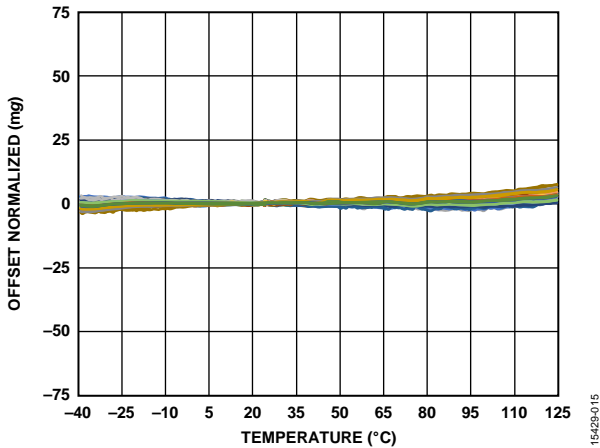
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Figure 14. ADXL356 X-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature



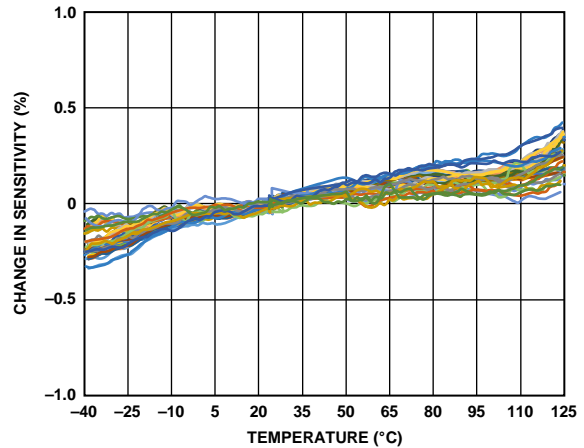
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Figure 17. ADXL356 X-Axis Change in Sensitivity Relative to 25°C vs. Temperature



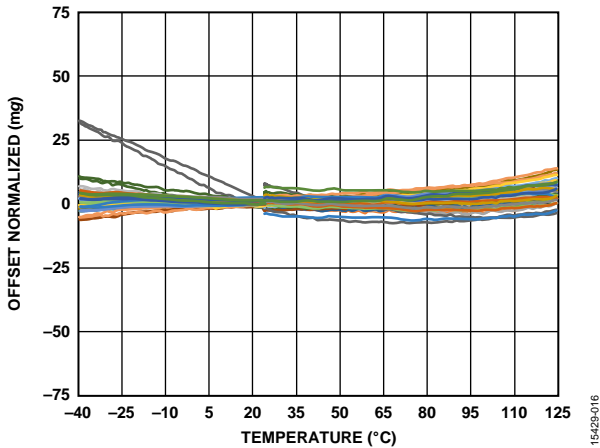
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Figure 15. ADXL356 Y-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature



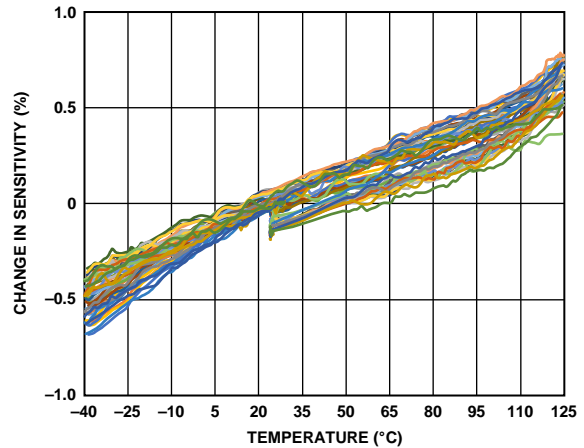
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Figure 18. ADXL356 Y-Axis Change in Sensitivity Relative to 25°C vs. Temperature



15429-016

Figure 16. ADXL356 Z-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature



15429-019

Figure 19. ADXL356 Z-Axis Change in Sensitivity Relative to 25°C vs. Temperature

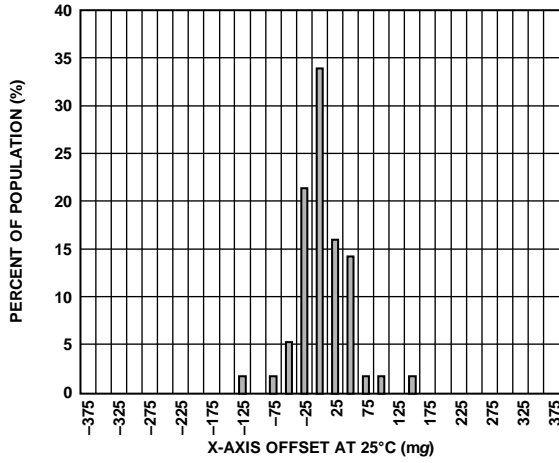


Figure 20. ADXL356 Zero g Offset Histogram at 25°C, X-Axis

15429-020

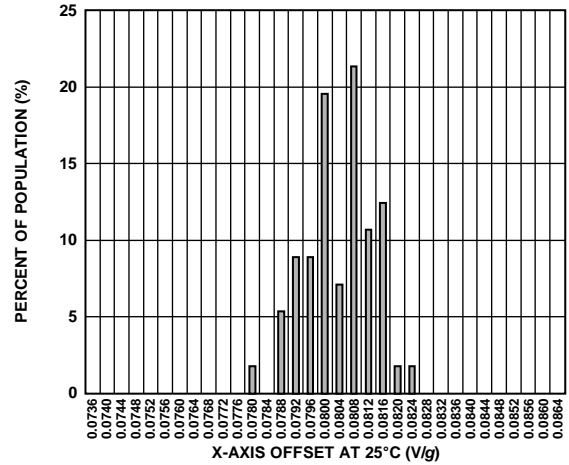


Figure 23. ADXL356 Sensitivity Histogram at 25°C, X-Axis

15429-023

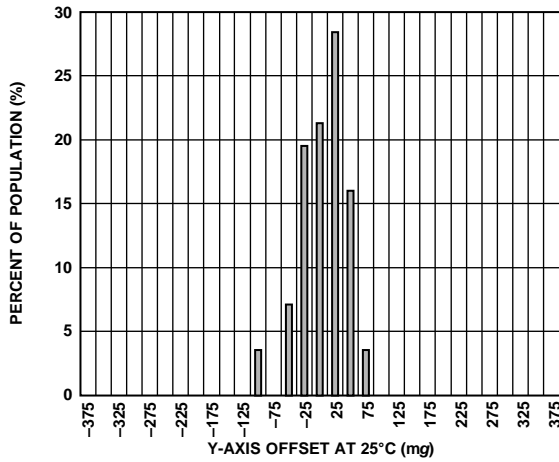


Figure 21. ADXL356 Zero g Offset Histogram at 25°C, Y-Axis

15429-021

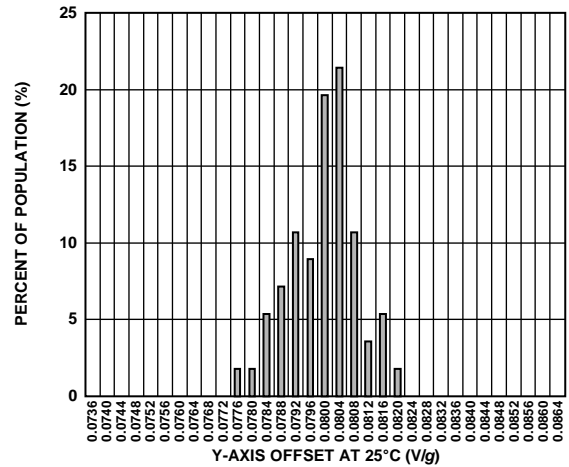


Figure 24. ADXL356 Sensitivity Histogram at 25°C, Y-Axis

15429-024

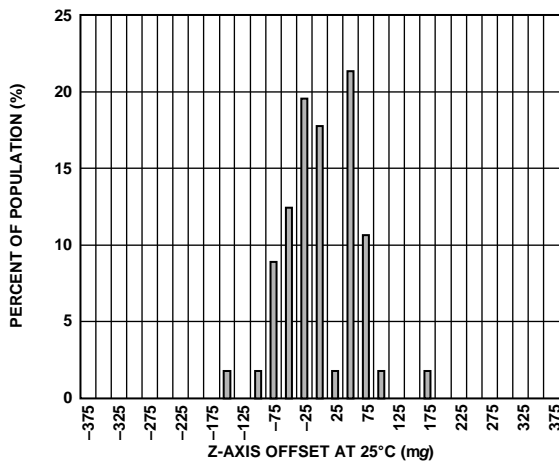


Figure 22. ADXL356 Zero g Offset Histogram at 25°C, Z-Axis

15429-022

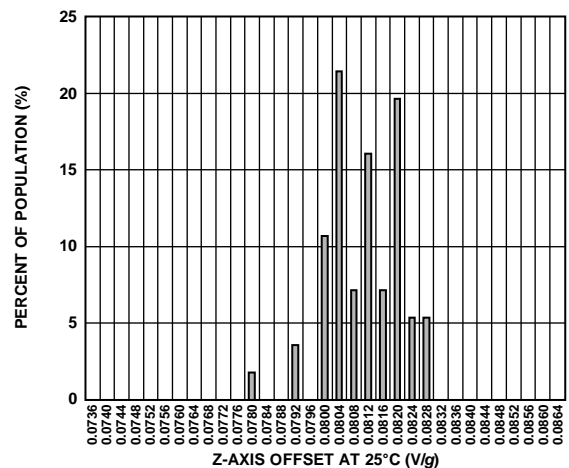


Figure 25. ADXL356 Sensitivity Histogram at 25°C, Z-Axis

15429-025

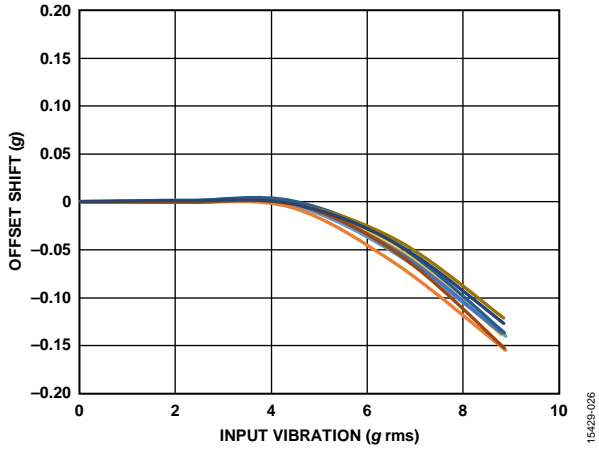


Figure 26. ADXL356 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±10 g Range, X-Axis Orientation = -1 g

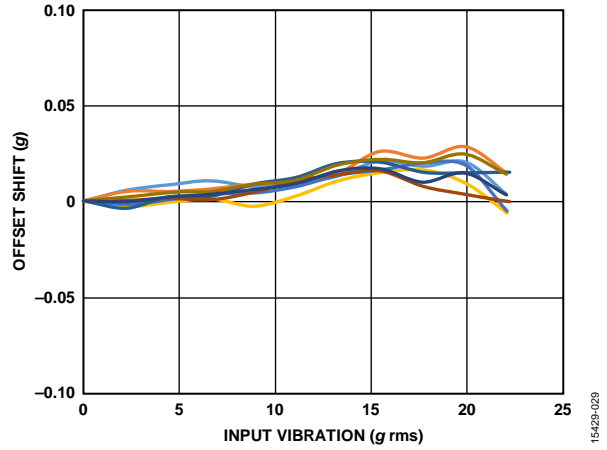


Figure 29. ADXL356 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±40 g Range, X-Axis Orientation = -1 g

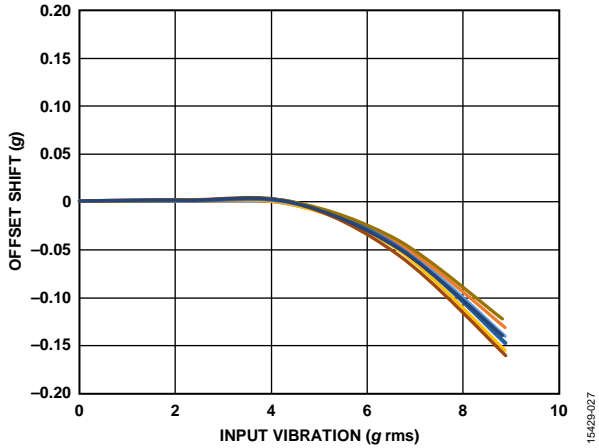


Figure 27. ADXL356 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±10 g Range, Y-Axis Orientation = +1 g

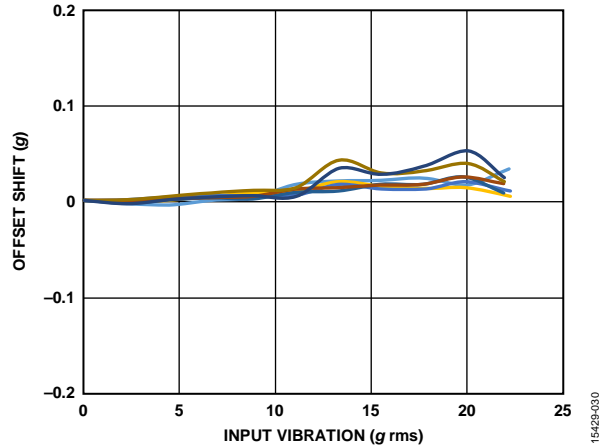


Figure 30. ADXL356 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±40 g Range, Y-Axis Orientation = +1 g

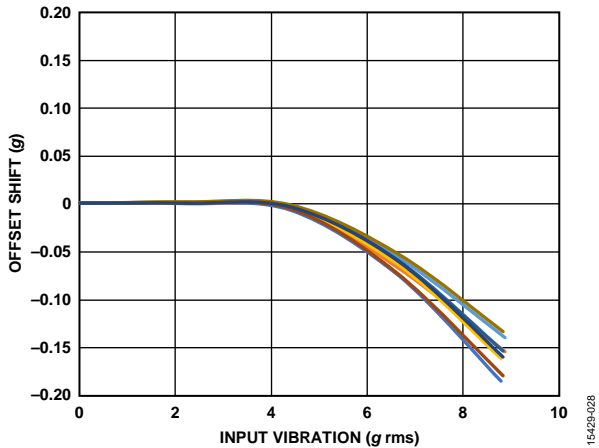


Figure 28. ADXL356 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±10 g Range, Z-Axis Orientation = +1 g

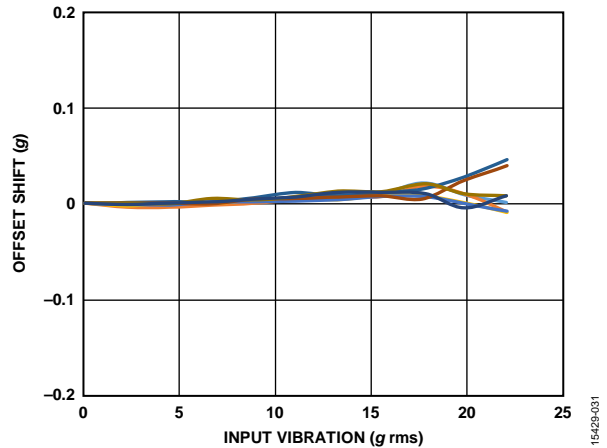


Figure 31. ADXL356 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±40 g Range, Z-Axis Orientation = +1 g

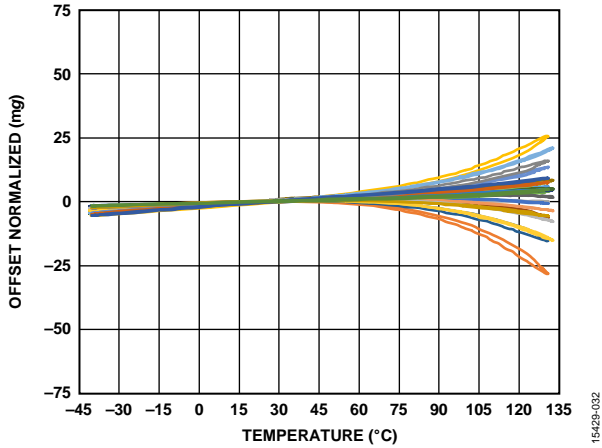


Figure 32. ADXL357 X-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

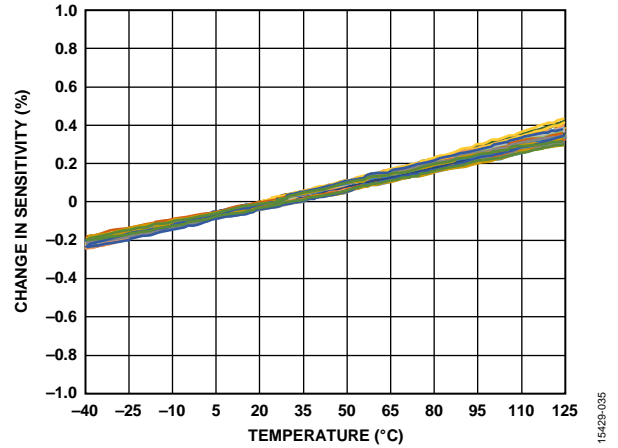


Figure 35. ADXL357 X-Axis Change in Sensitivity Relative to 25°C vs. Temperature

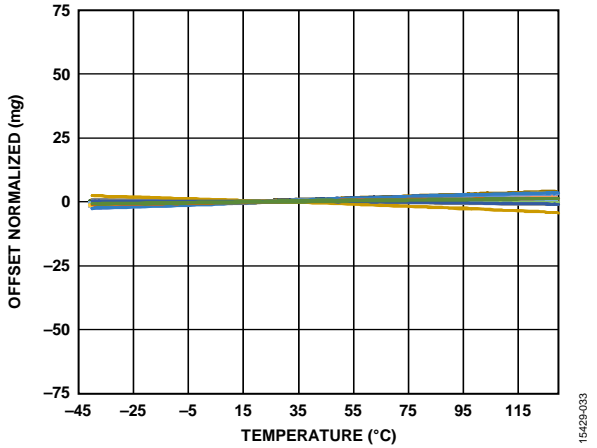


Figure 33. ADXL357 Y-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

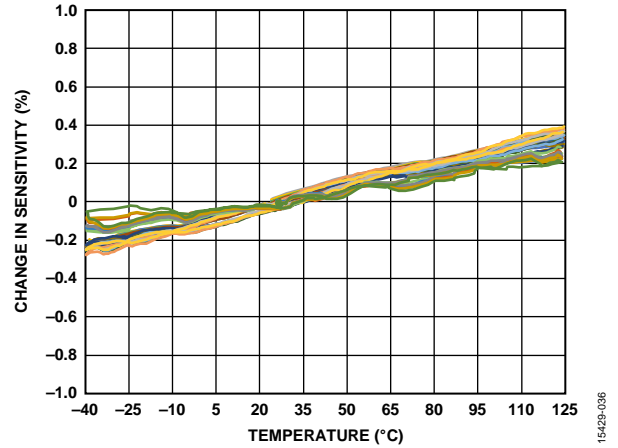


Figure 36. ADXL357 Y-Axis Change in Sensitivity Relative to 25°C vs. Temperature

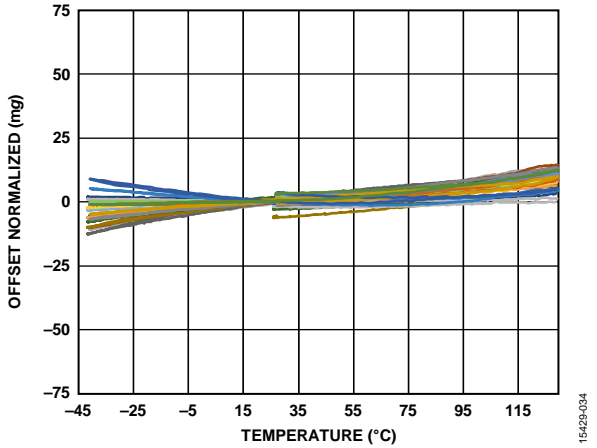


Figure 34. ADXL357 Z-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

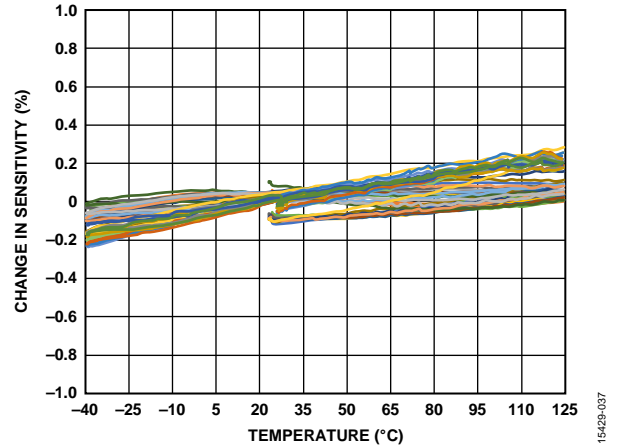
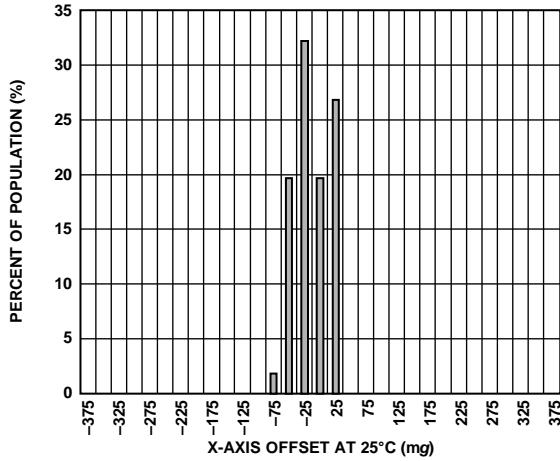
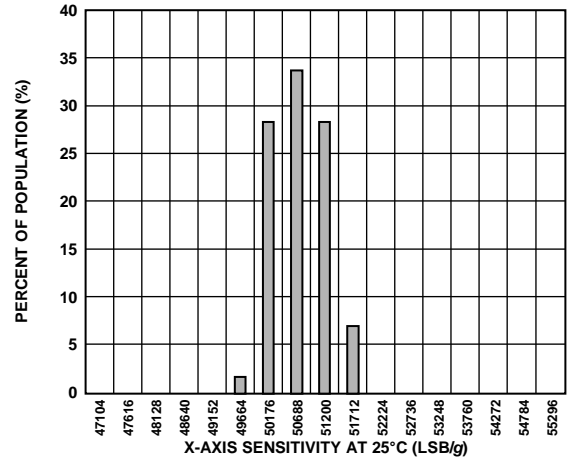


Figure 37. ADXL357 Z-Axis Change in Sensitivity Relative to 25°C vs. Temperature



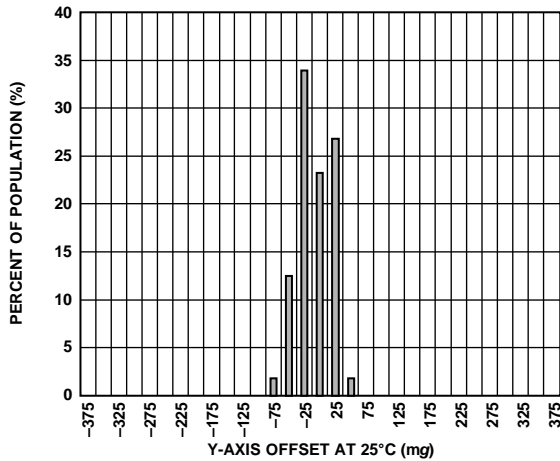
15429-038

Figure 38. ADXL357 Zero g Offset Histogram at 25°C, X-Axis



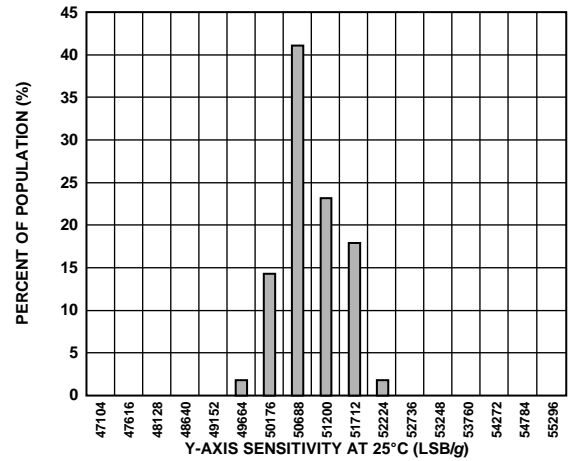
15429-041

Figure 41. ADXL357 Sensitivity Histogram at 25°C, X-Axis



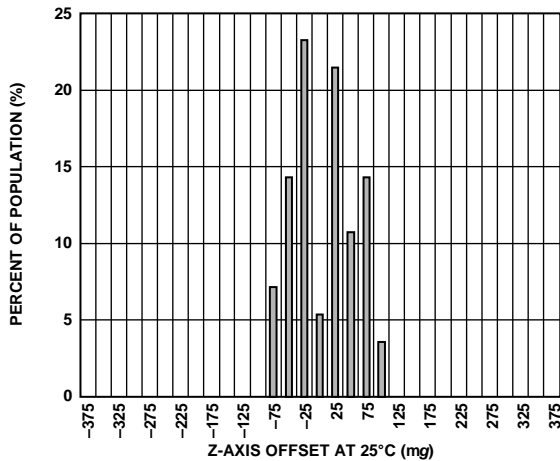
15429-039

Figure 39. ADXL357 Zero g Offset Histogram at 25°C, Y-Axis



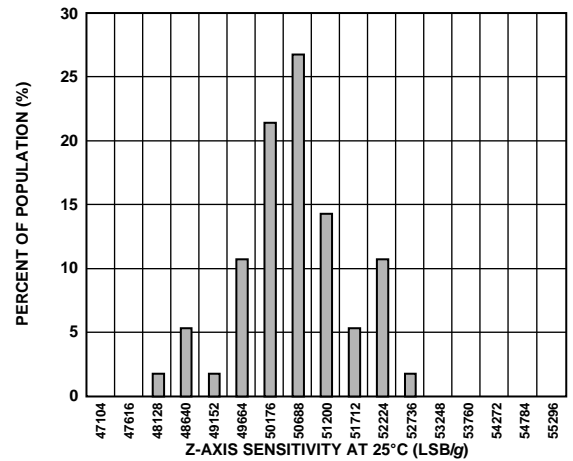
15429-042

Figure 42. ADXL357 Sensitivity Histogram at 25°C, Y-Axis



15429-040

Figure 40. ADXL357 Zero g Offset Histogram at 25°C, Z-Axis



15429-043

Figure 43. ADXL357 Sensitivity Histogram at 25°C, Z-Axis

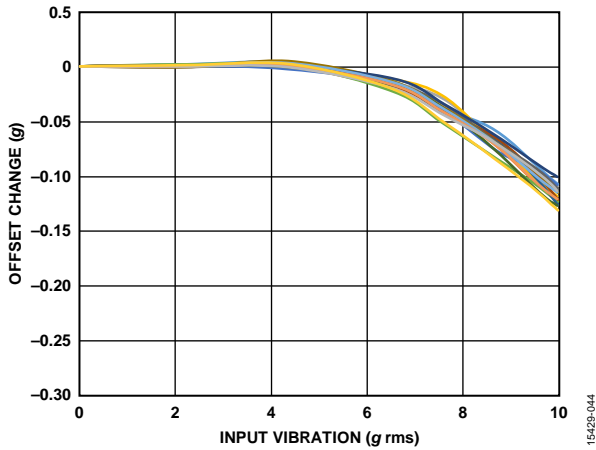


Figure 44. ADXL357 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ± 10 g Range, X-Axis Orientation = -1 g

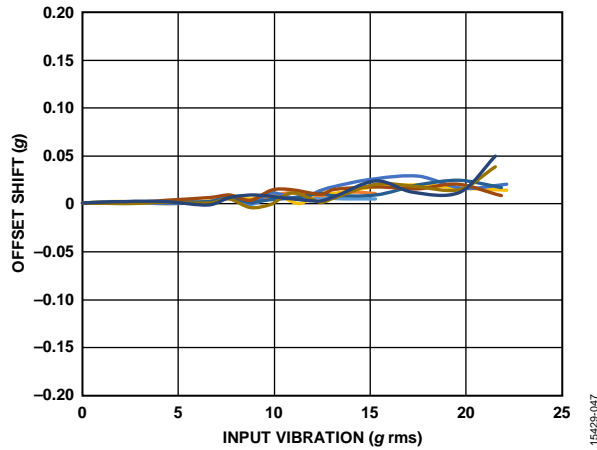


Figure 47. ADXL357 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ± 40 g Range, X-Axis Orientation = -1 g

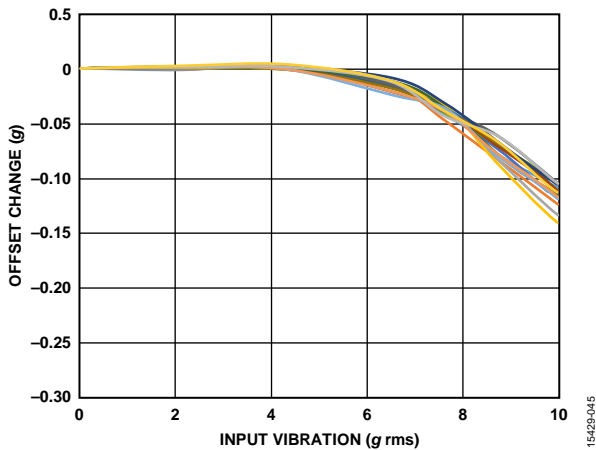


Figure 45. ADXL357 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ± 10 g Range, Y-Axis Orientation = +1 g

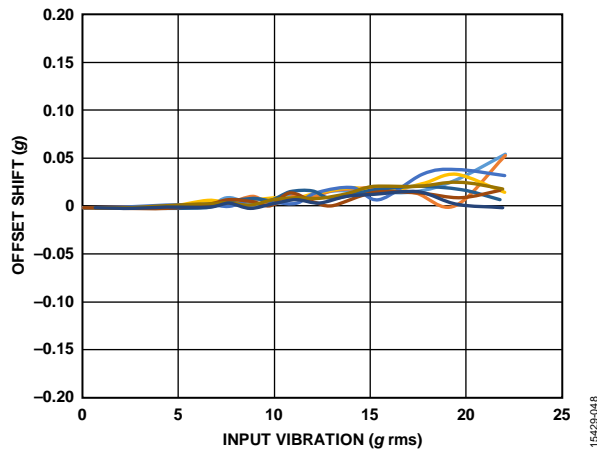


Figure 48. ADXL357 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ± 40 g Range, Y-Axis Orientation = +1 g

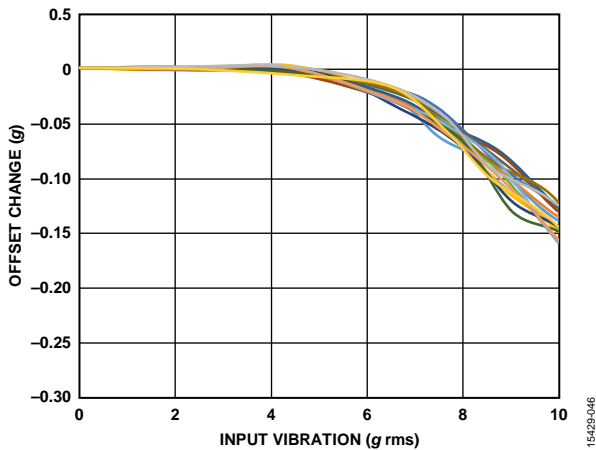


Figure 46. ADXL357 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ± 10 g Range, Z-Axis Orientation = +1 g

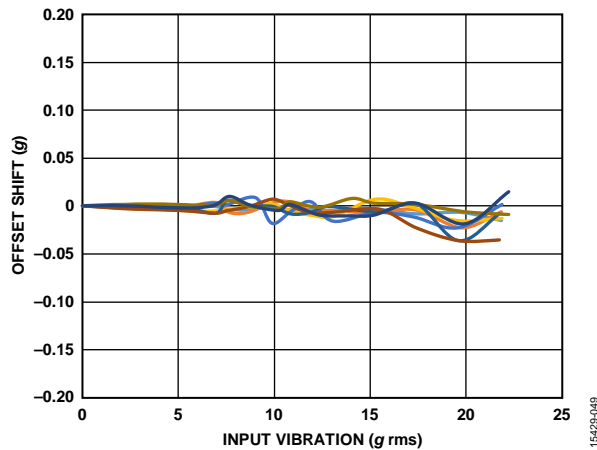


Figure 49. ADXL357 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ± 40 g Range, Z-Axis Orientation = +1 g

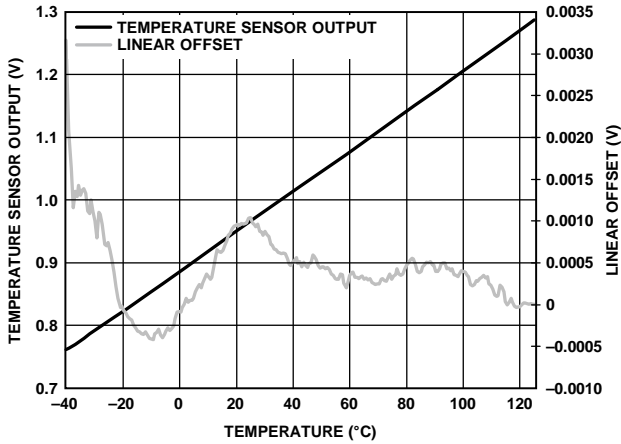


Figure 50. ADXL356 Temperature Sensor Output and Linearity Offset vs. Temperature

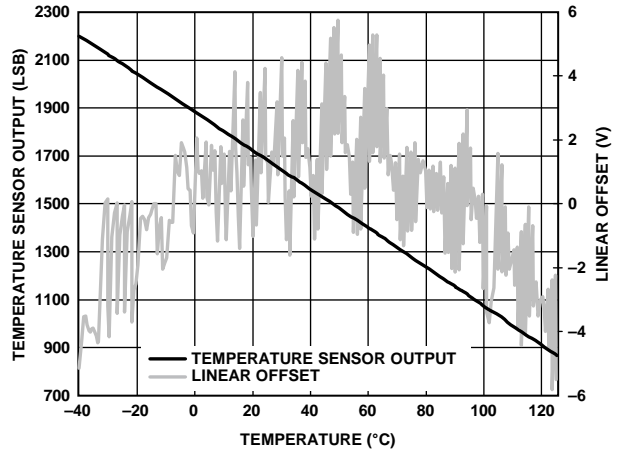


Figure 53. ADXL357 Temperature Sensor Output and Linearity Offset vs. Temperature

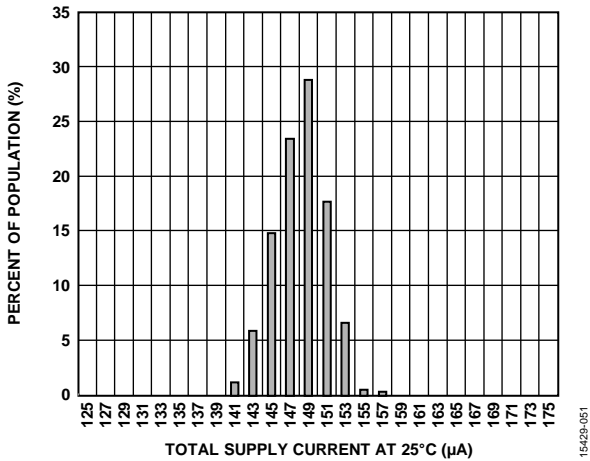


Figure 51. ADXL356 Total Supply Current, 3.3 V

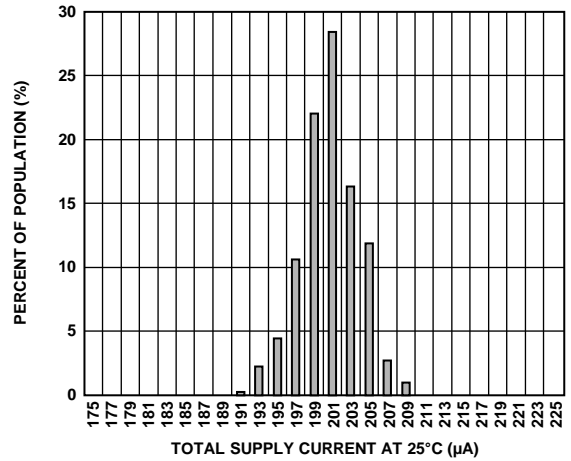


Figure 54. ADXL357 Total Supply Current, 3.3 V

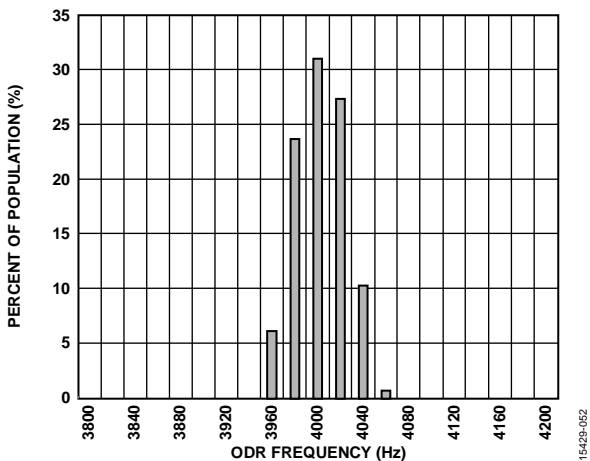


Figure 52. ADXL357 Internal ODR Frequency Histogram

ROOT ALLAN VARIANCE (RAV) ADXL357 CHARACTERISTICS

Figure 55 to Figure 57 include data for multiple devices and multiple lots, and they were taken in the ± 10 g range, unless otherwise noted.

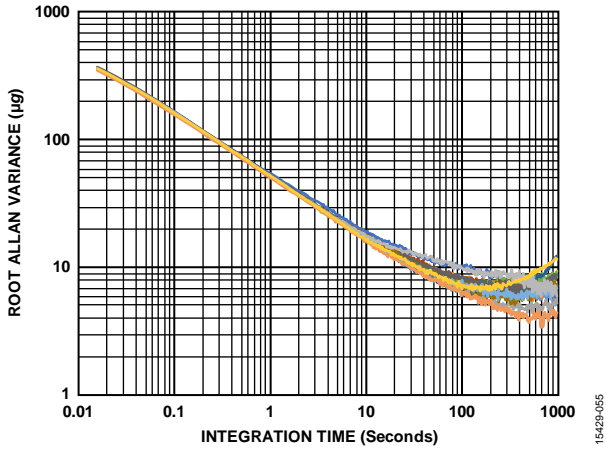


Figure 55. ADXL357 Root Allan Variance (RAV), X-Axis

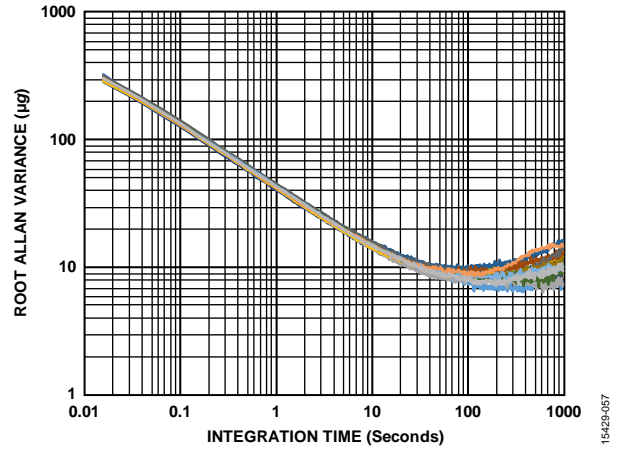


Figure 57. ADXL357 Root Allan Variance (RAV), Z-Axis

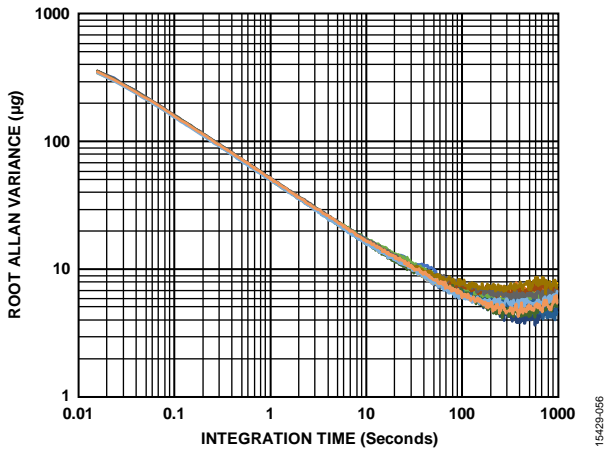


Figure 56. ADXL357 Root Allan Variance (RAV), Y-Axis

15425-055

15425-057

15425-056

THEORY OF OPERATION

The [ADXL356](#) is a complete 3-axis, ultralow noise and ultrastable offset MEMS accelerometer with outputs ratiometric to the analog 1.8 V supply, V_{IP8ANA} . The [ADXL357](#) adds three high resolution ADCs that use the analog 1.8 V supply as a reference to provide digital outputs insensitive to the supply voltage. The [ADXL356B](#) is pin selectable for $\pm 10\text{ g}$ or $\pm 20\text{ g}$ full scale, the [ADXL356C](#) is pin selectable for $\pm 10\text{ g}$ or $\pm 40\text{ g}$ full scale, and the [ADXL357](#) is programmable for $\pm 10.24\text{ g}$, $\pm 20.48\text{ g}$, and $\pm 40.96\text{ g}$ full scale. The [ADXL357](#) offers both SPI and I²C communications ports.

The micromachined, sensing elements are fully differential, comprising the lateral x-axis and y-axis sensors and the vertical, teeter totter z-axis sensors. The x-axis and y-axis sensors and the z-axis sensors go through separate signal paths that minimize offset drift and noise. The signal path is fully differential, except

for a differential to single-ended conversion at the analog outputs of the [ADXL356](#).

The analog accelerometer outputs of the [ADXL356](#) are ratiometric to V_{IP8ANA} ; therefore, carefully digitize them correctly. The temperature sensor output is not ratiometric. The X_{OUT} , Y_{OUT} , and Z_{OUT} analog outputs are filtered internally with an antialiasing filter. These analog outputs also have an internal 32 k Ω series resistor that can be used with an external capacitor to set the bandwidth of the output.

The [ADXL357](#) includes antialias filters before and after the high resolution Σ - Δ ADC. User-selectable output data rates and filter corners are provided. The temperature sensor is digitized with a 12-bit successive approximation register (SAR) ADC.

APPLICATIONS INFORMATION

ANALOG OUTPUT

Figure 58 shows the [ADXL356](#) application circuit. The analog outputs (X_{OUT} , Y_{OUT} , and Z_{OUT}) are ratiometric to the 1.8 V analog voltage from the V_{IP8ANA} pin. V_{IP8ANA} can be powered with an on-chip LDO regulator that is powered from V_{SUPPLY} . V_{IP8ANA} can also be supplied externally by forcing V_{SUPPLY} to V_{SS} , which disables the LDO regulator. Due to the ratiometric response, the analog output requires referencing to the V_{IP8ANA} supply when digitizing to achieve the inherent noise and offset performance of the [ADXL356](#). The 0 g bias output is nominally equal to $V_{IP8ANA}/2$. The recommended option is to use the [ADXL356](#) with a ratiometric ADC (for example, the Analog Devices, Inc., [AD7682](#)) with V_{IP8ANA} providing the voltage reference. This configuration results in self cancellation of errors due to minor supply variations.

The [ADXL356](#) outputs two forms of filtering: internal anti-aliasing filtering with a cutoff frequency of approximately 1.5 kHz, and external filtering. The external filter uses a fixed, on-chip, 32 kΩ resistance in series with each output in conjunction with the external capacitors to implement the low-pass filter anti-aliasing

and noise reduction prior to the external ADC. The antialias filter cutoff frequency must be significantly higher than the desired signal bandwidth. If the antialias filter corner is too low, ratiometricity can degrade where the signal attenuation is different from the reference attenuation.

DIGITAL OUTPUT

Figure 59 shows the [ADXL357](#) application circuit with the recommended bypass capacitors. The communications interface is either SPI or I²C (see the Serial Communications section for additional information).

The [ADXL357](#) includes an internal configurable digital band-pass filter. Both the high-pass and low-pass poles of the filter are adjustable, as detailed in the Filter Settings Register section and Table 44. At power-up, the default conditions for the filters are as follows:

- High-pass filter (HPF) = dc (off)
- Low-pass filter (LPF) = 1000 Hz
- Output data rate = 4000 Hz

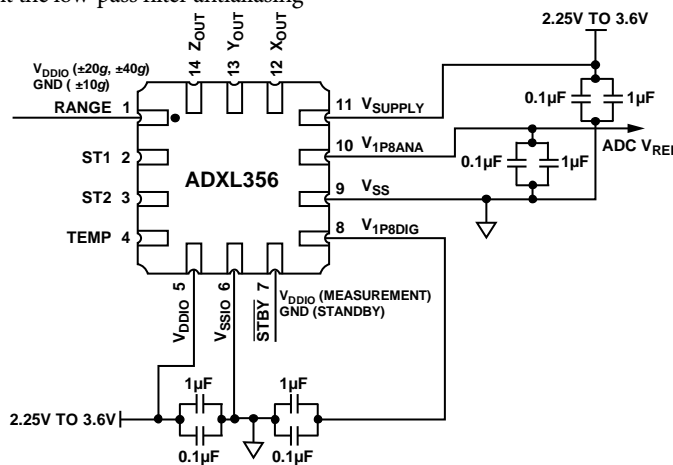


Figure 58. [ADXL356](#) Application Circuit

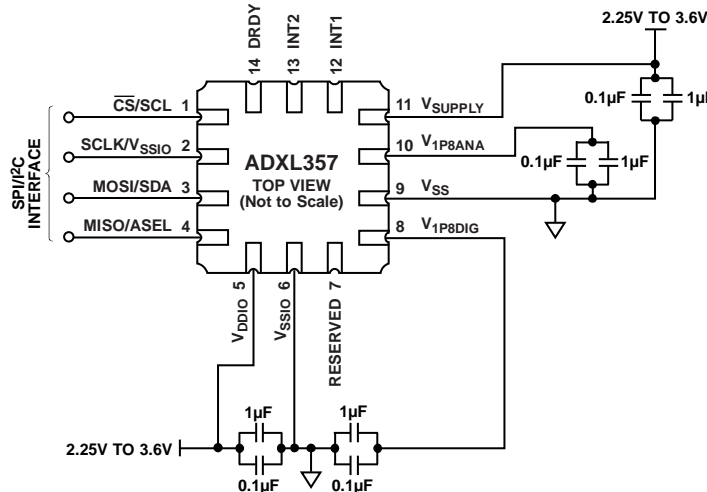


Figure 59. [ADXL357](#) Application Circuit

AXES OF ACCELERATION SENSITIVITY

Figure 60 shows the axes of acceleration sensitivity. Note that the output voltage increases when accelerated along the sensitive axis.

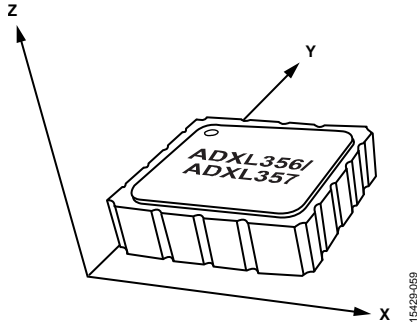


Figure 60. Axes of Acceleration Sensitivity

POWER SEQUENCING

There are two methods for applying power to the device. Typically, internal LDO regulators generate the 1.8 V power for the analog and digital supplies, V_{IP8ANA} and V_{IP8DIG} , respectively. Optionally, connecting V_{SUPPLY} to V_{SS} and driving V_{IP8ANA} and V_{IP8DIG} with an external supply can supply V_{IP8ANA} and V_{IP8DIG} .

When using the internal LDO regulators, connect V_{SUPPLY} to a voltage source between 2.25 V to 3.6 V. In this case, V_{DDIO} and V_{SUPPLY} can be powered in parallel. V_{SUPPLY} must not exceed the V_{DDIO} voltage by greater than 0.5 V. If necessary, V_{DDIO} can be powered before V_{SUPPLY} .

When disabling the internal LDO regulators and using an external 1.8 V supply to power V_{IP8ANA} and V_{IP8DIG} , tie V_{SUPPLY} to ground, and set V_{IP8ANA} and V_{IP8DIG} to the same final voltage level. In the case of bypassing the LDOs, the recommended power sequence is to apply power to V_{DDIO} , followed by V_{IP8DIG} approximately 10 μ s later, and then V_{IP8ANA} approximately 10 μ s later. If necessary, V_{IP8DIG} and V_{DDIO} can be powered from the same 1.8 V supply, which can also be tied to V_{IP8ANA} with proper isolation. In this case, proper decoupling and low frequency isolation is important to maintain the noise performance of the sensor.

POWER SUPPLY DESCRIPTION

The [ADXL356/ADXL357](#) have four different power supply domains: V_{SUPPLY} , V_{IP8ANA} , V_{IP8DIG} , and V_{DDIO} . The internal analog and digital circuitry operates at 1.8 V nominal.

V_{SUPPLY}

V_{SUPPLY} is 2.25 V to 3.6 V, which is the input range to the two LDO regulators that generate the nominal 1.8 V outputs for V_{IP8ANA} and V_{IP8DIG} . Connect V_{SUPPLY} to V_{SS} to disable the LDO regulators, which allows driving V_{IP8ANA} and V_{IP8DIG} from an external source.

V_{IP8ANA}

All sensor and analog signal processing circuitry operates in this domain. Offset and sensitivity of the analog output [ADXL356](#) are ratiometric to this supply voltage. When using

external ADCs, use V_{IP8ANA} as the reference voltage. The digital output [ADXL357](#) includes ADCs that are ratiometric to V_{IP8ANA} , thereby rendering offset and sensitivity insensitive to the value of V_{IP8ANA} . V_{IP8ANA} can be an input or an output as defined by the state of the V_{SUPPLY} voltage.

V_{IP8DIG}

V_{IP8DIG} is the supply voltage for the internal logic circuitry. A separate LDO regulator decouples the digital supply noise from the analog signal path. V_{IP8ANA} can be an input or an output as defined by the state of the V_{SUPPLY} voltage. If driven externally, V_{IP8DIG} must be the same voltage as the V_{IP8ANA} voltage.

V_{DDIO}

The V_{DDIO} value determines the logic high levels. On the analog output [ADXL356](#), V_{DDIO} sets the logic high level for the self test pins, ST1 and ST2, as well as the STBY pin. On the digital output [ADXL357](#), V_{DDIO} sets the logic high level for communications interface ports, as well as the interrupt and DRDY outputs.

The LDO regulators are operational when V_{SUPPLY} is between 2.25 V and 3.6 V. V_{IP8ANA} and V_{IP8DIG} are the regulator outputs in this mode. Alternatively, when tying V_{SUPPLY} to V_{SS} , V_{IP8ANA} and V_{IP8DIG} are supply voltage inputs with a 1.62 V to 1.98 V range.

OVERRANGE PROTECTION

To avoid electrostatic capture of the proof mass when the accelerometer is subject to input acceleration beyond its full-scale range, all sensor drive clocks turn off for 0.5 ms. In the $\pm 10 g/\pm 10.24 g$ range setting, the overrange protection activates for input signals beyond approximately $\pm 40 g$ ($\pm 25\%$), and for the $\pm 20 g/\pm 20.48 g$ and $\pm 40 g/\pm 40.95 g$ range settings, the threshold corresponds to about $\pm 80 g$ ($\pm 25\%$).

When overrange protection occurs, the X_{OUT} , Y_{OUT} , and Z_{OUT} pins on the [ADXL356](#) begin to drive to midscale. The [ADXL357](#) floats toward zero, and first in, first out (FIFO) buffer begins filling with this data.

SELF TEST

The [ADXL356](#) and [ADXL357](#) incorporate a self test feature that effectively tests the mechanical and electronic system. Enabling self test stimulates the sensor electrostatically to produce an output corresponding to the test signal applied as well as the mechanical force exerted. Only the z-axis response is specified to validate device functionality.

In the [ADXL356](#), drive the ST1 pin to V_{DDIO} to invoke self test mode. Then, by driving the ST2 pin to V_{DDIO} , the [ADXL356](#) applies an electrostatic force to the mechanical sensor and induces a change in output in response to the force. The self test delta (or response) is the difference in output voltage in the z-axis when ST2 is high vs. ST2 is low, while ST1 is asserted. After the self test measurement is complete, bring both pins low to resume normal operation.

The self test operation is similar in the [ADXL357](#), except ST1 and ST2 can be accessed through the SELF_TEST register (Register 0x2E).

The self test feature rejects externally applied acceleration and only responds to the self test force, which allows an accurate measurement of the self test, even in the presence of external mechanical noise.

FILTER

The ADXL356/ADXL357 use an analog, low-pass, antialiasing filter to reduce out of band noise and to limit bandwidth. The ADXL357 provides further digital filtering options to maintain excellent noise performance at various ODRs.

The analog, low-pass antialiasing filter in the ADXL356/ADXL357 provides a fixed bandwidth of approximately 1.5 kHz, the frequency at which the output response is attenuated by approximately 50%. The shape of the filter response in the frequency domain is that of a sinc3 filter.

The ADXL356 x-axis, y-axis, and z-axis analog outputs include an amplifier followed by a series 32 kΩ resistor, and output to the X_{OUT}, the Y_{OUT}, and the Z_{OUT} pins, respectively.

The ADXL357 provides an internal 20-bit, Σ-Δ ADC to digitize the filtered analog signal. Additional digital filtering (beyond the analog, low-pass, antialiasing filter) consists of a low-pass digital decimation filter and a bypassable high-pass filter that supports output data rates between 4 kHz and 3.906 Hz. The decimation filter consists of two stages. The first stage is fixed decimation with a 4 kHz ODR with a low-pass filter cutoff (50% reduction in output response) at about 1 kHz. A variable second stage decimation filter is used for the 2 kHz output data rate and below (it is bypassed for 4 kHz ODR). Figure 61 shows the low-pass filter response with a 1 kHz corner (4 kHz ODR) for the ADXL357. Note that Figure 61 does not include the fixed frequency analog, low-pass, antialiasing filter with a fixed bandwidth of approximately 1.5 kHz.

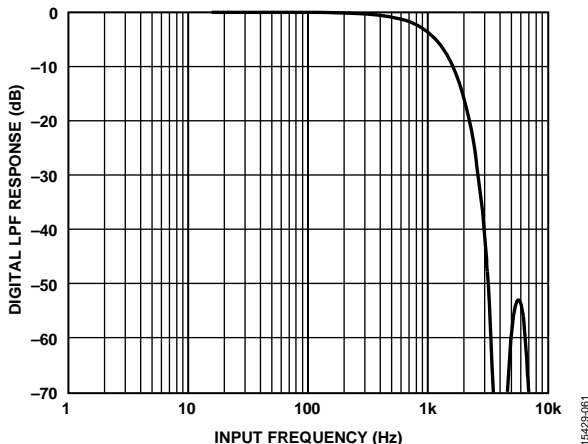


Figure 61. ADXL357 Digital Low-Pass Filter (LPF) Response for 4 kHz ODR

The ADXL357 pass band of the signal path relates to the combined filter responses, including the analog filter previously described, and the digital decimation filter/ODR setting. Table 10 shows the delay associated with the decimation filter for each setting and provides the attenuation at the ODR/4 corner.

The ADXL357 also includes an optional digital high-pass filter with a programmable corner frequency. By default, the high-pass filter is disabled. The high-pass corner frequency, where the output is attenuated by 50%, is related to the ODR, and the HPF_CORNER setting in the filter register (Register 0x28, Bits[6:4]). Table 11 shows the HPF_CORNER response. Figure 62 and Figure 63 show the simulated high-pass filter response and delay for a 10 Hz cutoff.

The ADXL357 also includes an interpolation filter, after the decimation filters, that produces oversampled/upconverted data and provides an external synchronization option. See the Data Synchronization section for more details. Table 12 shows the delay and attenuation relative to the programmed ODR.

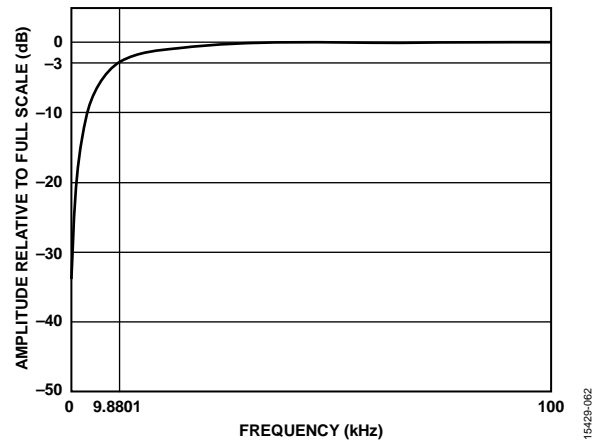


Figure 62. High-Pass Filter Pass-Band Response for a 4 kHz ODR and an HPF_CORNER Setting of 001 (Register 0x28, Bits[6:4])

Group delay is the digital filter delay from the input to the ADC until data is available at the interface (see the Filter section). This delay is the largest component of the total delay from sensor to serial interface.

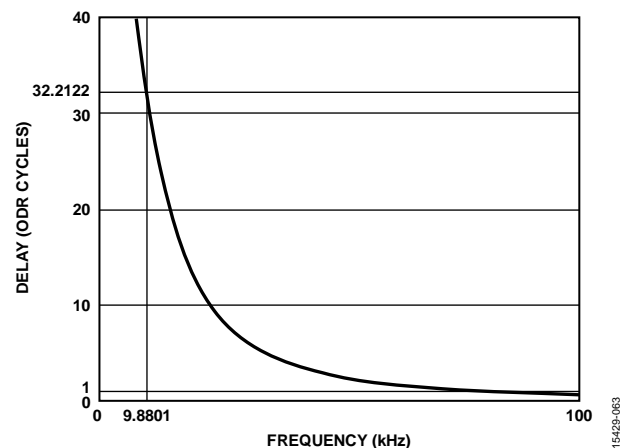


Figure 63. High-Pass Filter Delay Response for a 4 kHz ODR and an HPF_CORNER Setting of 001 (Register 0x28, Bits[6:4])

Table 10. Digital Filter Group Delay and Profile

Programmed ODR (Hz)	Delay		Attenuation	
	ODR (Cycles)	Time (ms)	Decimator at ODR/4 (dB)	Full Path at ODR/4 (dB)
4000	2.52	0.63	-3.44	-3.63
4000/2 = 2000	2.00	1.00	-2.21	-2.26
4000/4 = 1000	1.78	1.78	-1.92	-1.93
4000/8 = 500	1.63	3.26	-1.83	-1.83
4000/16 = 250	1.57	6.27	-1.83	-1.83
4000/32 = 125	1.54	12.34	-1.83	-1.83
4000/64 = 62.5	1.51	24.18	-1.83	-1.83
4000/128 ~ 31	1.49	47.59	-1.83	-1.83
4000/256 ~ 16	1.50	96.25	-1.83	-1.83
4000/512 ~ 8	1.50	189.58	-1.83	-1.83
4000/1024 ~ 4	1.50	384.31	-1.83	-1.83

Table 11. Digital High-Pass Filter Response

HPF_CORNER Register Setting (Register 0x28, Bits[6:4])	HPF_CORNER Frequency, -3 dB Point Relative to ODR Setting	-3 dB at 4 kHz ODR (Hz)
000	Not applicable, no high-pass filter enabled	Off
001	$247 \times 10^{-3} \times \text{ODR}$	9.88
010	$62.084 \times 10^{-3} \times \text{ODR}$	2.48
011	$15.545 \times 10^{-3} \times \text{ODR}$	0.62
100	$3.862 \times 10^{-3} \times \text{ODR}$	0.1545
101	$0.954 \times 10^{-3} \times \text{ODR}$	0.03816
110	$0.238 \times 10^{-3} \times \text{ODR}$	0.00952

Table 12. Combined Digital Interpolation Filter and Decimation Filter Response

Interpolator Data Rate Resolution Relative to $64 \times \text{ODR}$ (Hz)	Combined Interpolator/Decimator Delay (ODR Cycles)	Combined Interpolator/Decimator Delay (ms)	Combined Interpolator/Decimator Output Attenuation at ODR/4 (dB)
$64 \times 4000 = 256000$	3.51661	0.88	-6.18
$64 \times 2000 = 128000$	3.0126	1.51	-4.93
$64 \times 1000 = 64000$	2.752	2.75	-4.66
$64 \times 500 = 32000$	2.6346	5.27	-4.58
$64 \times 250 = 16000$	2.5773	10.31	-4.55
$64 \times 125 = 8000$	2.5473	20.38	-4.55
$64 \times 62.5 = 4000$	2.53257	40.52	-4.55
$64 \times 31.25 = 2000$	2.52452	80.78	-4.55
$64 \times 15.625 = 1000$	2.52045	161.31	-4.55
$64 \times 7.8125 = 500$	2.5194	322.48	-4.55
$64 \times 3.90625 = 250$	2.51714	644.39	-4.55

SERIAL COMMUNICATIONS

The 4-wire serial interface communicates in either the SPI or I²C protocol. It affectively autodetects the format being used, requiring no configuration control to select the format.

SPI PROTOCOL

Wire the [ADXL357](#) for SPI communication as shown in the connection diagram in Figure 64. The SPI protocol timing is shown in Figure 65 to Figure 68. The timing scheme follows the clock polarity (CPOL) = 0 and clock phase (CPHA) = 0. The SPI clock speed ranges from 100 kHz to 10 MHz.

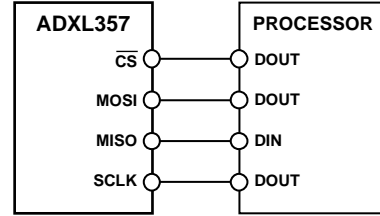


Figure 64. 4-Wire SPI Connection

15429-064

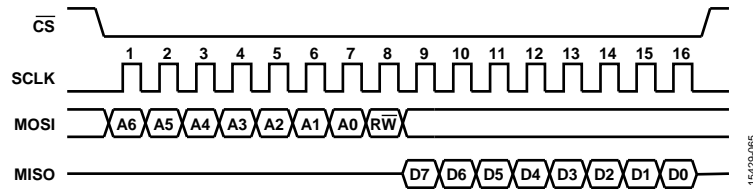


Figure 65. SPI Timing Diagram—Single-Byte Read

15429-065

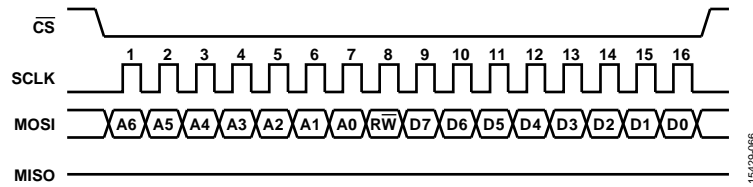


Figure 66. SPI Timing Diagram—Single-Byte Write

15429-066

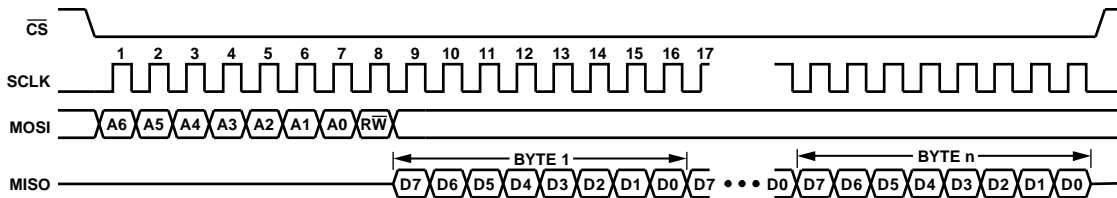


Figure 67. SPI Timing Diagram—Multibyte Read

15429-067

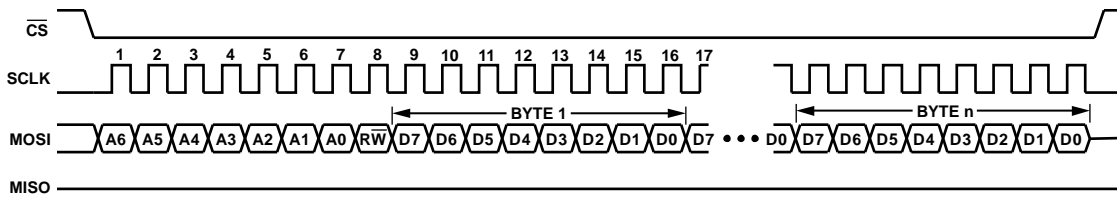


Figure 68. SPI Timing Diagram—Multibyte Write

15429-068

I²C PROTOCOL

The ADXL357 supports point to point I²C communication. However, when sharing an SDA bus, the ADXL357 may prevent communication with other devices on that bus. If at any point, even when the ADXL357 is not being addressed, the 0x3A and 0x3B bytes (when the ADXL357 device ID is set to 0x1D), or the 0xA6 and 0xA7 bytes (when the ADXL357 device ID is set to 0x53) are transmitted on the SDA bus, the ADXL357 responds with an acknowledge bit and pulls the SDA line down. For example, this response can occur when reading or writing the data bytes (0x3A/0x3B or 0xA6/0xA7) to another sensor on the bus. When the ADXL357 pulls the SDA line down, communication with other devices on the bus may be interrupted. To resolve this, the ADXL357 must be connected to a separate SDA bus, or the SCL pin must be switched high when communication with the ADXL357 is not desired (it is normally grounded).

The ADXL357 supports standard (100 kHz), fast (up to 1 MHz) and high speed (up to 3.4 MHz) data transfer modes when the bus parameters in Table 4 are met. There is no minimum SCL frequency, with the exception that, when reading data, the clock must be fast enough to read an entire sample set before new data overwrites it. Single- or multiple-byte reads/writes are supported. With the ASEL pin low, the I²C address for the device is 0x1D and an alternate I²C address of 0x53 can be chosen by pulling the ASEL pin high.

There are no internal pull-up or pull-down resistors for any unused pins; therefore, there is no known state or default state for the pins if left floating or unconnected. It is required that SCLK/V_{SSIO} be connected to ground when communicating to the ADXL357 using I²C.

Due to communication speed limitations, the maximum output data rate when using the 400 kHz I²C mode is 800 Hz, and it scales linearly with a change in the I²C communication speed. For example, using I²C at 100 kHz limits the maximum ODR to 200 Hz. Operation at an output data rate above the recommended maximum may result in an undesirable effect on the acceleration data, including missing samples or additional noise.

Figure 69 to Figure 71 detail the I²C protocol timing. The I²C interface can be used on most buses operating in I²C standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high speed mode (3.4 MHz). The ADXL357 I²C device ID is as follows:

- ASEL (pin) = 0, device address = 0x1D
- ASEL (pin) = 1, device address = 0x53

If other devices are connected to the same I²C bus, the nominal operating voltage level of these other devices cannot exceed V_{DDIO} by more than 0.3 V. External pull-up resistors, R_p, are necessary for proper I²C operation.

READING ACCELERATION OR TEMPERATURE DATA FROM THE INTERFACE

Acceleration data is left justified and has a register address order of most significant data to least significant data, which allows the user to use multibyte transfers and to take only as much data as required—either 8 bits, 16 bits, or 20 bits, plus the marker. Temperature data is 12 bits unsigned, right justified. The ADXL357 temperature value is split over two bytes, but is not double-buffered, meaning the value can update between readings of the two registers. The data in XDATA, YDATA, and ZDATA is always the most recent available. It is not guaranteed that XDATA, YDATA, and ZDATA form a set corresponding to one sample point in time. The routine used to retrieve the data from the device controls this data set continuity. If data transfers are initiated when the DATA_RDY bit goes high and completes in a time approximately equal to 1/ODR, XDATA, YDATA, and ZDATA apply to the same data set.

For multibyte read or write transactions through either serial interface, the internal register address auto-increments. When the top of the register address range, 0x3FF, is reached the auto-increment stops and does not wrap back to Hexadecimal Address 0x00.

The address auto-increment function disables when the FIFO address is used, so that data can be read continuously from the FIFO as a multibyte transaction. In cases where the starting address of a multibyte transaction is less than the FIFO address, the address auto-increments until reaching the FIFO address, and then stops at the FIFO address.

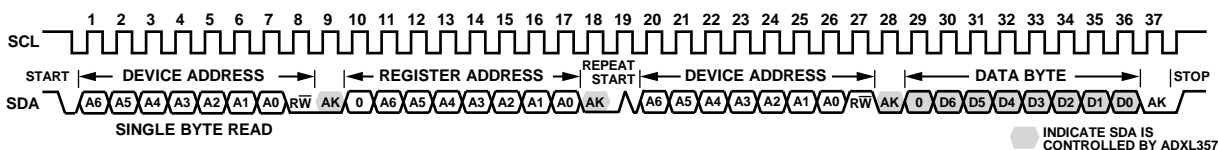


Figure 69. I²C Timing Diagram—Single-Byte Read

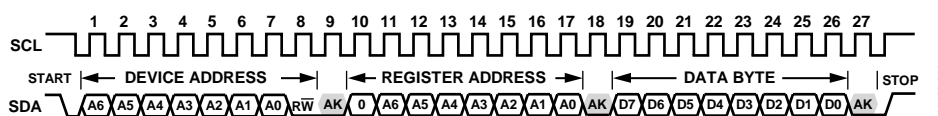


Figure 70. I²C Timing Diagram—Single-Byte Write

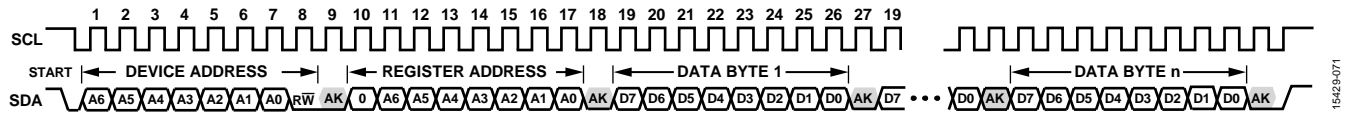


Figure 71. I²C Timing Diagram—Multibyte Write

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FIFO

FIFO operates in a stream mode; that is, when the FIFO overruns new data overwrites the oldest data in the FIFO. A read from the FIFO address guarantees that the three bytes associated with the acceleration measurement on an axis all pertain to the same measurement. If the FIFO never overflows, the data is always taken out in sets (multiples of three data points).

There are 96 21-bit locations in the FIFO. Each location contains 20 bits of data and a marker bit for the x-axis data. A single-byte read from the FIFO address pops one location from the FIFO. A multibyte read to the FIFO location pops the FIFO on the read of the first byte and every third byte read thereafter.

Figure 72 shows the organization of the data in the FIFO. The acceleration data is two's complement, 20-bit data. The FIFO control logic inserts the two virtual bits (0b00) between the data bits and the empty indicator bit. Bit 1 indicates that an attempt was made to read an empty FIFO, and that the data is not valid acceleration data. Bit 0 is a marker bit to identify the x-axis, which allows a user to verify that the FIFO data was correctly read. An acceleration data point for a given axis occupies one FIFO location. The read pointer, RD_PTR, points to the oldest stored data that was not read already from the interface (see Figure 72). There are no physical x-acceleration, y-acceleration, or z-acceleration data registers. This data also comes directly from the most recent data set in the FIFO, which points to by the z pointer, Z_PTR (see Figure 72).

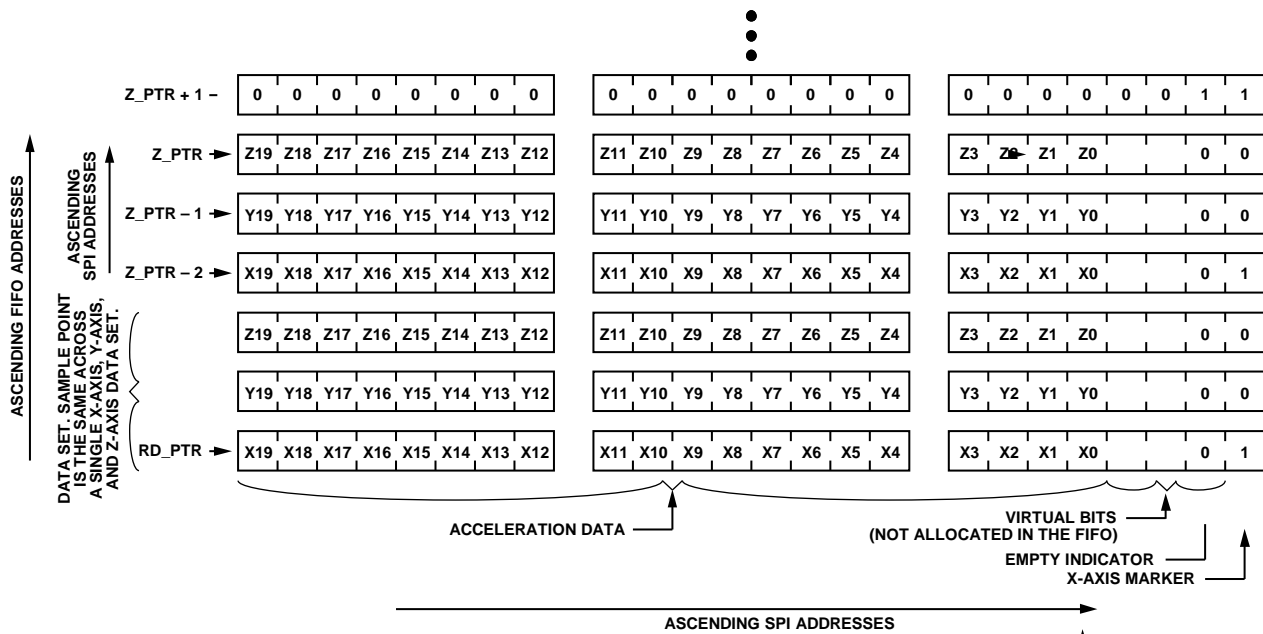


Figure 72. FIFO Data Organization

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INTERRUPTS

The status register (Register 0x04) contains five individual bits, four of which can be mapped to either the INT1 pin, the INT2 pin, or both. The polarity of the interrupt, active high or active low, is also selectable via the INT_POL bit in the range (Register 0x2C) register. In general, the status register clears when read, but this is not the case if the condition that caused the interrupt persists after the read of the register. The definition of persist varies slightly in each case, but it is described in the DATA_RDY, DRDY Pin, FIFO_FULL, FIFO_OVR, and Activity sections. The DRDY pin is similar to an interrupt pins (INTx) but clears very differently. This case is also described.

DATA_RDY

The DATA_RDY bit is set when new acceleration data is available to the interface. It clears on a read of the status register. It is not set again until acceleration data that is newer than the status register read is available.

Special logic on the clear of the DATA_RDY bit covers the corner case where new data arrives during the read of the status register. In this case, the data ready condition may be missed completely. This logic results in a delay of the clearing of DATA_RDY of up to four 512 kHz cycles.

DRDY PIN

The DRDY pin is not a status register bit; it instead behaves similar to an unmaskable interrupt. DRDY is set when new acceleration data is available to the interface. It clears on a read of the FIFO, on a read of XDATA, YDATA, or ZDATA, or by an autoclear function that occurs approximately halfway between output acceleration data sets.

DRDY is always active high. The INT_POL bit does not affect DRDY. In external sync modes (EXT_SYNC = 01, EXT_SYNC = 10), the first few DRDY pulses after initial synchronization can be lost or corrupted. The length of this potential corruption is less than the group delay.

FIFO_FULL

The FIFO_FULL bit is set when the entries in the FIFO are equal to the setting of the FIFO_SAMPLES bits. It clears as follows:

- If the number of entries in the FIFO is less than the number of samples indicated by the FIFO_SAMPLES bits, which is only the case if sufficient data is read from the FIFO.
- On a read of the status register, but only when the entries in the FIFO are less than the FIFO_SAMPLES bits.

FIFO_OVR

The FIFO_OVR bit is set when the FIFO is so far overrange that data is lost. The specified size of the FIFO is 96 locations. The FIFO_OVR is set only when there is an attempt to write past this 96 location limit.

A read of the status register clears FIFO_OVR. It is not set again until data is lost subsequent to this data register read.

ACTIVITY

The activity bit (Register 0x04, Bit 3) is set when the measured acceleration on any axis is above the ACT_THRESH bits for ACT_COUNT consecutive measurements. An overthreshold condition can shift from one axis to another on successive measurements and is still counted toward the consecutive ACT_COUNT count.

A read of the status register clears the activity bit (Register 0x04, Bit 3), but it sets again at the end of the next measurement if the activity bit (Register 0x04, Bit 3) conditions are still satisfied.

NVM_BUSY

The NVM_BUSY bit indicates that the nonvolatile memory (NVM) controller is busy, and it cannot be accessed to read, write, or generate an interrupt.

A status register read that occurs after the NVM controller is no longer busy clears NVM_BUSY.

EXTERNAL SYNCHRONIZATION AND INTERPOLATION

There are three possible synchronization options for the [ADXL357](#), shown in Figure 73 to Figure 75. For clarity, the clock frequencies and delays are drawn to scale. The labels in Figure 73 to Figure 75 are defined as follows:

- Internal ODR is the alignment of the decimated output data based on the internal clock.
- ADC CLK shows the internal master clock rate
- DRDY is an output indicator signaling a sample is ready.

The three modes are as follows:

- No external synchronization (internal clocks used)
- Synchronization with interpolation filter enabled
- Sync with an external sync and clock signals, no interpolation filter

EXT_SYNC = 00—No External Sync or Interpolation

For this case, an internal clock that serves as the synchronization master generates the data. No external signals are required, and this is used commonly when the external processor retrieves data from the device asynchronously and absolute synchronization to an external source is not required. Use Register 0x28 to program the ODR.

The device outputs a DRDY (active high) to signal that a new sample is available, and data is retrieved from the real-time registers or the FIFO. The group delay is based on the decimation setting as shown in Table 10.

EXT_SYNC = 10—External Sync with Interpolation

In this case, the internal clock generates data; however, an interpolation filter provides additional time resolution of 64 times the programmed ODR. Synchronization using interpolation filters and an external ODR clock is commonly used when the external processor can provide a synchronization signal (which is asynchronous to the internal clock) at the desired ODR. Synchronization with the interpolation filter enabled (EXT_SYNC = 10) allows the nonsynchronous external clock to output data most closely associated with the external clock rising edge. The interpolation filter provides a frequency resolution related to ODR (see Table 12).

The advantage of this mode is that data is available at a user defined sample rate and is asynchronous to the internal oscillator. The disadvantage of this mode is that the group delay is increased, with increased attenuation at the band edge. Additionally, because there is a limit to the time resolution, there is some distortion related to the mismatch of the external sync relative to the internal oscillator. This mismatch degrades spectral performance. The group delay is based on the decimation setting and interpolation setting (see Table 12). Table 13 shows the delay between the SYNC signal (input) to DRDY (output).

Table 13. EXT_SYNC = 10, DRDY Delay

ODR_LPF	Delay (Oscillator Cycles)
0x0	8
0x1	10
0x2	14
0x3	22
0x4	38
0x5	70
0x6	134
0x7	262
0x8	1031
0x9	2054
0x10	4102

Table 14. Multiplexing of INT2 and DRDY

Register or Bit Fields			Pins		Comments
EXT_CLK	EXT_SYNC[1:0]	INT_MAP[7:4]	INT2 (Pin 13)	DRDY (Pin 14)	
0	00	0000	Low	DRDY	Synchronization is to the internal clocks, and there is no external clock synchronization.
0	00	Not 0000	INT2	DRDY	
1	00	0000	EXT_CLK	DRDY	
1	00	Not 0000 ²	EXT_CLK	DRDY	
0	01	0000	DRDY	SYNC	These options reset the digital filters on every synchronization pulse and are not recommended.
0	01 ¹	Not 0000	INT2	SYNC	
1	01 ¹	0000	EXT_CLK	SYNC	External synchronization, no interpolation filter, and DRDY (active high) signals that data is ready. Data represents a sample point group delay earlier in time.
1	01 ¹	Not 0000 ²	EXT_CLK	SYNC	
0	10	0000	DRDY	SYNC	External synchronization, interpolation filter, and DRDY (active high) signals that data is ready. Data sample group delay earlier in time.
0	10 ¹	Not 0000	INT2	SYNC	
1	10 ¹	0000	EXT_CLK	SYNC	
1	10 ¹	Not 0000	EXT_CLK	SYNC	

¹ No DRDY.

² No INT2, even though it is enabled.

EXT_SYNC = 01—External Sync and External Clock, No Interpolation Filter

In this case, an external source provides an external clock at a frequency of $4 \times 64 \times \text{ODR}$. The external clock becomes the master clock source for the device. In addition, an external synchronization signal is needed to align the decimation filter output to a specific clock edge, which provides full external synchronization and is commonly used when a fixed external clock captures and processes data, and asynchronous clocks are not allowed. When using multiple sensors, synchronization with an external master clock is beneficial and requires time alignment.

When configured for EXT_SYNC = 01 with an ODR of 4 kHz, the user must supply an external clock at 1.024 MHz ($64 \times 4 \times 4 \text{ kHz}$) on the INT2 pin (Pin 13), and an external synchronization on DRDY pin (Pin 14), as shown in Table 14.

Special restrictions when using this mode include the following:

- An external clock (EXT_CLK) must be provided as well as an external sync.
- The frequency of EXT_CLK must be exactly $4 \times 64 \times \text{ODR}$.
- The width of sync must be a minimum of four EXT_CLK periods.
- The phase of sync must meet an approximate 25 ns setup time to the EXT_CLK rising edge.

When using the EXT_SYNC mode and without providing sync, the device runs on its own synchronization. Similarly, after synchronization, the device continues to run synchronized to the last sync pulse it received, which means that EXT_SYNC = 01 mode can be used with only a single synchronization pulse.

The interpolation filter provides a frequency resolution related to the ODR (see Table 12). In this case, the data provided corresponds to the external signal, which can be greater than the set ODR, but the output pass band remains the same it was prior to the interpolation filter.

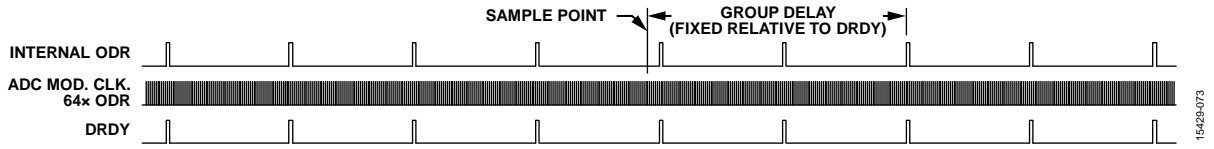


Figure 73. External Synchronization Option—EXT_SYNC = 00, Internal Sync

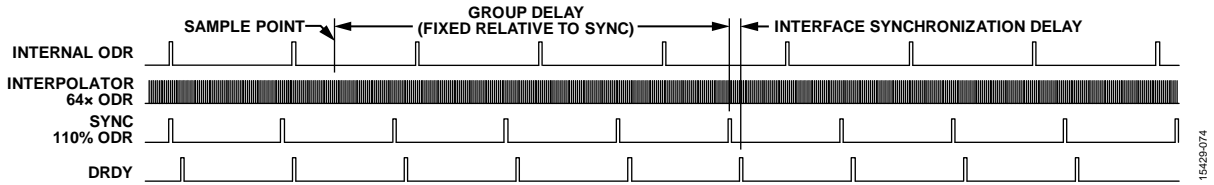


Figure 74. External Synchronization Option—EXT_SYNC = 10, External Sync, External Clock, Interpolation Filter

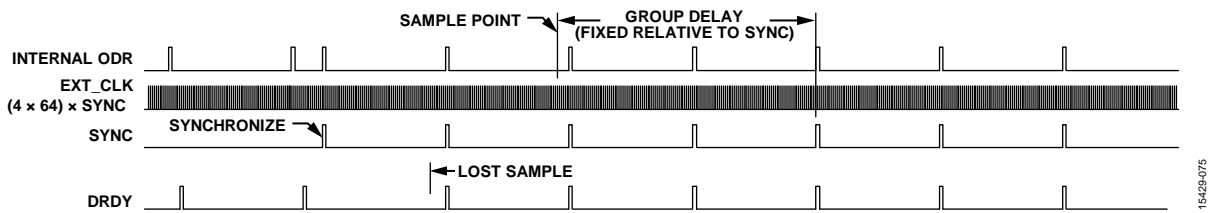


Figure 75. External Synchronization Option—EXT_SYNC = 01, External Sync, No Interpolation Filter

ADXL357 REGISTER MAP

Note that while configuring the ADXL357 in an application, all configuration registers must be programmed before enabling measurement mode in the POWER_CTL register. When the ADXL357 is in measurement mode, only the following configurations can change: the HPF_CORNER bits in the filter register, the INT_MAP register, the ST1 and ST2 bits in the SELF_TEST register, and the reset register.

Table 15. ADXL357 Register Map

Hex. Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W	
0x00	DEVID_AD	DEVID_AD								0xAD	R	
0x01	DEVID_MST	DEVID_MST								0x1D	R	
0x02	PARTID	PARTID								0xED	R	
0x03	REVID	REVID								0x01	R	
0x04	Status	Reserved			NVM_BUSY	Activity	FIFO_OVR	FIFO_FULL	DATA_RDY	0x00	R	
0x05	FIFO_ENTRIES	Reserved	FIFO_ENTRIES								0x00	R
0x06	TEMP2	Reserved				Temperature, Bits[11:8]				0x00	R	
0x07	TEMP1	Temperature, Bits[7:0]								0x00	R	
0x08	XDATA3	XDATA, Bits[19:12]								0x00	R	
0x09	XDATA2	XDATA, Bits[11:4]								0x00	R	
0x0A	XDATA1	XDATA, Bits[3:0]				Reserved				0x00	R	
0x0B	YDATA3	YDATA, Bits[19:12]								0x00	R	
0x0C	YDATA2	YDATA, Bits[11:4]								0x00	R	
0x0D	YDATA1	YDATA, Bits[3:0]				Reserved				0x00	R	
0x0E	ZDATA3	ZDATA, Bits[19:12]								0x00	R	
0x0F	ZDATA2	ZDATA, Bits[11:4]								0x00	R	
0x10	ZDATA1	ZDATA, Bits[3:0]				Reserved				0x00	R	
0x11	FIFO_DATA	FIFO_DATA								0x00	R	
0x1E	OFFSET_X_H	OFFSET_X, Bits[15:8]								0x00	R/W	
0x1F	OFFSET_X_L	OFFSET_X, Bits[7:0]								0x00	R/W	
0x20	OFFSET_Y_H	OFFSET_Y, Bits[15:8]								0x00	R/W	
0x21	OFFSET_Y_L	OFFSET_Y, Bits[7:0]								0x00	R/W	
0x22	OFFSET_Z_H	OFFSET_Z, Bits[15:8]								0x00	R/W	
0x23	OFFSET_Z_L	OFFSET_Z, Bits[7:0]								0x00	R/W	
0x24	ACT_EN	Reserved					ACT_Z	ACT_Y	ACT_X	0x00	R/W	
0x25	ACT_THRESH_H	ACT_THRESH, Bits[15:8]								0x00	R/W	
0x26	ACT_THRESH_L	ACT_THRESH, Bits[7:0]								0x00	R/W	
0x27	ACT_COUNT	ACT_COUNT								0x01	R/W	
0x28	Filter	Reserved	HPF_CORNER				ODR_LPF				0x00	R/W
0x29	FIFO_SAMPLES	Reserved	FIFO_SAMPLES								0x60	R/W
0x2A	INT_MAP	ACT_EN2	OVR_EN2	FULL_EN2	RDY_EN2	ACT_EN1	OVR_EN1	FULL_EN1	RDY_EN1	0x00	R/W	
0x2B	Sync	Reserved					EXT_CLK	EXT_SYNC			0x00	R/W
0x2C	Range	I2C_HS	INT_POL	Reserved				Range			0x81	R/W
0x2D	POWER_CTL	Reserved					DRDY_OFF	TEMP_OFF	Standby	0x01	R/W	
0x2E	SELF_TEST	Reserved							ST2	ST1	0x00	R/W
0x2F	Reset	Reset								0x00	W	

REGISTER DEFINITIONS

This section describes the functions of the [ADXL357](#) registers. The [ADXL357](#) powers up with the default register values, as shown in the Reset column of Table 15.

ANALOG DEVICES ID REGISTER

This register contains the Analog Devices ID, 0xAD.

Address: 0x00, Reset: 0xAD, Name: DEVID_AD

Table 16. Bit Descriptions for DEVID_AD

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVID_AD		Analog Devices ID	0xAD	R

ANALOG DEVICES MEMS ID REGISTER

This register contains the Analog Devices MEMS ID, 0x1D.

Address: 0x01, Reset: 0x1D, Name: DEVID_MST

Table 17. Bit Descriptions for DEVID_MST

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVID_MST		Analog Devices MEMS ID	0x1D	R

DEVICE ID REGISTER

This register contains the device ID, 0xED (355 octal).

Address: 0x02, Reset: 0xED, Name: PARTID

Table 18. Bit Descriptions for PARTID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PARTID		Device ID (355 octal)	0xED	R

PRODUCT REVISION ID REGISTER

This register contains the product revision ID, beginning with 0x00 and incrementing for each subsequent revision.

Address: 0x03, Reset: 0x01, Name: REVID

Table 19. Bit Descriptions for REVID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	REVID		Mask revision	0x01	R

STATUS REGISTER

This register includes bits that describe the various conditions of the [ADXL357](#).

Address: 0x04, Reset: 0x00, Name: Status

Table 20. Bit Descriptions for Status

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	Reserved		Reserved.	0x0	R
4	NVM_BUSY		NVM controller is busy with either refresh, programming, or built in, self test (BIST).	0x0	R
3	Activity		Activity, as defined in the ACT_THRESH_x and ACT_COUNT registers, is detected.	0x0	R
2	FIFO_OVR		FIFO has overrun, and the oldest data is lost.	0x0	R
1	FIFO_FULL		FIFO watermark is reached.	0x0	R
0	DATA_RDY		A complete x-axis, y-axis, and z-axis measurement was made and results can be read.	0x0	R

FIFO ENTRIES REGISTER

This register indicates the number of valid data samples present in the FIFO buffer. This number ranges from 0 to 96.

Address: 0x05, Reset: 0x00, Name: FIFO_ENTRIES

Table 21. Bit Descriptions for FIFO_ENTRIES

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved	0x0	R
[6:0]	FIFO_ENTRIES		Number of data samples stored in the FIFO	0x0	R

TEMPERATURE DATA REGISTERS

These two registers contain the uncalibrated temperature data. The nominal intercept is 1852 LSB at 25°C and the nominal slope is -9.05 LSB/°C. TEMP2 contains the four most significant bits, and TEMP1 contains the eight least significant bits of the 12-bit value. The [ADXL357](#) temperature value is not double-buffered, meaning the value can update between reading of the two registers.

Address: 0x06, Reset: 0x00, Name: TEMP2

Table 22. Bit Descriptions for TEMP2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	Reserved		Reserved.		
[3:0]	Temperature, Bits[11:8]		Uncalibrated temperature data	0x0	R

Address: 0x07, Reset: 0x00, Name: TEMP1

Table 23. Bit Descriptions for TEMP1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	Temperature, Bits[7:0]		Uncalibrated temperature data	0x0	R

X-AXIS DATA REGISTERS

These three registers contain the x-axis acceleration data. Data is left justified and formatted as twos complement.

Address: 0x08, Reset: 0x00, Name: XDATA3

Table 24. Bit Descriptions for XDATA3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	XDATA, Bits[19:12]		X-axis data	0x0	R

Address: 0x09, Reset: 0x00, Name: XDATA2

Table 25. Bit Descriptions for XDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	XDATA, Bits[11:4]		X-axis data	0x0	R

Address: 0x0A, Reset: 0x00, Name: XDATA1

Table 26. Bit Descriptions for XDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	XDATA, Bits[3:0]		X-axis data	0x0	R
[3:0]	Reserved		Reserved	0x0	R

Y-AXIS DATA REGISTERS

These three registers contain the y-axis acceleration data. Data is left justified and formatted as twos complement.

Address: 0x0B, Reset: 0x00, Name: YDATA3

Table 27. Bit Descriptions for YDATA3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	YDATA, Bits[19:12]		Y-axis data	0x0	R

Address: 0x0C, Reset: 0x00, Name: YDATA2

Table 28. Bit Descriptions for YDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	YDATA, Bits[11:4]		Y-axis data	0x0	R

Address: 0x0D, Reset: 0x00, Name: YDATA1

Table 29. Bit Descriptions for YDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	YDATA, Bits[3:0]		Y-axis data	0x0	R
[3:0]	Reserved		Reserved	0x0	R

Z-AXIS DATA REGISTERS

These three registers contain the z-axis acceleration data. Data is left justified and formatted as twos complement.

Address: 0x0E, Reset: 0x00, Name: ZDATA3

Table 30. Bit Descriptions for ZDATA3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ZDATA, Bits[19:12]		Z-axis data	0x0	R

Address: 0x0F, Reset: 0x00, Name: ZDATA2

Table 31. Bit Descriptions for ZDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ZDATA, Bits[11:4]		Z-axis data	0x0	R

Address: 0x10, Reset: 0x00, Name: ZDATA1

Table 32. Bit Descriptions for ZDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ZDATA, Bits[3:0]		Z-axis data	0x0	R
[3:0]	Reserved		Reserved	0x0	R

FIFO ACCESS REGISTER**Address: 0x11, Reset: 0x00, Name: FIFO_DATA**

Read this register to access data stored in the FIFO.

Table 33. Bit Descriptions for FIFO_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FIFO_DATA		FIFO data is formatted to 24 bits, 3 bytes, most significant byte first. A read to this address pops an effective three equal byte words of axis data from the FIFO. Two subsequent reads or a multibyte read completes the transaction of this data onto the interface. Continued reading or a sustained multibyte read of this field continues to pop the FIFO every third byte. Multibyte reads to this address do not increment the address pointer. If this address is read due to an auto-increment from the previous address, it does not pop the FIFO. Instead, it returns zeros and increments onto the next address.	0x0	R

X-AXIS OFFSET TRIM REGISTERS**Address: 0x1E, Reset: 0x00, Name: OFFSET_X_H****Table 34. Bit Descriptions for OFFSET_X_H**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_X, Bits[15:8]		Offset added to x-axis data after all other signal processing. Data is in twos complement format. The bit significance of OFFSET_X[15:0] matches the significance of XDATA[19:4].	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: OFFSET_X_L**Table 35. Bit Descriptions for OFFSET_X_L**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_X, Bits[7:0]		Offset added to x-axis data after all other signal processing. Data is in twos complement format. The significance of OFFSET_X[15:0] matches the significance of XDATA[19:4].	0x0	R/W

Y-AXIS OFFSET TRIM REGISTERS**Address: 0x20, Reset: 0x00, Name: OFFSET_Y_H****Table 36. Bit Descriptions for OFFSET_Y_H**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Y, Bits[15:8]		Offset added to y-axis data after all other signal processing. Data is in twos complement format. The significance of OFFSET_Y[15:0] matches the significance of YDATA[19:4].	0x0	R/W

Address: 0x21, Reset: 0x00, Name: OFFSET_Y_L**Table 37. Bit Descriptions for OFFSET_Y_L**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Y, Bits[7:0]		Offset added to y-axis data after all other signal processing. Data is in twos complement format. The significance of OFFSET_Y[15:0] matches the significance of YDATA[19:4].	0x0	R/W

Z-AXIS OFFSET TRIM REGISTERS**Address: 0x22, Reset: 0x00, Name: OFFSET_Z_H**

Table 38. Bit Descriptions for OFFSET_Z_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Z, Bits[15:8]		Offset added to z-axis data after all other signal processing. Data is in twos complement format. The significance of OFFSET_Z[15:0] matches the significance of ZDATA[19:4].	0x0	R/W

Address: 0x23, Reset: 0x00, Name: OFFSET_Z_L

Table 39. Bit Descriptions for OFFSET_Z_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Z, Bits[7:0]		Offset added to z-axis data after all other signal processing. Data is in twos complement format. The significance of OFFSET_Z[15:0] matches the significance of ZDATA[19:4].	0x0	R/W

ACTIVITY ENABLE REGISTER**Address: 0x24, Reset: 0x00, Name: ACT_EN**

Table 40. Bit Descriptions for ACT_EN

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	Reserved		Reserved.	0x0	R
2	ACT_Z		Z-axis data is a component of the activity detection algorithm.	0x0	R/W
1	ACT_Y		Y-axis data is a component of the activity detection algorithm.	0x0	R/W
0	ACT_X		X-axis data is a component of the activity detection algorithm.	0x0	R/W

ACTIVITY THRESHOLD REGISTERS**Address: 0x25, Reset: 0x00, Name: ACT_THRESH_H**

Table 41. Bit Descriptions for ACT_THRESH_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_THRESH[15:8]		Threshold for activity detection. Acceleration magnitude must be above ACT_THRESH to trigger the activity counter. ACT_THRESH is an unsigned magnitude. The significance of ACT_THRESH[15:0] matches the significance of XDATA[18:3], YDATA[18:3], and ZDATA[18:3].	0x0	R/W

Address: 0x26, Reset: 0x00, Name: ACT_THRESH_L

Table 42. Bit Descriptions for THRESH_ACT_X_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_THRESH[7:0]		Threshold for activity detection. The acceleration magnitude must be greater than the value in ACT_THRESH to trigger the activity counter. ACT_THRESH is an unsigned magnitude. The significance of ACT_THRESH[15:0] matches the bit significance of XDATA[18:3], YDATA[18:3], and ZDATA[18:3].	0x0	R/W

ACTIVITY COUNT REGISTER**Address: 0x27, Reset: 0x01, Name: ACT_COUNT**

Table 43. Bit Descriptions for ACT_COUNT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_COUNT		Number of consecutive events above threshold (from ACT_THRESH) required to detect activity	0x1	R/W

FILTER SETTINGS REGISTER**Address: 0x28, Reset: 0x00, Name: Filter**

Use this register to specify parameters for the internal high-pass and low-pass filters.

Table 44. Bit Descriptions for Filter

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved	0x0	R
[6:4]	HPF_CORNER	000 001 010 011 100 101 110	-3 dB filter corner for the first-order, high-pass filter relative to the ODR Not applicable, no high-pass filter enabled $247 \times 10^{-3} \times \text{ODR}$ $62.084 \times 10^{-3} \times \text{ODR}$ $15.545 \times 10^{-3} \times \text{ODR}$ $3.862 \times 10^{-3} \times \text{ODR}$ $0.954 \times 10^{-3} \times \text{ODR}$ $0.238 \times 10^{-3} \times \text{ODR}$	0x0	R/W
[3:0]	ODR_LPF	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010	ODR and low-pass filter corner 4000 Hz and 1000 Hz 2000 Hz and 500 Hz 1000 Hz and 250 Hz 500 Hz and 125 Hz 250 Hz and 62.5 Hz 125 Hz and 31.25 Hz 62.5 Hz and 15.625 Hz 31.25 Hz and 7.813 Hz 15.625 Hz and 3.906 Hz 7.813 Hz and 1.953 Hz 3.906 Hz and 0.977 Hz	0x0	R/W

FIFO SAMPLES REGISTER**Address: 0x29, Reset: 0x60, Name: FIFO_SAMPLES**

Use the FIFO_SAMPLES value to specify the number of samples to store in the FIFO. The default value of this register is 0x60 to avoid triggering the FIFO watermark interrupt.

Table 45. Bit Descriptions for FIFO_SAMPLES

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved.	0x0	R
[6:0]	FIFO_SAMPLES		Watermark number of samples stored in the FIFO that triggers a FIFO_FULL condition. Values range from 1 to 96.	0x60	R/W

INTERRUPT PIN (INTx) FUNCTION MAP REGISTER**Address: 0x2A, Reset: 0x00, Name: INT_MAP**

The INT_MAP register configures the interrupt pins. Bits[7:0] select which functions generate an interrupt on the INT1 and INT2 pins. Multiple events can be configured. If the corresponding bit is set to 1, the function generates an interrupt on the interrupt pins.

Table 46. Bit Descriptions for INT_MAP

Bits	Bit Name	Settings	Description	Reset	Access
7	ACT_EN2		Activity interrupt enable on INT2	0x0	R/W
6	OVR_EN2		FIFO_OVR interrupt enable on INT2	0x0	R/W
5	FULL_EN2		FIFO_FULL interrupt enable on INT2	0x0	R/W
4	RDY_EN2		DATA_RDY interrupt enable on INT2	0x0	R/W
3	ACT_EN1		Activity interrupt enable on INT1	0x0	R/W
2	OVR_EN1		FIFO_OVR interrupt enable on INT1	0x0	R/W
1	FULL_EN1		FIFO_FULL interrupt enable on INT1	0x0	R/W
0	RDY_EN1		DATA_RDY interrupt enable on INT1	0x0	R/W

DATA SYNCHRONIZATION**Address: 0x2B, Reset: 0x00, Name: Sync**

Use this register to control the external timing triggers.

Table 47. Bit Descriptions for Sync

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	Reserved		Reserved.	0x0	R
2	EXT_CLK		Enable external clock. See Table 14. Multiplexing of INT2 and DRDY Table 14 for configuration details.	0x0	R/W
[1:0]	EXT_SYNC	00 01 10 11	Enable external sync control. Internal sync. External sync, no interpolation filter. After synchronization, and for EXT_SYNC within specification, DATA_RDY occurs on EXT_SYNC. External sync, interpolation filter, next available data indicated by DATA_RDY 14 to 8204 oscillator cycles later (longer delay for higher ODR_LPF setting), data represents a sample point group delay earlier in time. Reserved.	0x0	R/W

I²C SPEED, INTERRUPT POLARITY, AND RANGE REGISTER**Address: 0x2C, Reset: 0x81, Name: Range****Table 48. Bit Descriptions for Range**

Bits	Bit Name	Settings	Description	Reset	Access
7	I2C_HS	1 0	I ² C speed. High speed mode. Fast mode.	0x1	R/W
6	INT_POL	0 1	Interrupt polarity. INT1 and INT2 are active low. INT1 and INT2 are active high.	0x0	R/W
[5:2]	Reserved		Reserved.	0x0	R
[1:0]	Range	01 10 11	Range. ±10 g. ±20 g. ±40 g.	0x1	R/W

POWER CONTROL REGISTER**Address: 0x2D, Reset: 0x01, Name: POWER_CTL****Table 49. Bit Descriptions for POWER_CTL**

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	Reserved		Reserved.	0x0	R
2	DRDY_OFF		Set to 1 to force the DRDY output to 0 in modes where it is normally signal data ready.	0x0	R/W
1	TEMP_OFF		Set to 1 to disable temperature processing. Temperature processing is also disabled when standby = 1.	0x0	R/W
0	Standby	1 0	Standby or measurement mode. Standby mode. In standby mode, the device is in a low power state, and the temperature and acceleration datapaths are not operating. In addition, digital functions, including FIFO pointers, reset. Changes to the configuration setting of the device must be made when standby = 1. An exception is a high-pass filter that can be changed when the device is operating. Measurement mode.	0x1	R/W

SELF TEST REGISTER**Address: 0x2E, Reset: 0x00, Name: SELF_TEST**

Refer to the Self Test section for more information on the operation of the self test feature.

Table 50. Bit Descriptions for SELF_TEST

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	Reserved		Reserved.	0x0	R
1	ST2		Set to 1 to enable self test force	0x0	R/W
0	ST1		Set to 1 to enable self test mode	0x0	R/W

RESET REGISTER**Address: 0x2F, Reset: 0x00, Name: Reset****Table 51. Bit Descriptions for Reset**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	Reset		Write Code 0x52 to resets the device, similar to a power-on reset (POR)	0x0	W

PCB FOOTPRINT PATTERN

Figure 76 shows the PCB footprint pattern and dimensions in millimeters.

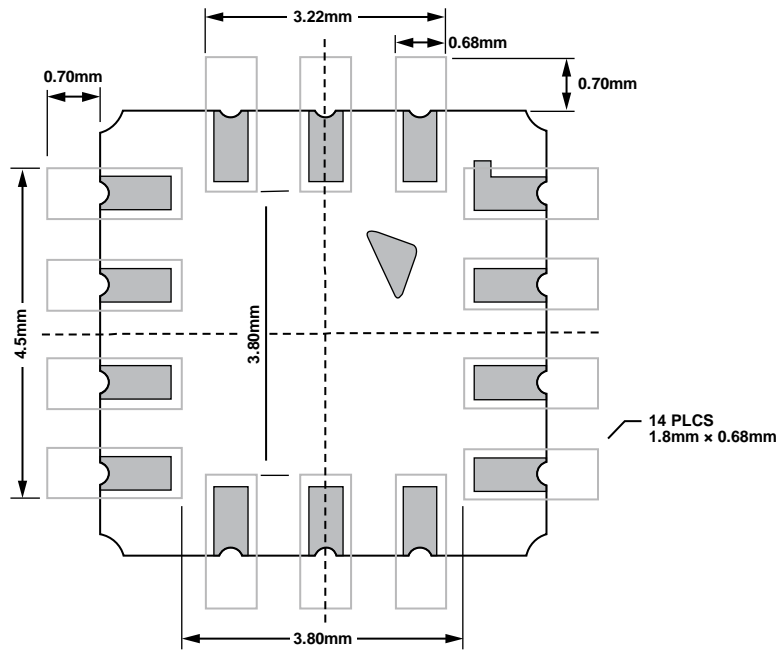


Figure 76. PCB Footprint Pattern and Dimensions in Millimeters

15423-076

OUTLINE DIMENSIONS

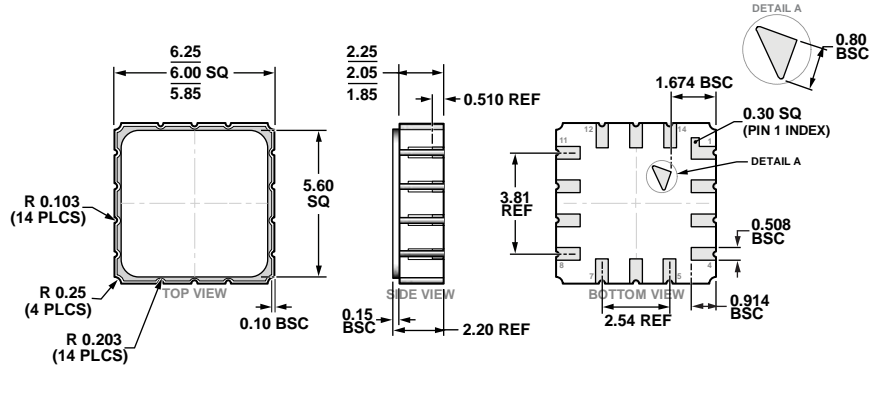


Figure 77. 14-Terminal Ceramic Leadless Chip Carrier [LCC] (E-14-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Output Mode	Measurement Range (g)	Specified Voltage (V)	Temperature Range	Package Description	Package Option
ADXL356BEZ	Analog	±10, ±20	3.3	-40°C to +125°C	14-Terminal LCC	E-14-1
ADXL356BEZ-RL	Analog	±10, ±20	3.3	-40°C to +125°C	14-Terminal LCC, 13" Reel	E-14-1
ADXL356BEZ-RL7	Analog	±10, ±20	3.3	-40°C to +125°C	14-Terminal LCC, 7" Reel	E-14-1
ADXL356CEZ	Analog	±10, ±40	3.3	-40°C to +125°C	14-Terminal LCC	E-14-1
ADXL356CEZ-RL	Analog	±10, ±40	3.3	-40°C to +125°C	14-Terminal LCC, 13" Reel	E-14-1
ADXL356CEZ-RL7	Analog	±10, ±40	3.3	-40°C to +125°C	14-Terminal LCC, 7" Reel	E-14-1
ADXL357BEZ	Digital	±10.24, ±20.48, ±40.96	3.3	-40°C to +125°C	14-Terminal LCC	E-14-1
ADXL357BEZ-RL	Digital	±10.24, ±20.48, ±40.96	3.3	-40°C to +125°C	14-Terminal LCC	E-14-1
ADXL357BEZ-RL7	Digital	±10.24, ±20.48, ±40.96	3.3	-40°C to +125°C	14-Terminal LCC	E-14-1
EVAL-ADXL356BZ					Evaluation Board for ADXL356B	
EVAL-ADXL356CZ					Evaluation Board for ADXL356C	
EVAL-ADXL357Z					Evaluation Board for ADXL357	

¹Z = RoHS Compliant Part.