TC7660H

High Frequency DC-to-DC Voltage Converter

Features

- Pin Compatible with 7660, High Frequency Performance DC-to-DC Converter
- Low Cost, Two Low Value External Capacitors Required (1.0 µF)
- Converts +5V Logic Supply to ±5V System
- Wide Input Voltage Range 1.5V to 10V
- Voltage Conversion 99.7%
- Power Efficiency 85%
- Available in 8-Pin SOIC and 8-Pin PDIP Packages

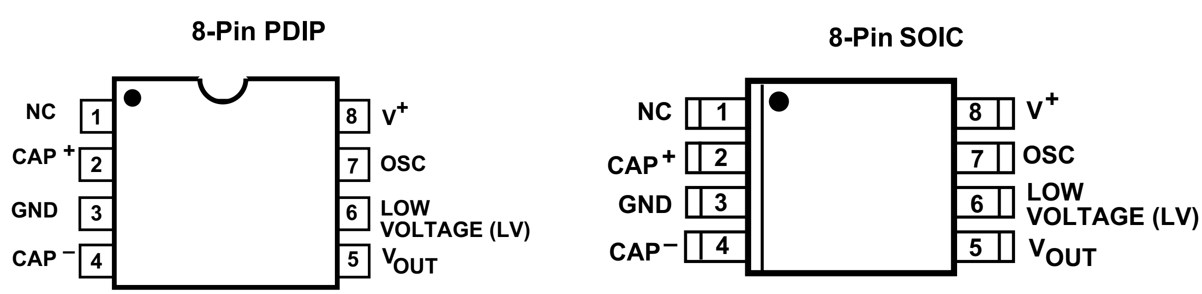
General Description

The TC7660H is a pin-compatible, high-frequency upgrade to the industry standard TC7660 charge pump voltage converter. It converts a +1.5V to +10V input to a corresponding -1.5V to -10V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI.

The TC7660H operates at a frequency of 120 kHz (versus 10 kHz for the TC7660), allowing the use of 1.0 µF external capacitors. Oscillator frequency can be reduced (for lower supply current applications) by connecting an external capacitor from OSC to ground.

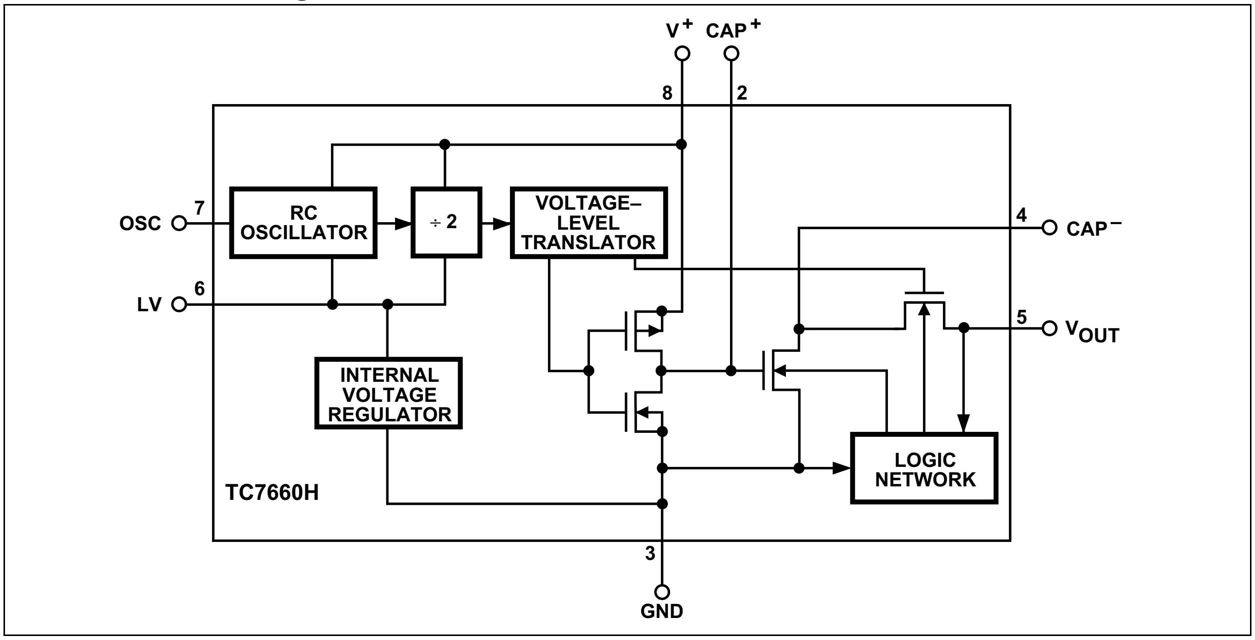
The TC7660H is available in 8-pin DIP and small outline (SOIC) packages in commercial and extended temperature ranges.

Package Types



NC = No Internal Connection

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage .... +10.5V
LV and OSC Inputs Voltage (Note 1) .... -0.3V to (V^+ + 0.3V) for V^+ < 5.5V
.... (V^+ – 5.5V) to (V^+ + 0.3V) for V^+ > 5.5V
Current Into LV (Note 1) .... 20 µA for V^+ > 3.5V
Output Short Duration (V_{SUPPLY} ≤ 5.5V) .... Continuous
Power Dissipation (T_A ≤ +70°C) (Note 2)
PDIP .... 730 mW
SOIC .... 470 mW
Operating Temperature Range
C Suffix .... 0°C to +70°C
E Suffix .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

† **Notice:** Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over Operating Temperature Range with V^+= 5V, C_1 = C_2 = 1 µF, C_{OSC} = 0, Test Circuit (Figure 4-1), unless otherwise indicated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current	I^+	—	0.46	1	mA	R_L = ∞
Supply Voltage Range, High	V_H^+	3	—	10	V	Min ≤ T_A ≤ Max, R_L = 5 kΩ, LV Open
Supply Voltage Range, Low	V_L^+	1.5	—	3.5	V	Min ≤ T_A ≤ Max, R_L = 5 kΩ, LV to GND
Output Source Resistance	R_{OUT}	—	55	80	Ω	I_{OUT} = 20 mA, T_A = 25°C
		—	—	95		I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C (C Device)
		—	—	110		I_{OUT} = 20 mA, -40°C ≤ T_A ≤ +85°C (E Device)
		—	150	250		V^+ = 2V, I_{OUT} = 3 mA, LV to GND, 0°C ≤ T_A ≤ +70°C
Oscillator Frequency	F_{OSC}	—	120	—	kHz	
Switching Frequency (**Note 3**)	F_{SW}	—	60	—	kHz	
Power Efficiency	P_{EFF}	81	85	—	%	I_{OUT} = 10 mA, Min ≤ T_A ≤ Max
Voltage Efficiency	V_{EFF}	99	99.7	—	%	R_L = ∞

Note 1: Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the TC7660H.

2: Derate linearly above 50°C by 5.5 mW/°C.

3: The pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

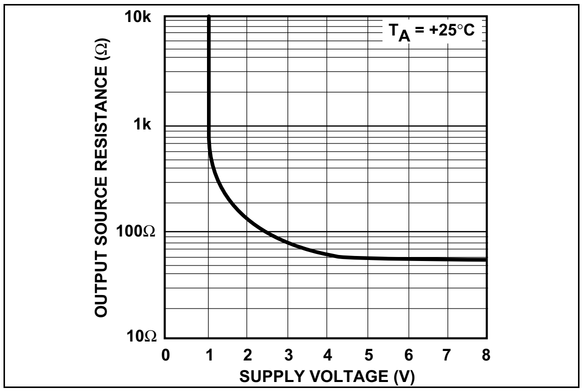


FIGURE 2-1: *Output Source Resistance vs. Supply Voltage.*

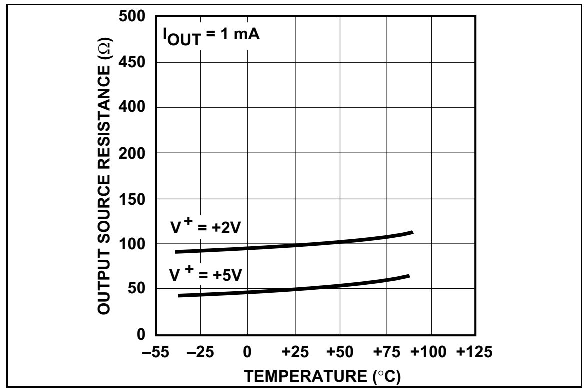


FIGURE 2-3: *Output Source Resistance vs. Temperature.*

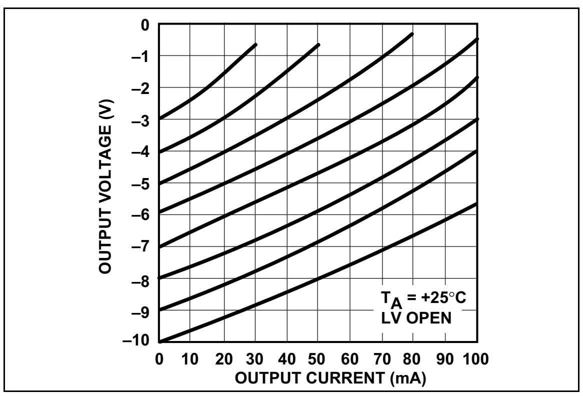


FIGURE 2-2: *Output Voltage vs. Output Current ($C_1 = C_2 = 1\ \mu F$).*

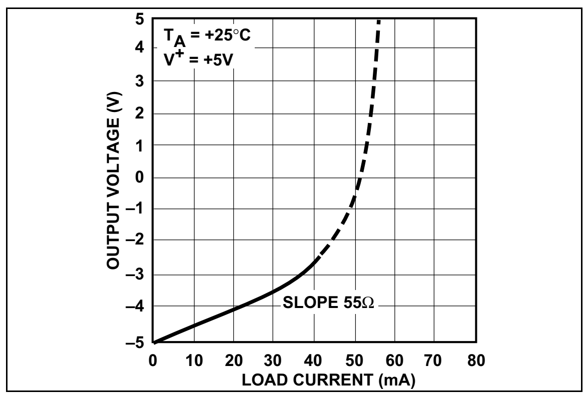


FIGURE 2-4: *Output Voltage vs. Load Current.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

PDIP, SOIC	Symbol	Description
1	NC	No connection
2	CAP^+	Charge pump capacitor positive terminal
3	GND	Ground terminal
4	CAP^-	Charge pump capacitor negative terminal
5	V_{OUT}	Output voltage
6	LV	Low Voltage pin. Connect to GND for V+ < 3.5V.
7	OSC	Oscillator control input. Bypass with an external capacitor to slow the oscillator.
8	V^+	Power supply positive voltage input

4.0 APPLICATIONS INFORMATION

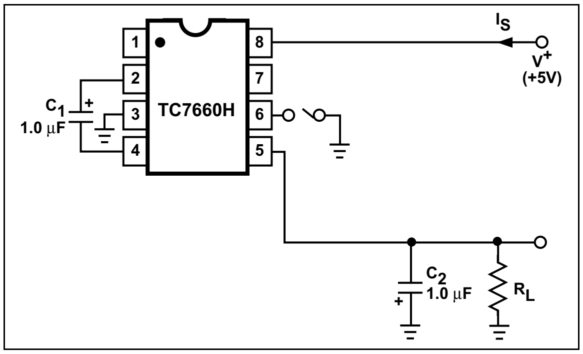


FIGURE 4-1: *TC7660H Test Circuit.*

4.1 Detailed Description

The TC7660H contains all the necessary circuitry to implement a voltage inverter, with the exception of two external capacitors, which may be inexpensive 1.0 µF non-polarized capacitors. Operation is best understood by considering Figure 4-2, which shows an idealized voltage inverter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed.

Note:	Switches S_2 and S_4 are open during this half cycle.

During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

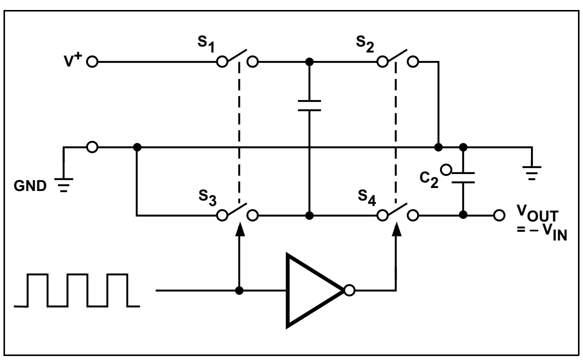


FIGURE 4-2: *Idealized Charge Pump Inverter.*

To improve low-voltage operation, the LV pin should be connected to GND. For supply voltages greater than 3.5V, the LV terminal **must be left open to ensure latch-up-proof operation and prevent device damage**.

4.2 Theoretical Power Efficiency Considerations

In theory, a capacitative charge pump can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660H approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2 \times C_1 \times (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4-1), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

4.3 Do's and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7660H and the + terminal of C_2 must be connected to GND Pin 3.

4.4 Simple Negative Voltage Converter

Figure 4-3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 4-3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of -10 mA and a supply voltage of +5V, the output voltage would be -4.3V.

The dynamic output impedance of the TC7660H is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f \times C_1} = 2.12\Omega$$

Where:

f = 150 kHz

C_1 = 1.0 µF

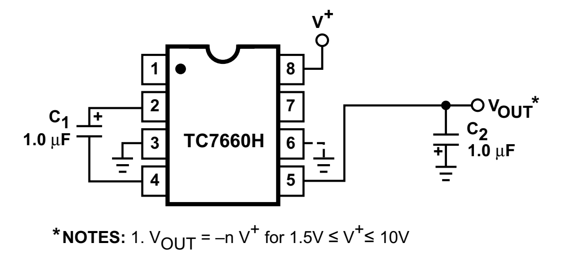


FIGURE 4-3: *Simple Negative Converter.*

4.5 Paralleling Devices

Any number of TC7660H voltage converters may be paralleled to reduce output resistance (Figure 4-4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}(of\ TC7660H)}{n\,(number\ of\ devices)}$$

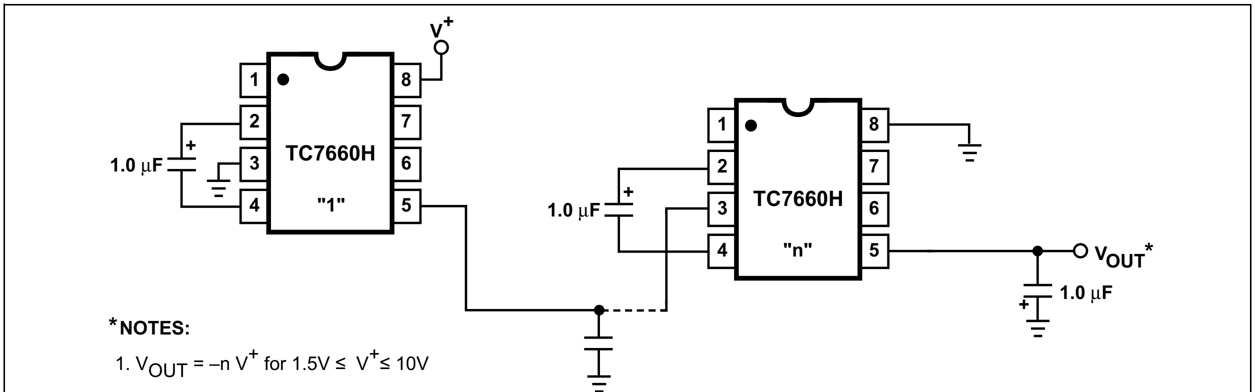


FIGURE 4-4: *Increased Output Voltage by Cascading Devices.*

4.6 Cascading Devices

The TC7660H may be cascaded as shown in Figure 4-4 to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is probably 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n \times (V_{IN})$$

Where:

n = an integer representing the number of devices cascaded

The resulting output resistance would be approximately the weighted sum of the individual TC7660H R_{OUT} values.

4.7 Changing the TC7660H Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase or decrease the oscillator frequency. This can be achieved by overdriving the oscillator from an external clock, as shown in Figure 4-6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

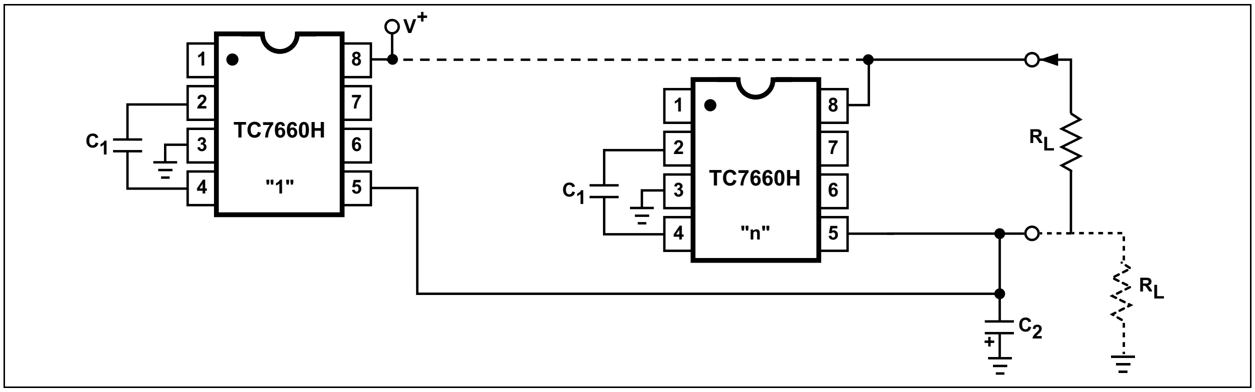


FIGURE 4-5: *Paralleling Devices Lowers Output Impedance.*

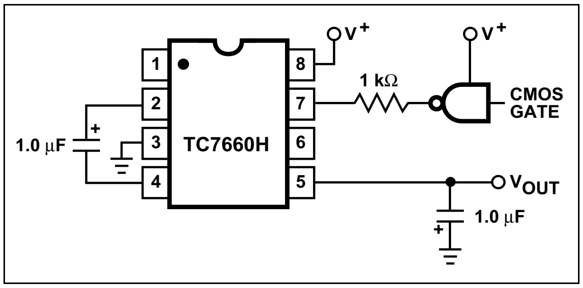


FIGURE 4-6: *External Clocking.*

4.8 Positive Voltage Multiplication

The TC7660H may be employed to achieve positive voltage multiplication using the circuit shown in Figure 4-7. In this application, the pump inverter switches of the TC7660H are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\ V^+) - (2\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

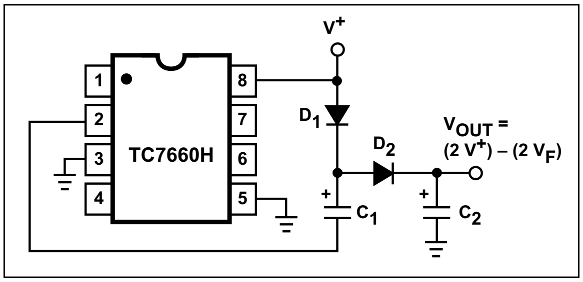


FIGURE 4-7: *Positive Voltage Multiplier.*

4.9 Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 4-8 combines the functions shown in Figure 4-3 and Figure 4-7 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration, which combines both functions; however, the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

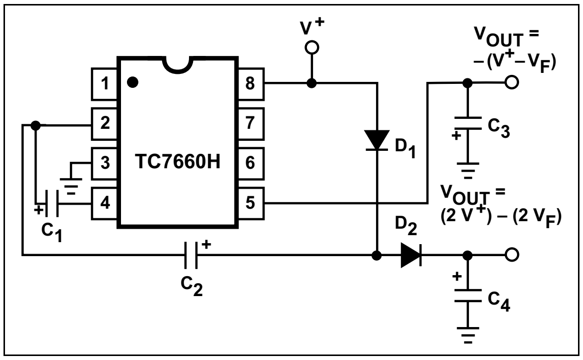


FIGURE 4-8: *Combined Negative Converter and Positive Multiplier.*

4.10 Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 4-9 shows a TC7660H transforming -5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switchdrive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 4-9, could be used to start this circuit up, after which it will bypass the diode and resistor shown dotted in Figure 4-9.

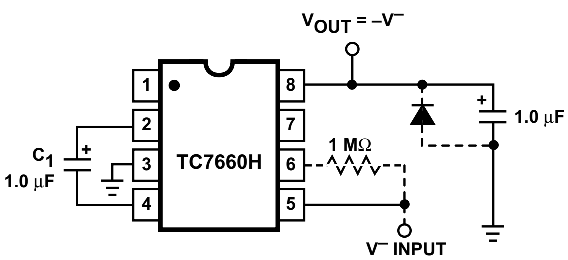
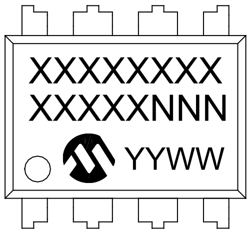


FIGURE 4-9: *Positive Voltage Conversion.*

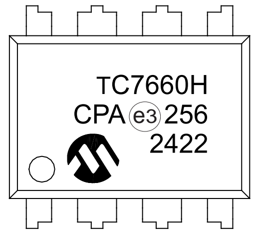
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

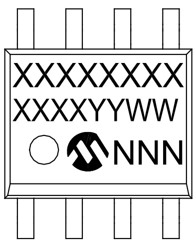
8-Lead PDIP (300 mil)



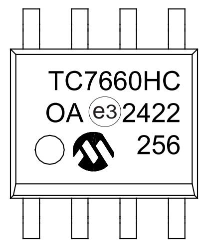
Example



8-Lead SOIC (3.90 mm)



Example

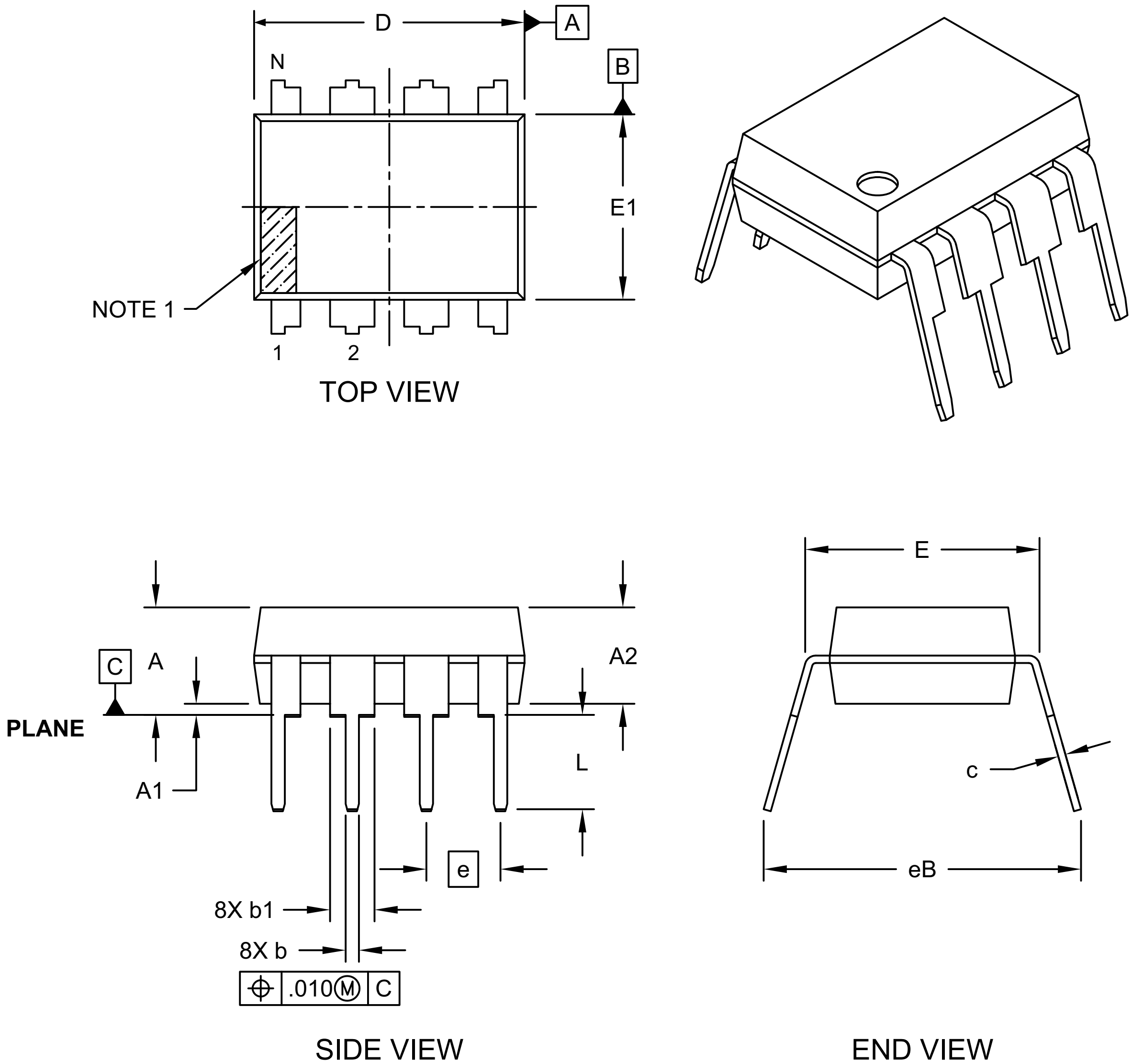


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP]
Atmel Legacy Package

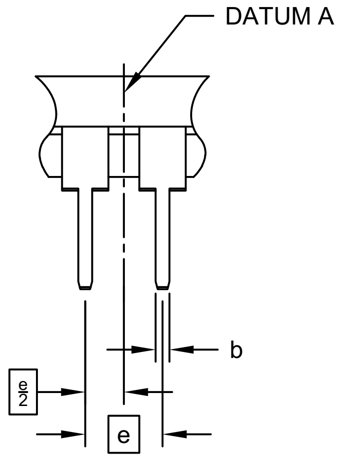
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



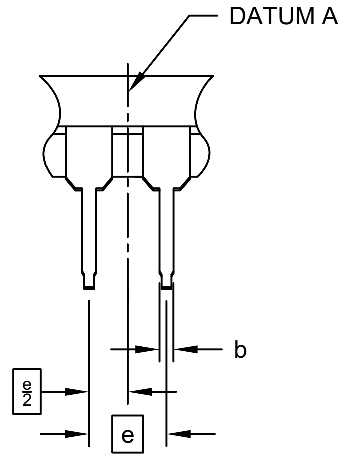
Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 1 of 2

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP] Atmel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



ALTERNATE LEAD DESIGN
(NOTE 5)



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

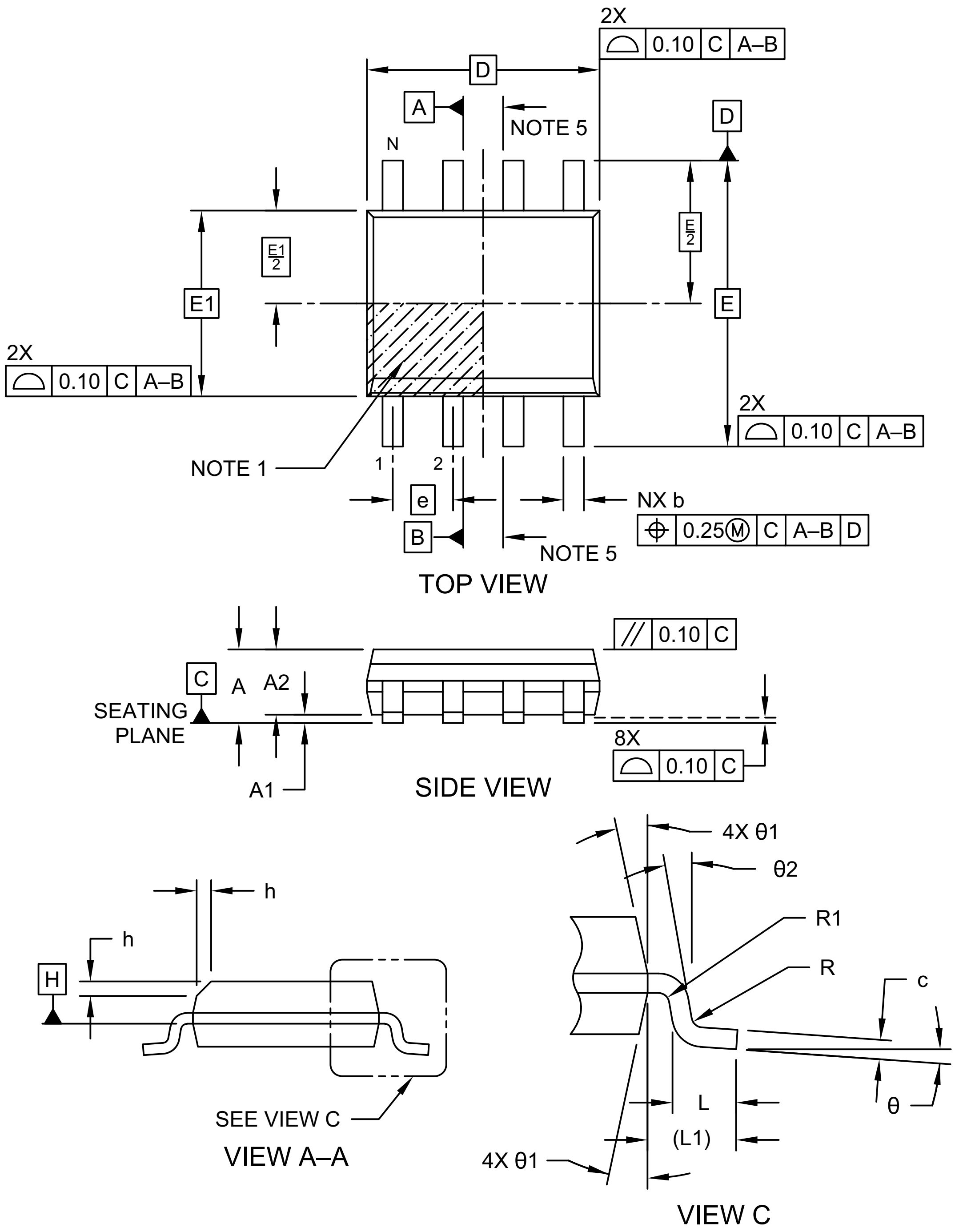
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

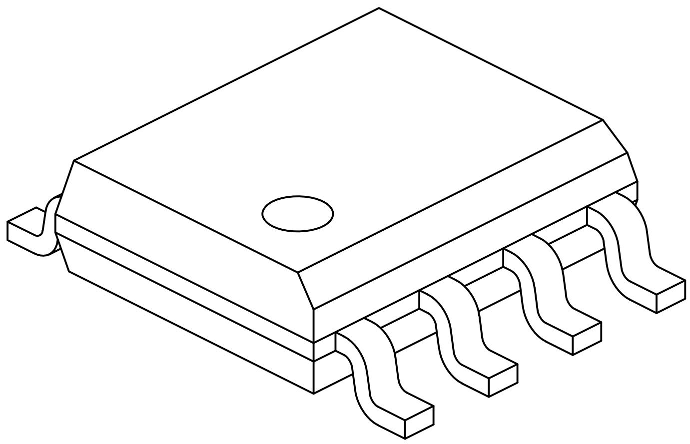
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

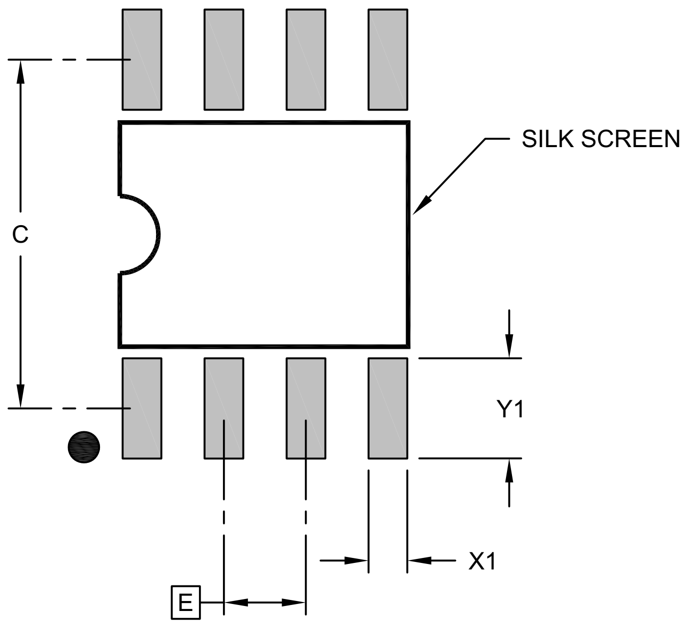
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (November 2024)

- Added “Switching Frequency” parameter to Electrical Characteristics table.
- Updated the Package Outline Drawings and Package Marking Information in **Section 5.0 “Packaging Information”** to current document formatting; physical package is the same.
- Added **Section “Product Identification System”** and **Appendix A: “Revision History”**.
- Minor changes throughout the document.

Revision A (2001)

- Initial release of the document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX(1)
Device	Temperature Range	Package Options	Media Type

Device: TC7660H: High Frequency DC-to-DC Voltage Converter

Temperature Range:
C = 0°C to +70°C
E = -40°C to +85°C

Package Options:
PA = 8-Lead PDIP (300 mil Body)
OA = 8-Lead SOIC (150 mil Body)

Media Type:
Blank= Tube, 60 per Tube (8-Lead PDIP option only)
Blank= Tube, 100 per Tube (8-Lead SOIC option only)
713 = Tape and Reel, 3300 per Reel

Examples:

a) TC7660HCPA: High Frequency DC-to-DC Voltage Converter, 0°C to +70°C, 8-Lead PDIP package, 60 per Tube.

b) TC7660HEOA: High Frequency DC-to-DC Voltage Converter, -40°C to +85°C, 8-Lead SOIC package, 100 per Tube.

c) TC7660HEOA713: High Frequency DC-to-DC Voltage Converter, -40°C to +85°C, 8-Lead SOIC package, Tape and Reel, 3300/Reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

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