CMOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B – – – BCD Type

CD4516B – – – Binary Type

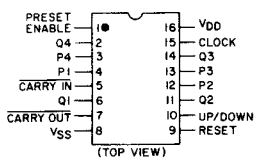
■ CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. **(See Fig. 15).**

These devices are similar to types MC14510 and MC14516.

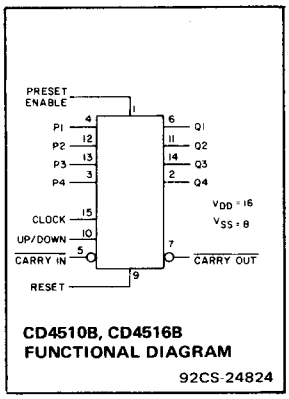
The CD4510B and CD4516B Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



CD4510B, CD4516B TERMINAL ASSIGNMENT

Features:

- **Medium-speed operation -- f_{CL} = 8 MHz typ. at 10 V**
- **Synchronous internal carry propagation**
- **Reset and Preset capability**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4510B, CD4516B FUNCTIONAL DIAGRAM

92CS-24824

Applications:

- **Up/Down difference counting**
- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	150	–	ns
	10	75	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Preset Enable or Reset Removal Time•	5	150	–	ns
	10	80	–	
	15	60	–	
Clock Rise and Fall Time, t_rCL, t_fCL *	5	–	15	μs
	10	–	5	
	15	–	5	
Carry-In Setup Time, t_S	5	130	–	ns
	10	60	–	
	15	45	–	
Up-Down Setup Time, t_S	5	360	–	ns
	10	160	–	
	15	110	–	
Preset Enable or Reset Pulse Width, t_W	5	220	–	ns
	10	100	–	
	15	75	–	

•Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

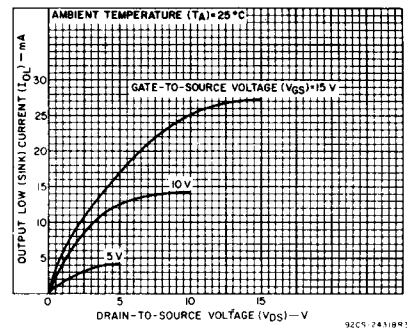


Fig.1 – Typical output low (sink) current characteristics.

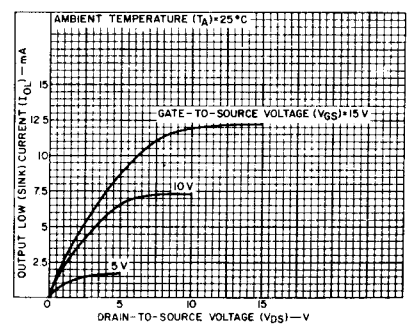


Fig.2 – Minimum output low (sink) current characteristics.

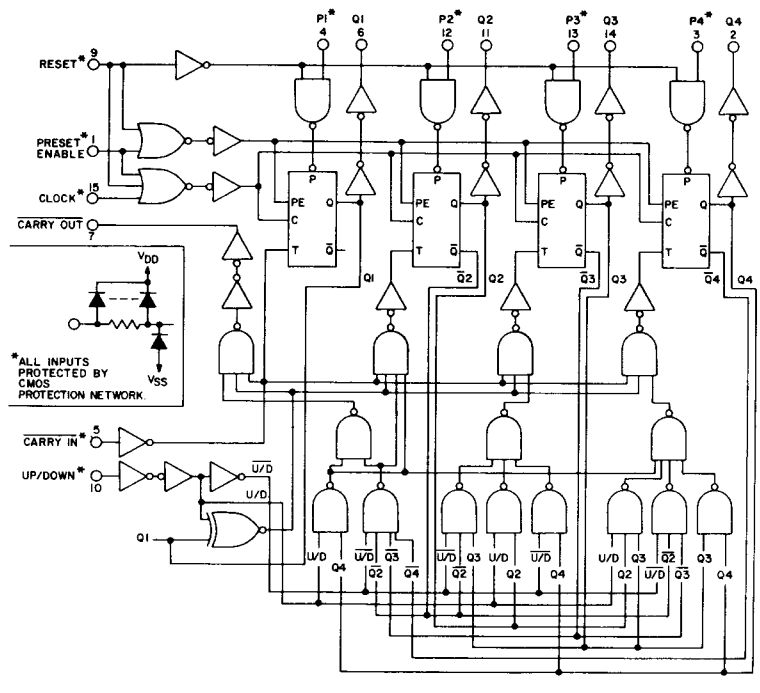


Fig.3 – Logic Diagram for CD4510B.

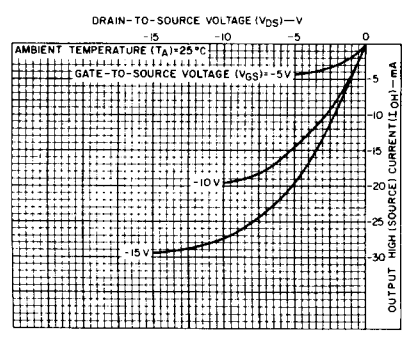


Fig.4 – Typical output high (source) current characteristics.

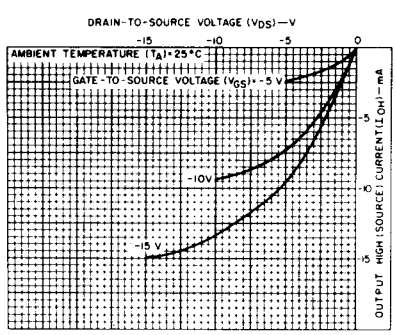


Fig.5 – Minimum output high (source) current characteristics.

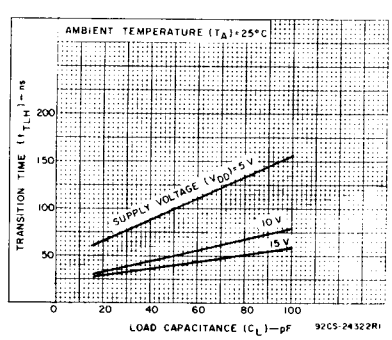


Fig.6 – Typical transition time vs. load capacitance.

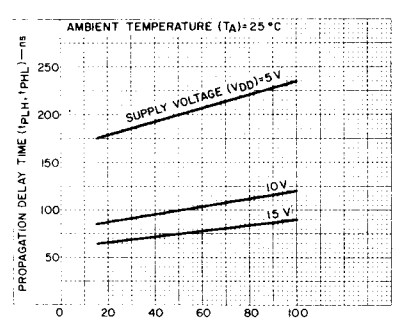


Fig.7 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

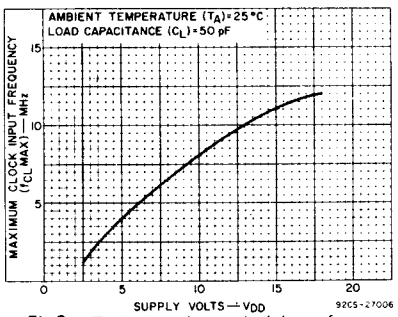


Fig.8 – Typical maximum clock input frequency vs. supply voltage.

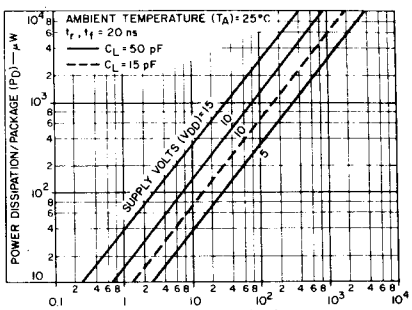


Fig.9 – Typical dynamic power dissipation vs. frequency.

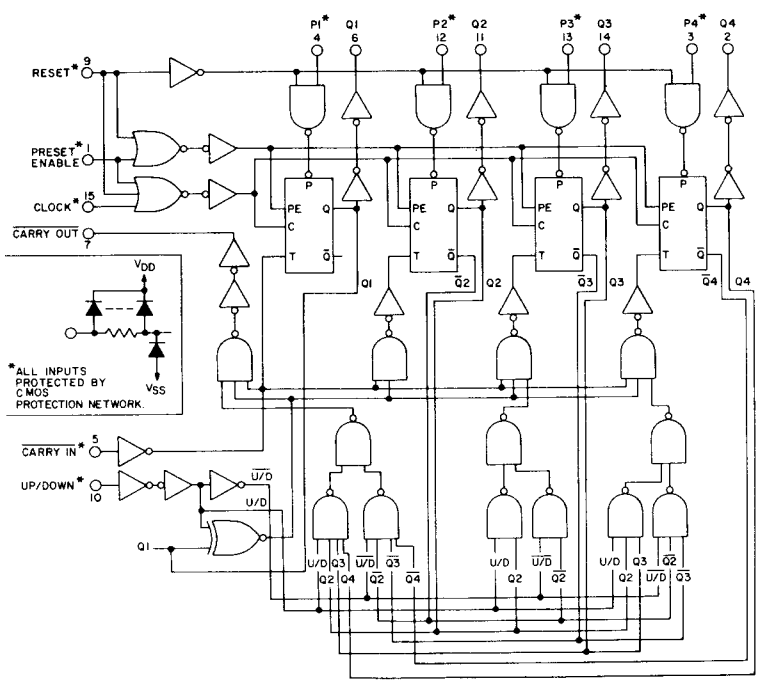


Fig.10 – Logic Diagram for CD4516B. 92CL-27504R2

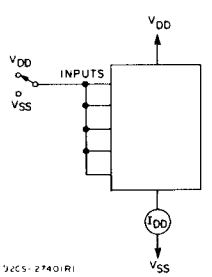


Fig. 11 – Quiescent-device-current test circuit.

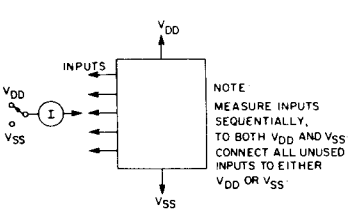


Fig. 12 – Input-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Q Output (See Fig. 10)	5	–	200	400	ns
	10	–	100	200	
	15	–	75	150	
Preset or Reset-to-Q Output	5	–	210	420	ns
	10	–	105	210	
	15	–	80	160	
Clock-to-Carry Out	5	–	240	480	ns
	10	–	120	240	
	15	–	90	180	
Carry-In-to-Carry Out	5	–	125	250	ns
	10	–	60	120	
	15	–	50	100	
Preset or Reset-to-Carry Out	5	–	320	640	ns
	10	–	160	320	
	15	–	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Input Capacitance (C_{IN})		–	5	7.5	pF
Set-up Time, t_S Preset Enable to J_n	5	25	12	—	ns
	10	10	6	—	
	15	10	5	—	
Hold times, t_H Clock to Carry-In	5	60	30	—	
	10	30	4	—	
	15	30	1	—	
Clock to Up/Down	5	30	10	—	
	10	30	4	—	
	15	30	5	—	
Preset Enable to J_n	5	70	35	—	
	10	40	20	—	
	15	40	20	—	

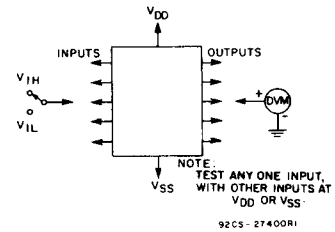
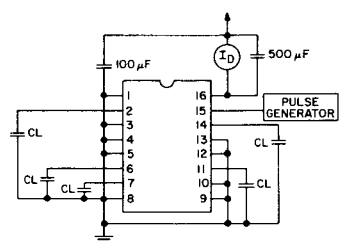


Fig. 13 – Input-voltage test circuit.



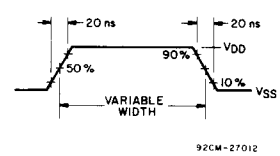


Fig. 14 – Power-dissipation test circuit and input waveform.

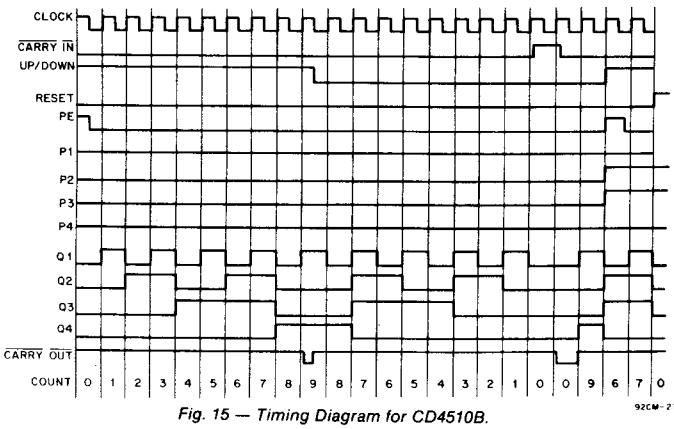


Fig. 15 — Timing Diagram for CD4510B.

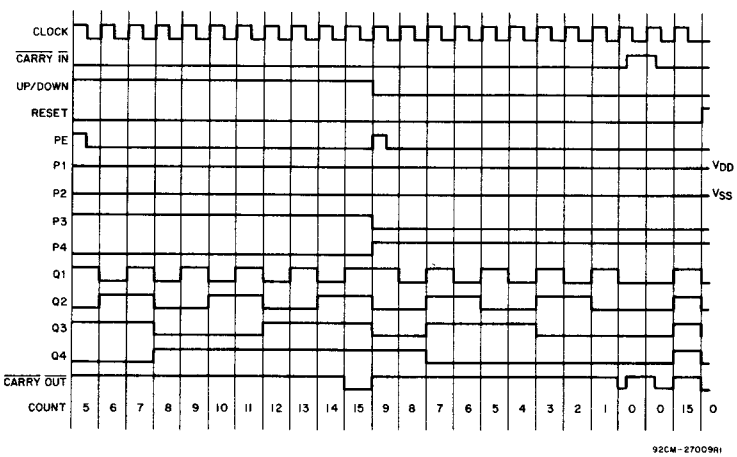
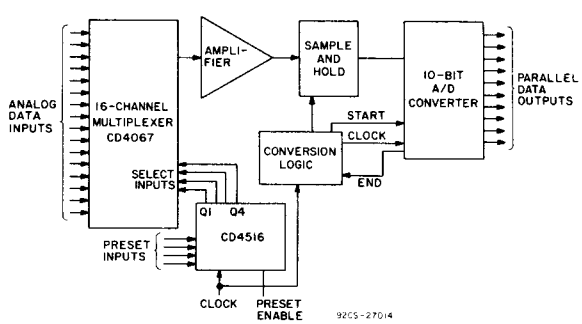


Fig. 16 — Timing diagram for CD4516B.



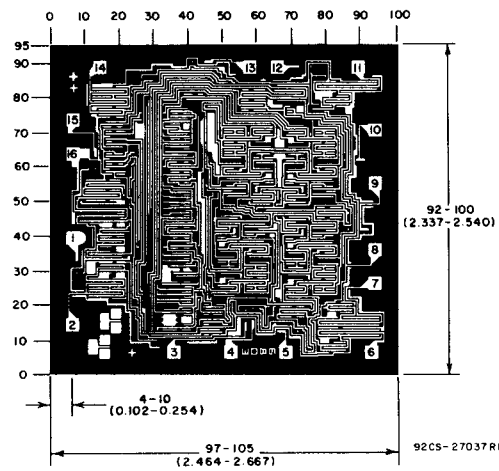
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516B.

Fig. 17 — Typical 16-channel, 10-bit data acquisition system.

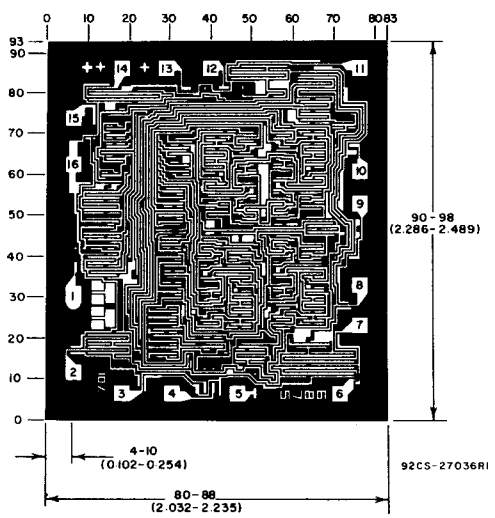
CL	$\overline{CI}$	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⌐	0	1	0	0	COUNT UP
⌐	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

TRUTH TABLE

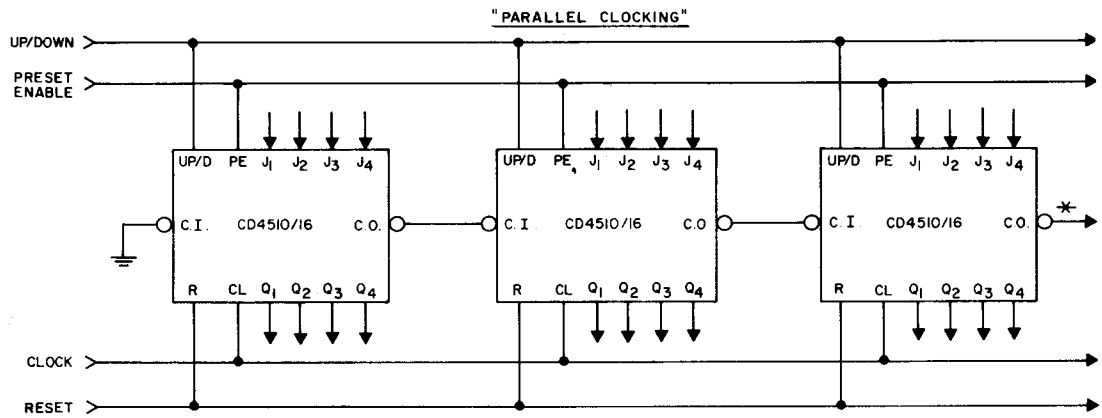


Dimensions and Pad Layout for CD4510BH.

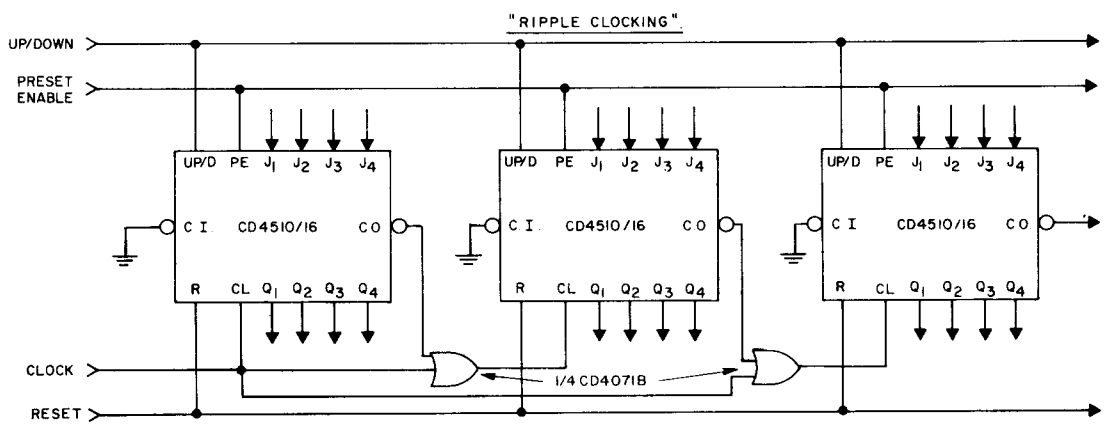


Dimensions and Pad Layout for CD4516BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



* **$\overline{\text{CARRY OUT}}$ lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4510/16 IC's. These negative-going glitches do not affect proper CD4510/16 operation. However, if the $\overline{\text{CARRY OUT}}$ signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the $\overline{\text{CARRY OUT}}$ signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.**



RIPPLE CLOCKING MODE:
THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE "HIGH".

For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and $\overline{\text{CO}}$ is connected directly to the CL input of the next stage with $\overline{\text{CI}}$ grounded.

92CL-17194R5

Fig. 18 — Cascading counter packages.