

Structure	Silicon Monolithic Integrated Circuit
Product Name	Dual, Low-Dropout Linear Regulators
Type	BD7003NUX
Functions	•2-channel 300mA, CMOS-type LDOs. •Pin-Programmable Output Voltage. (9 steps adjustable VO; See the Table of “Output-Voltage Programming”.) •LDOs Power ON/OFF Enable Control. •2.0mm × 2.0mm Package. •Small Ceramic Output Capacitors(1 μ F) •Equipped with Over Current Limiter and Thermal Shutdown Circuit(TSD) .

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage (VIN)	VIN	-0.3 ~ 7	V
Maximum Input Voltage 1 (P1,P2,EN1,EN2)	VINMAX1	-0.3 ~ 7	V
Maximum Input Voltage 2 (Vout1,Vout2)	VINMAX2	-0.3~Vin+0.3	V
Power Dissipation	Pd	1360	mW
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +150	°C

*This is the allowable loss of when it is mounted on a ROHM specification board 40mm × 40mm × 1.5mm
 To use at temperature higher than 25°C , derate 10.9mW per 1°C.

Operating range (Ta=-40°C ~ +85°C) (Do not exceed Pd)

Parameter	Symbol	Range	Unit
Input Power Supply Voltage Range	VIN	2.5~5.5	V

◎This product is not especially designed to be protected from radioactivity.

Electrical Characteristics

V_{IN}=3.7V, EN1=EN2=V_{IN}, T_a =+25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Voltage range	V _{OUT}	1.5	-	3.3	V	
Input Voltage range	V _{IN}	2.5	-	5.5	V	
Output Voltage Accuracy	Δ v _{out}	-1.8	-	1.8	%	I _{out} =1mA
Maximum Output Current	I _{max}	300	-	-	mA	
Short Circuit Current	I _{sc}	-	150	-	mA	V _{OUT} = 0V
Ground Pin Current	I _q	-	55	95	μ A	I _{out} =0mA
		-	35	65		One LDO shutdown, I _{out} =0mA
Dropout Voltage	V _{drop}	-	120	170	mV	V _{IN} =2.5V, V _{OUT} =2.6V, I _{out} =100mA
		-	90	140		V _{IN} =2.7V, V _{OUT} =2.8V, I _{out} =100mA
		-	70	120		V _{IN} =3.2V, V _{OUT} =3.3V, I _{out} =100mA
		-	360	510		V _{IN} =2.5V, V _{OUT} =2.6V, I _{out} =300mA
		-	270	420		V _{IN} =2.7V, V _{OUT} =2.8V, I _{out} =300mA
		-	210	360		V _{IN} =3.2V, V _{OUT} =3.3V, I _{out} =300mA
Line Regulation	Δ V _{LNR}	-	0.02	0.2	%/V	V _{IN} =V _{OUT} +1V to V _{IN} =5.5V, I _{out} =10mA
Load Regulation	Δ V _{LDR}	-	0.2	0.6	%	I _{out} =1mA to 300mA
Ripple Rejection	PSRR	-	66	-	dB	f=100Hz, I _{out} =10mA@V _{OUT} =1.5V
Output Noise	e _n	-	150	-	μ VRMS	fBW=10Hz to 100kHz; I _{out} =10mA
● EN1, EN2						
Enable Input Threshold	V _{iH}	1.2	-	-	V	Regulator enabled
	V _{iL}	-	-	0.5		Regulator shutdown
Enable Input Leakage Current	I _{en}	-	0.1	1	μ A	V _{en} =V _{IN} , T _a =+25°C
Shutdown Supply Current	I _{QSHDN}	-	0.1	1	μ A	V _{out} =0V , T _a =+25°C

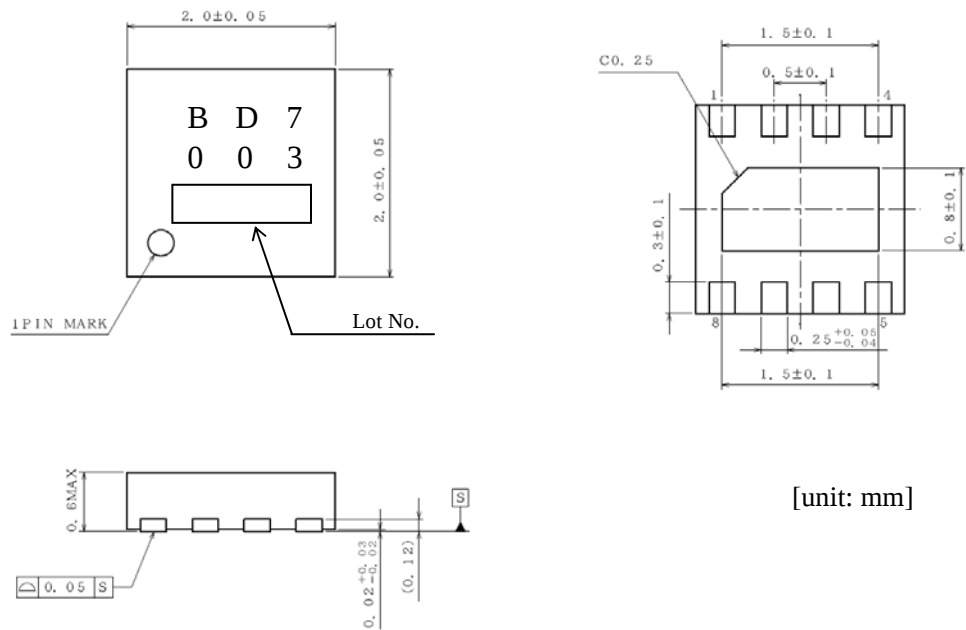
Output-Voltage Programming

PIN Name	P1	P2	V _{OUT1}	V _{OUT2}
Set up	OPEN	OPEN	1.50	2.80
	OPEN	GND	1.80	2.60
	OPEN	V _{IN}	1.80	2.70
	GND	OPEN	1.80	2.80
	GND	GND	1.80	2.90
	GND	V _{IN}	2.60	2.80
	V _{IN}	OPEN	2.80	2.80
	V _{IN}	GND	2.90	2.90
	V _{IN}	V _{IN}	2.80	3.30

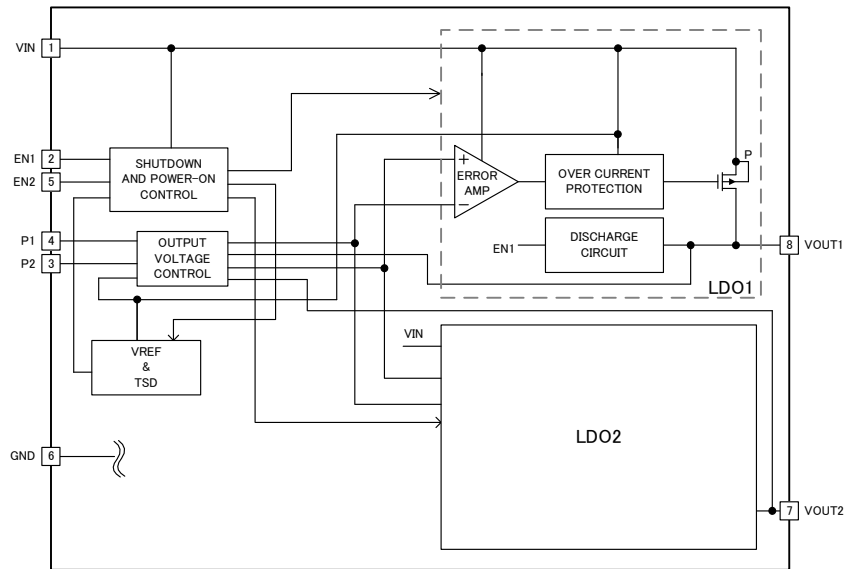
Output voltages, V_{OUT1} and V_{OUT2}, are determined at power up by the state of P1 and P2(see the table of “Output-Voltage Programming”).

Subsequent changes to P1 and P2 do not change the output voltages unless the supply power is cycled, or all EN inputs are simultaneously driven low to shutdown the device.

Package



Block Diagram



PIN description

PIN No.	PIN Name
1	VIN
2	EN1
3	P2
4	P1
5	EN2
6	GND
7	VOUT2
8	VOUT1

● Use-related Cautions

(1) Absolute maximum ratings

If applied voltage (VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins, between a pin and a power supply or GND.

(7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)

When the junction temperature reaches the defined value, the thermal shutdown circuit operates and turns the switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(14) Rush Current

Extra care must be taken on power coupling, power, ground line impedance, and PCB design while excess amount of rush current might instantly flow through the power line when powering-up a LSI which is equipped with several power supplies, depending on on/off sequence, and ramp delays.

Notes

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