

Evaluating the **AD8338** Low Power VGA

FEATURES

- Full-featured evaluation board for the **AD8338**
- On-board voltage regulator
- Low cost and easy-to-use header for control signals
- All analog design, no software needed
- Footprints provided for alternate configurations

EVALUATION KIT CONTENTS

- AD8338-EVALZ** evaluation board
- Evaluation board wire harness
- AD8338-EVALZ** User Guide (**UG-559**)

ADDITIONAL EQUIPMENT NEEDED

- A signal generator capable of producing differential outputs
- A single +3.5 V to +5.0 V supply for power
- A single, 0 V to +3 V programmable supply for gain control
- An oscilloscope with a 100 MHz minimum bandwidth
- 2 SMA (M) to BNC (M) cables
- 2 interface cables for the signal generator to the evaluation module

ONLINE RESOURCES

- AD8338** data sheet
- UG-559** user guide

GENERAL DESCRIPTION

This user guide describes the **AD8338** evaluation board and discusses common configurations. The design of this board (**AD8338-EVALZ**) emphasizes simplicity and ease of use, which is evident in the minimalist approach to connector implementation.

The **AD8338** data sheet, available at www.analog.com, covers the details of the device's operation. Using this data sheet for reference will help the designer in their end application. The data sheet is helpful for understanding the operation of the **AD8338** evaluation board, especially during the initial configuration and when powering up for the first time.

THE **AD8338-EVALZ** EVALUATION BOARD

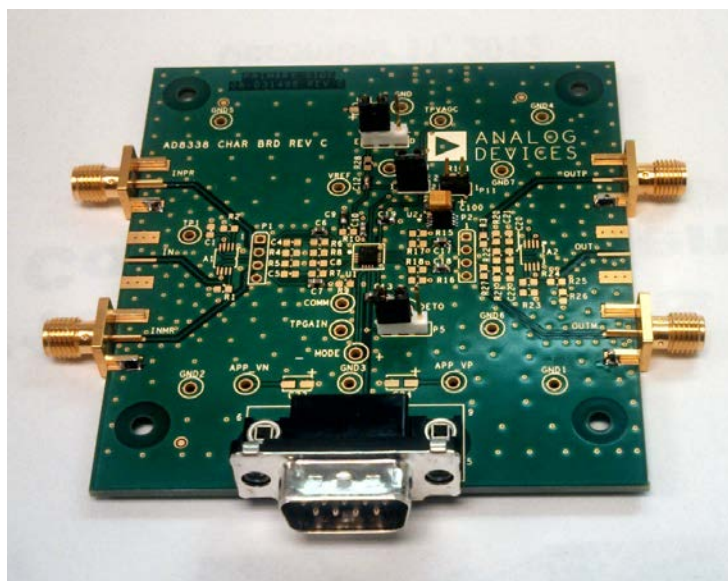


Figure 1. **AD8338** Evaluation Board

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REVISION HISTORY

8/13—Rev. 0 to Rev. A	
Changes to Power Supplies Section.....	5
Changes to Figure 6.....	6
5/13—Revision 0: Initial Version	

EVALUATION BOARD QUICK START PROCEDURES

INITIAL SETUP

The [AD8338](#) evaluation board needs only a few external connections. Setting up this board for the first time requires the following:

- Two dc supplies: one for board power, one for GAIN control
- The 9-pin D-SUB wire harness connector for connecting the control signals
- Cables to connect the board to the signal source
- Cables to connect the board to the oscilloscope

The addition of the wire harness allows the user, once comfortable with the evaluation board, to extend its value to a prototype platform in conjunction with other prototyping blocks. As the configuration changes, the harness is easily disconnected and reconnected.

INITIAL CONNECTIONS

Before any other signals are setup, connect the SMA to BNC cables from the output SMA connectors (OUTP, OUTM) to the oscilloscope. Set the oscilloscope to 1 M Ω input impedance.

If the output of the signal source can be disabled or turned off, disable the output and then connect the signal generator to the evaluation board. If the source cannot be disabled, power off the source and then connect the source to the evaluation board.

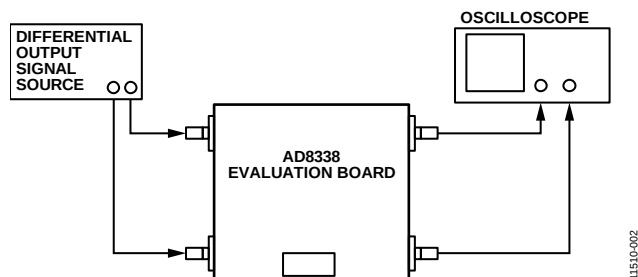


Figure 2. Basic Connections for the [AD8338](#) Evaluation Module

POWERING UP THE [AD8338](#)

Exercising caution in powering up the [AD8338](#) prevents possible failures. For instance, should power be applied to the GAIN pin (connector pin 2) before power is applied to VIN (connector pin 4), the user may exceed the electrical limits of the device. This may damage the part.

Before applying any signals or supplies, ensure that the jumpers are all set to their default settings (indicated on the PCB).

For the first-time power up, set the power supply to +5 V. For the gain control input (GAIN pin) set the output to +0.350 V, which will set the gain to +20 dB.

Enable or turn on the +5.0 V supply to VIN. Next, power up the control voltage for gain (GAIN) to +0.350 V.

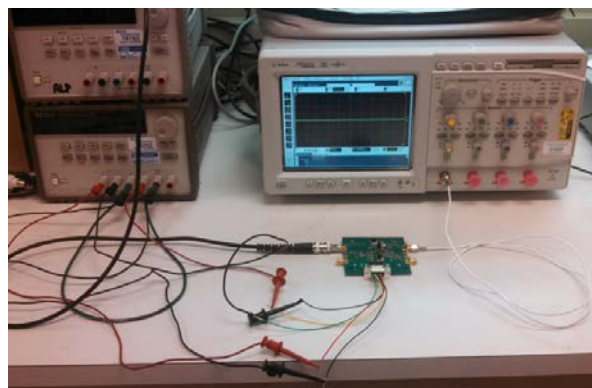


Figure 3. [AD8338](#) Setup for Single-Ended Measurements

If the signal source has an output enable function, leave the output disabled and set the differential signal source to output 20 mV p-p (± 10 mV at each input) at a frequency of 1 MHz. Choose a sine wave output. Then, enable the output. The oscilloscope should now display two signals of about ± 100 mV (200 mV p-p) amplitude.

If the signal source does not have an output enable function, power up the signal source, and proceed to configure the output for a differential output of 20 mV p-p (± 10 mV amplitude at each input). Set the frequency for 1 MHz, with an output shape of a sine wave. The oscilloscope should now show two sine-waves, each approximately ± 100 mV in amplitude (200 mV p-p differentially).

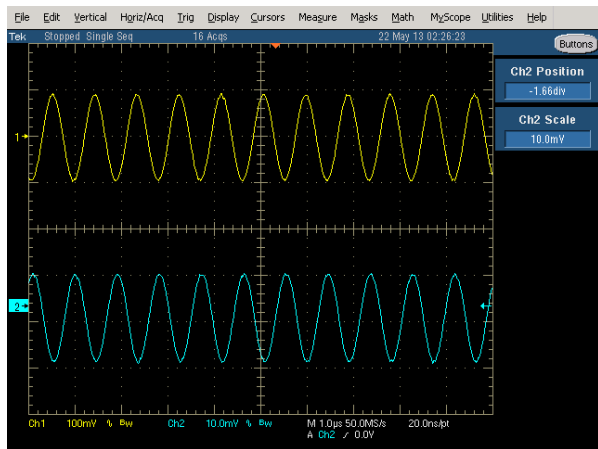


Figure 4. Start-Up Operation Verification

VERIFYING GAIN BEHAVIOR

With most oscilloscopes, setting the vertical resolution to 10 mV or lower rarely produces a signal that is distinguishable by casual observation. As such, increase the voltage on the GAIN pin to +0.525 V (+40 dB).

The oscilloscope should now display two signals at ± 0.5 V amplitude each (1 V p-p differentially). If successful, then the evaluation board is working properly and ready for the user's experimentation.

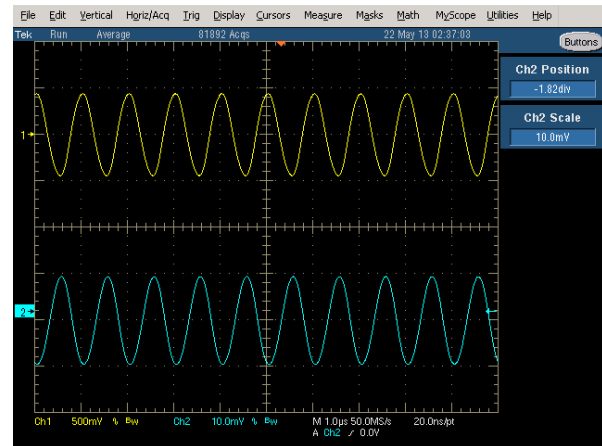


Figure 5. Gain Adjust Verification (+34 dB/GAIN = 0.525 V)

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The [AD8338](#) evaluation board includes the best in class (for noise), [ADP151](#) LDO for the [AD8338](#). This LDO supplies a very clean +3.0 V supply to the [AD8338](#), with a typical 9 μ V of rms noise at the output.

To drive the [ADP151](#), the user must supply power to the supply input. This supply should be no less than 3.5 V and no greater than 5.0 V.

Note that since the supply input to the evaluation board is not reverse bias protected, it is important to exercise care to prevent damage.

Additionally, the EN pin of the LDO must be pulled high to the supply level to enable the [AD8338](#).

INPUT CONTROLS

The [AD8338](#) has few input controls. These control inputs alter the fundamental behavior of the [AD8338](#) in one of two fundamental modes of operation: automatic gain control (AGC) mode, and direct-gain control mode.

AGC mode attempts to regulate the output magnitude to a target rms voltage. This mode requires some altered jumper settings (see Figure 9) and then the target rms voltage is set by applying a voltage on the VAGC pin. Direct gain control mode, gain can increase with increasing-voltage, or decreasing voltage, depending on the setting of the MODE pin and the voltage applied to the GAIN pin. This is the default mode of operation shown in Figure 7.

When the AGC mode is disabled, the MODE pin selects the direction of the gain slope, either positive or negative. While the AGC mode is disabled, the GAIN pin then directly controls the gain with an input ranging between 0.1 V to 1.1 V. The VAGC pin should be tied to VREF when the AGC circuit is not used.

When the AGC mode is enabled, the DETO pin is connected, by the user, to the GAIN pin (via a jumper). In this mode, the

user controls the rms output level through applying an input signal to VAGC. For the lowest gain, VAGC is tied to VREF, where the loop attempts to attenuate the output to 0 V rms. As the input to VAGC moves away from the 1.5 V of VREF (in either the positive or negative direction), the gain begins to increase.

One control input that is not pinned out to the connector is the offset nulling (OFSN) circuit. The application of the offset nulling feature applies a capacitor between OFNS and VREF, where the internal correction circuit passes signals of a higher frequency. This feature is set by a jumper.

INPUT SIGNALS

The signal inputs to the evaluation board start with SMA connectors designated by INPR and INMR. On the board, these signals are ac coupled through 0.1 μ F capacitors. After the coupling capacitors, input signals drive the resistor input terminals of the [AD8338](#).

The user does have the option of using the direct input terminals to the [AD8338](#). For user-selected values of input resistors, the INPR and INMR pins must be shorted together to prevent device instability. Refer to the data sheet for design considerations when using external resistors.

The [AD8338](#) does provide some dc operation with the inputs. When dc coupled, reference the input signals to the VREF signal. For the best operation in dc coupled mode, disable the offset nulling circuit.

OUTPUT SIGNALS

The [AD8338](#) outputs swing nearly rail to rail, centered about VREF. These outputs are ac coupled through 0.1 μ F capacitors, and should not be loaded with terminating values less than 500 Ω on each output. Below 500 Ω , the linearity of the outputs begins to degrade.

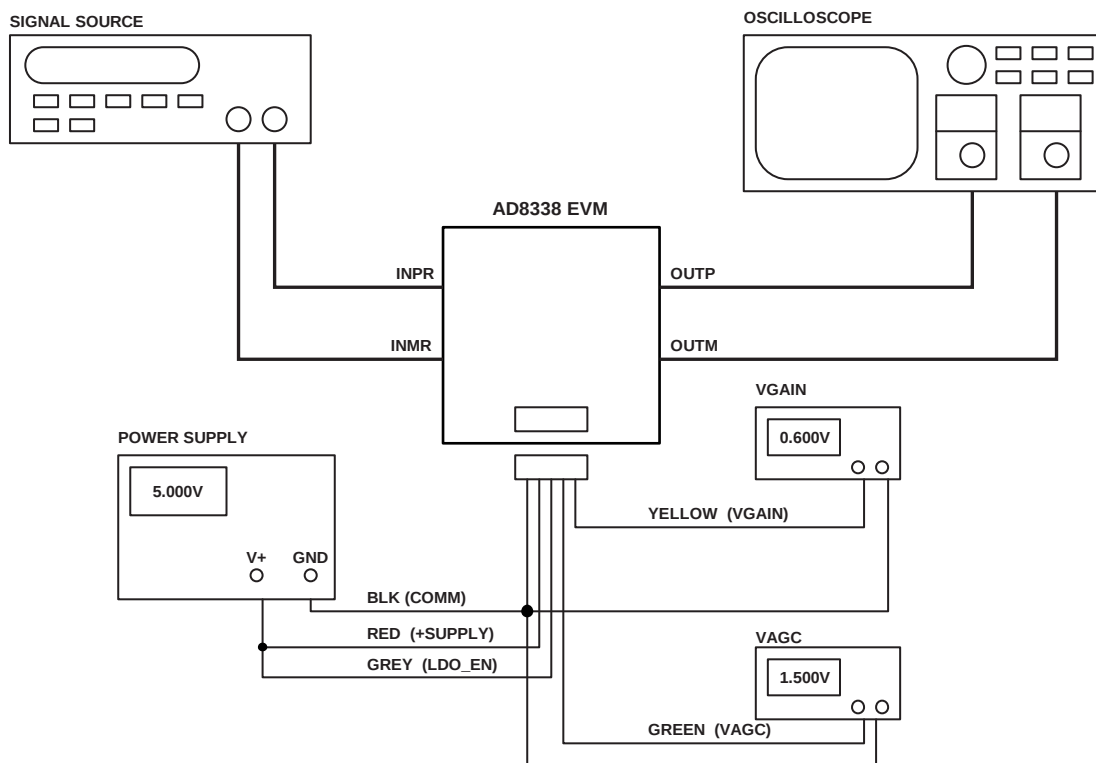


Figure 6. Evaluation Board Connection

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DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

Factory Default Configuration

The [AD8338](#) evaluation board ships with a default configuration shown in Figure 7. Offset nulling is enabled, MODE is set to high, and GAIN increases the system gain with an input from 0.1 V to 1.1 V.

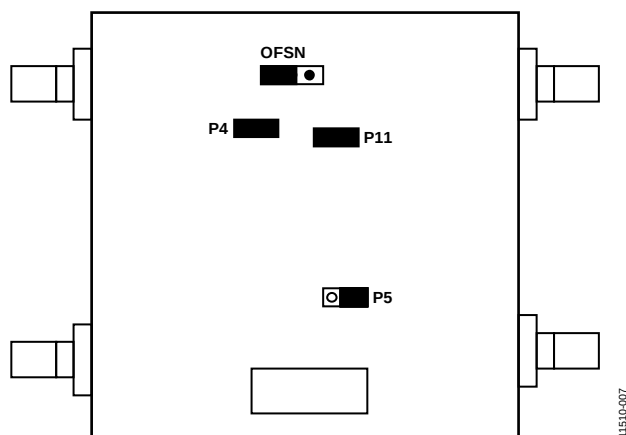


Figure 7. Standard Jumper Configuration

Configuration for Decreasing Gain with Increasing Voltage on GAIN Pin

Figure 8 shows the basic connections. MODE is set to low to achieve these results.

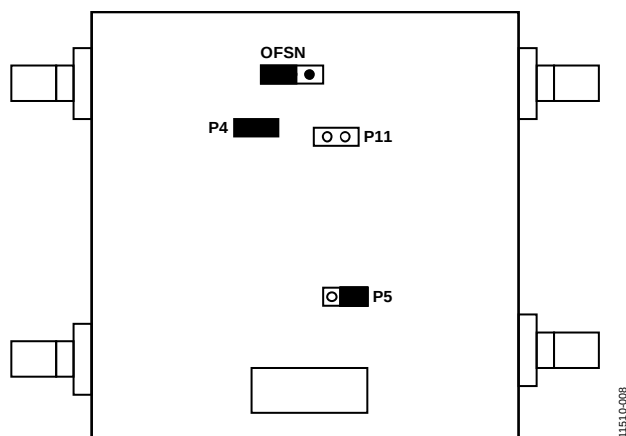


Figure 8. Jumper Configuration for MODE = Low

Configuration for Using AGC Loop

For the application of the AGC loop, set MODE on the [AD8338](#) to high. Set the DETO jumper (P5) as shown in Figure 9. Discontinue the use of the GAIN pin; no external signal should drive it. With the board configured as illustrated in Figure 9, the signal into VAGC sets the output rms level.

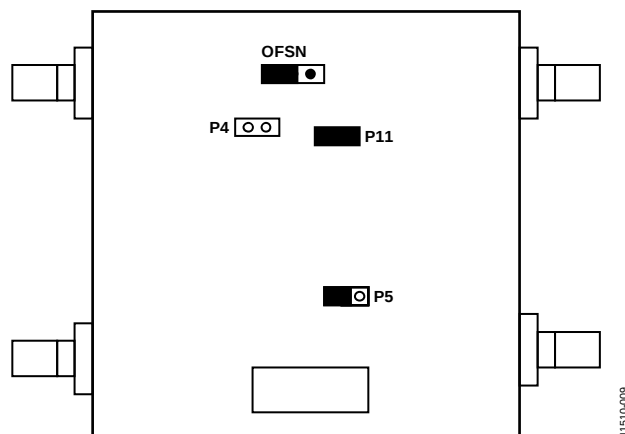


Figure 9. Jumper Settings for AGC Mode

ALTERNATE CONFIGURATIONS

The [AD8338](#) evaluation board supports two additional features, which are not populated from the factory as follows:

- A. A single-ended input to differential-output circuit via an [AD8131](#)
- B. A differential-in, single-ended output stage via an [AD8130](#)

For Configuration A, this feature eliminates the need for a differential output signal source. The tradeoff is then the need for an additional part, and higher system operating current. To implement this portion of the board, the user needs to install the [AD8131](#) amplifier to designator A1. They will then need to populate components R1 and R2. For correct operation, the user must provide an additional split supply. This supply is provided through the same wire harness as the other control signals. The positive supply must be tied to APP_V+, and the negative supply must be tied to APP_V–.

With Configuration B, this amplifier combines the two differential signals and produces a single output. As with Configuration A, a split supply is required. In addition, this configuration may be either dc or ac coupled. Configuring this for dc coupling requires 0 Ω shorts placed in designators C17 and C18.

To configure the [AD8130](#) for your specific application, refer to the [AD8130](#) data sheet. The [AD8338](#) evaluation board does provide footprints for the most common component configurations.

EVALUATION BOARD SCHEMATIC

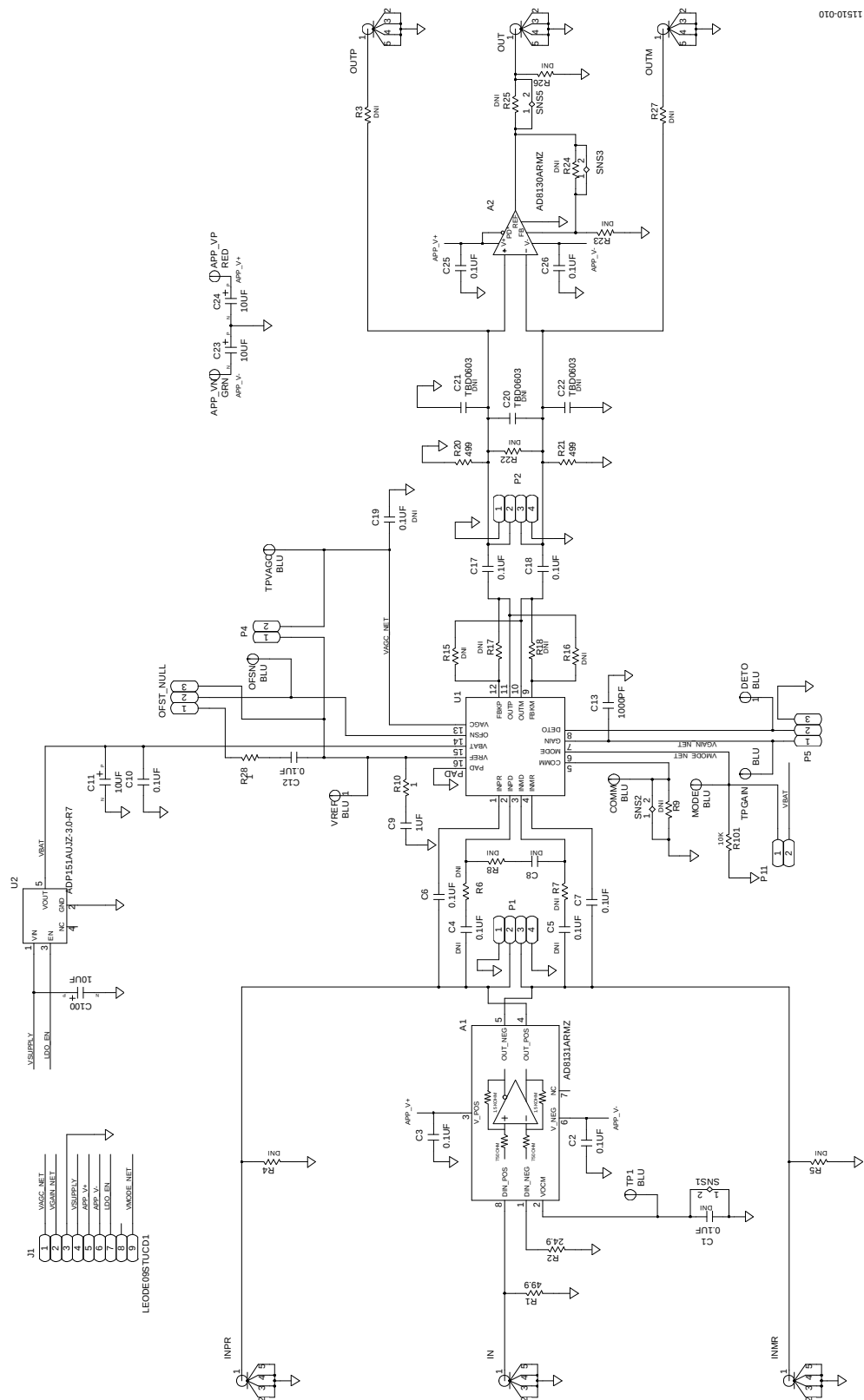


Figure 10. Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Item	Qty	Reference Designator	Description	Manufacturer	Part Number
1	7	C6, C7, C10, C12, C17, C18, C19	Capacitor, 0.1 μ F, 0603, ceramic, X5R, 25 V	TDK Corporation	C1608X7R1E104M080AA
2	1	C13	Capacitor 0.01 μ F, 0603, ceramic, X7R, 50 V	TDK Corporation	C1608X7R1H103K080AA
3	2	C11, C100	Capacitor 10 μ F, 1206, ceramic, X7R, 16 V	TDK Corporation	C3216Y5V1A106Z/1.15
4	1	C9	Capacitor 1 μ F, 0603, ceramic, X7R, 10 V	TDK Corporation	C1608X5R1A105K080AC
5	1	R011	Resistor, 10 k, 0603, 1%	Vishay	CRCW060310K0JNEA
6	2	R10, R28	Resistor 1 Ω , 0603, 1%	Panasonic	ERJ-3GEYJ1R0V
7	1	U1	0 dB to 80 dB gain, low power VGA	Analog Devices	AD8338ACPZ
8	1	U10	Ultra-low noise LDO	Analog Devices	ADP151AUJZ-3.0-R7
9	4	INPR, INMR, OUTP, OUTM	End launch SMA connector	Emerson	142-0701-801
10	1	J1	D-sub miniature, 9-position, right-angle connector	TE Connectivity	1734351-1
11	2	P4, P11	2-pin male headers	TE Connectivity	5-146285-2
12	2	OFST_NULL, P5	3-pin male headers	TE Connectivity	5-146280-3

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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