TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC166P,TC74AC166F,TC74AC166FN

8-Bit Shift Register (P-IN, S-OUT)

The TC74AC166 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/ $\overline{\text{LOAD}}$ input. When the SHIFT/ $\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

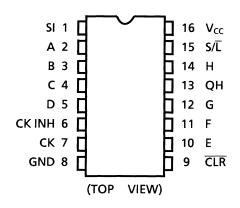
Features

- High speed: $f_{max} = 170 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $ICC = 8 \mu A \text{ (max)}$ at $Ta = 25^{\circ}C$
- High noise immunity: VNIH = VNIL = 28% VCC (min)
- Symmetrical output impedance: |IOH| = IOL = 24 mA (min) Capability of driving 50 Ω

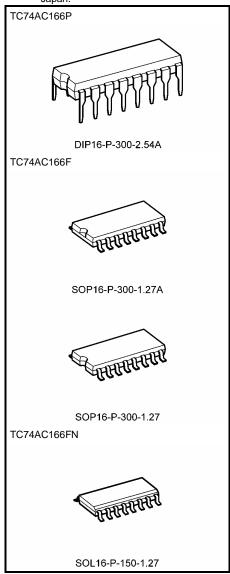
transmission lines.

- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 5.5 V
- Pin and function compatible with 74HC166

Pin Assignment



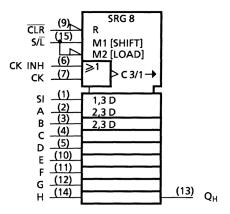
Note: xxxFN (JEDEC SOP) is not available in



Weight
DIP16-P-300-2.54A : 1.00 g (typ.)
SOP16-P-300-1.27A : 0.18 g (typ.)
SOP16-P-300-1.27 : 0.18 g (typ.)
SOL16-P-150-1.27 : 0.13 g (typ.)

1 2006-02-01

IEC Logic Symbol



Truth Table

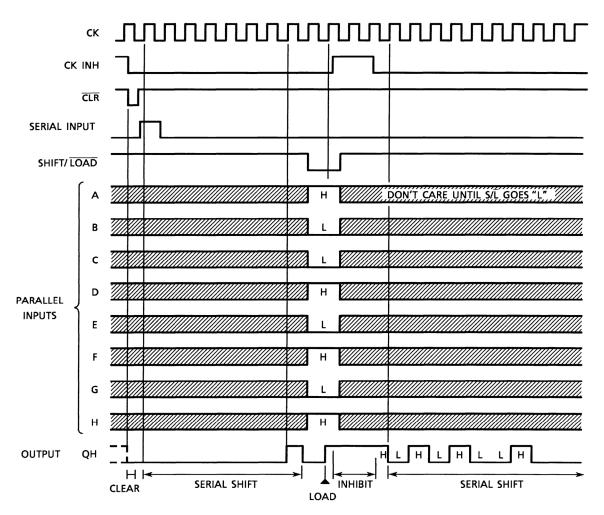
Inputs							Output
CLR	SHIFT/ LOAD	CK INH.	CK	SERIAL IN	PARALLEL A······H	QA QB	QH
L	Х	Х	Х	Х	Х	L L	L
Н	Х	Х	\rightarrow	Х	Х	No Cl	nange
Н	L	L		Х	a·····h	a b	h
Н	Н	L		Н	Х	H QAn	QGn
Н	Н	L		L	Х	L QAn	QGn
Н	Х	Н	Х	Х	Х	No Cl	nange

X: Don't care

a $\cdot \cdot \cdot \cdot$ h: The level of steady state input voltage at inputs A through H respectively

2

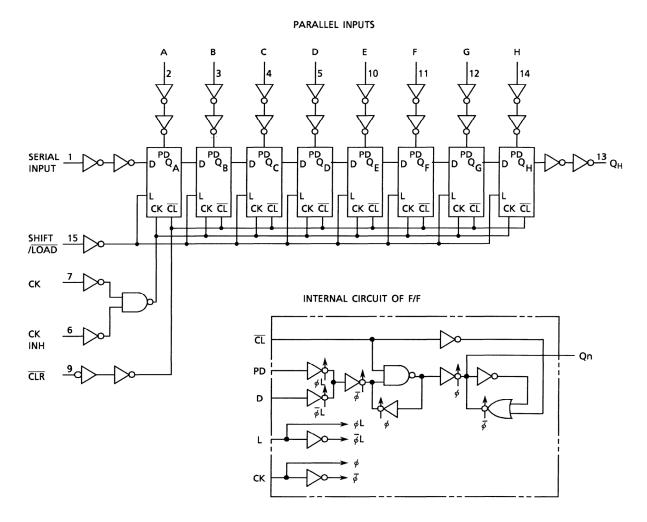
Timing Chart



3 2006-02-01



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	Vcc	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±50	mA
DC output current	l _{OUT}	±50	mA
DC V _{CC} /ground current	Icc	±100	mA
Power dissipation	P _D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T _{stg}	−65 to 150	°C

Note1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

4



Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 5.5	V
Input voltage	V _{IN}	0 to V _{CC}	٧
Output voltage	V _{OUT}	0 to V _{CC}	٧
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3 \text{ V}$) 0 to 20 ($V_{CC} = 5 \pm 0.5 \text{ V}$)	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
Characteristics	Symbol				V _C C (V)	Min	Тур.	Max	Min	Max	Offic
					2.0	1.50	_	_	1.50	_	
High-level input voltage	V_{IH}		_		3.0	2.10	_	_	2.10	_	V
ŭ					5.5	3.85		_	3.85	_	
					2.0	_	_	0.50	_	0.50	
Low-level input voltage	V _{IL}		_		3.0	_	_	0.90	_	0.90	V
					5.5	_	_	1.65	_	1.65	
						1.9	2.0	_	1.9	_	
	Voн	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -50 \ \mu A$		3.0	2.9	3.0	_	2.9	_	V
High-level output					4.5	4.4	4.5	_	4.4	_	
voltage			$I_{OH} = -4 \text{ mA}$		3.0	2.58	_	_	2.48	_	
			$I_{OH} = -24 \text{ mA}$		4.5	3.94	_	_	3.80	_	
			$I_{OH} = -75 \text{ mA}$	(Note)	5.5	_	_	_	3.85	_	
	VoL	VIN = V _{IH} or VIL			2.0	_	0.0	0.1	_	0.1	
			$I_{OL} = 50 \mu A$		3.0	_	0.0	0.1	_	0.1	
Low-level output					4.5	_	0.0	0.1	_	0.1	V
voltage			I _{OL} = 12 mA		3.0	_	_	0.36	_	0.44	
			I _{OL} = 24 mA		4.5	_	_	0.36	_	0.44	
			$I_{OL} = 75 \text{ mA}$	(Note)	5.5	_	_	_	_	1.65	
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		5.5	_	_	±0.1	_	±1.0	μΑ	
Quiescent supply current	I _{CC}	$V_{IN} = V_{C}$	_C or GND		5.5	_	_	8.0	l	80.0	μА

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.



Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C	Ta = -40 to 85°C	Unit	
			V _{CC} (V)	Limit	Limit	
Minimum pulse width	t _{W (H)}		3.3 ± 0.3	7.0	7.0	20
(CK)	t _{W (L)}	_	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width	4		3.3 ± 0.3	8.0	8.0	20
(CLR)	t _{W (L)}	_	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time			3.3 ± 0.3	8.0	8.0	
(SI, PI)	t _S	_	5.0 ± 0.5	4.0	4.0	ns
Minimum set-up time			3.3 ± 0.3	7.0	7.0	
(S/L)	t _S	_	5.0 ± 0.5	4.0	4.0	ns
Minimum hold time			3.3 ± 0.3	0.5	0.5	
(SI, PI)	t _h	_	5.0 ± 0.5	0.5	0.5	ns
Minimum hold time			3.3 ± 0.3	1.0	1.0	
(S/L)	t _h	_	5.0 ± 0.5	1.0	1.0	ns
Minimum removal time			3.3 ± 0.3	4.0	4.0	
(CLR)	t _{rem}	_	5.0 ± 0.5	1.5	1.5	ns

AC Characteristics (C_L = 50 pF, R_L = 500 Ω , input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
	-,		V _{CC} (V)	Min	Тур.	Max	Min	Max	
Propagation delay time (CK-QH)	t _{pLH}	_	3.3 ± 0.3 5.0 ± 0.5	_	9.4 6.6	16.1 10.0	1.0 1.0	18.3 11.4	ns
Propagation delay time (CLR -QH)	t _{pHL}	_	3.3 ± 0.3 5.0 ± 0.5	_	9.2 6.4	15.2 9.6	1.0 1.0	17.4 10.9	ns
Maximum clock frequency	f _{max}	_	3.3 ± 0.3 5.0 ± 0.5	55 90	105 150	_ _	55 90	_	MHz
Input capacitance	C _{IN}	_		_	5	10	_	10	pF
Power dissipation capacitance	C _{PD} (Note)	_		_	67	_	_	_	pF

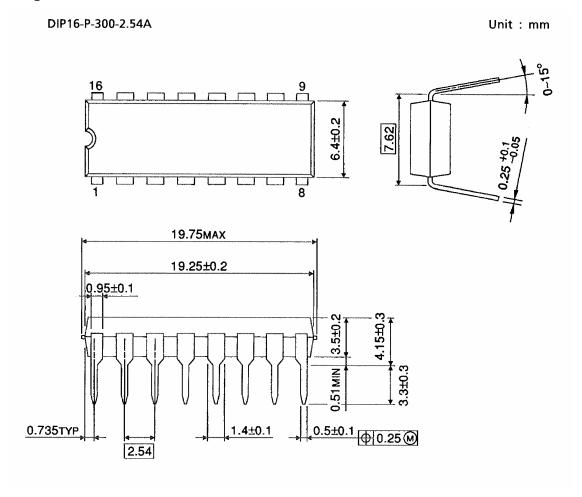
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} \ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$



Package Dimensions



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm 5.3 ± 0.2 7.8 ± 0.3 8 F 1.27 0.705TYP 10.8MAX $0.15^{+0.075}_{-0.035}$ 10.3 ± 0.2 0.25 0.8 ± 0.2 1.5±0.2

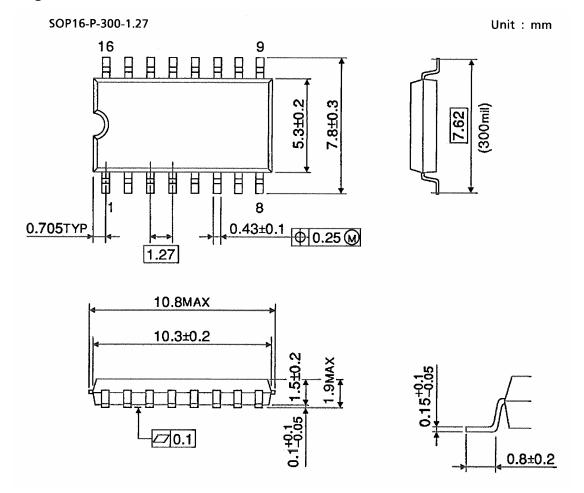
1.9MAX

Weight: 0.18 g (typ.)

□ 0.1



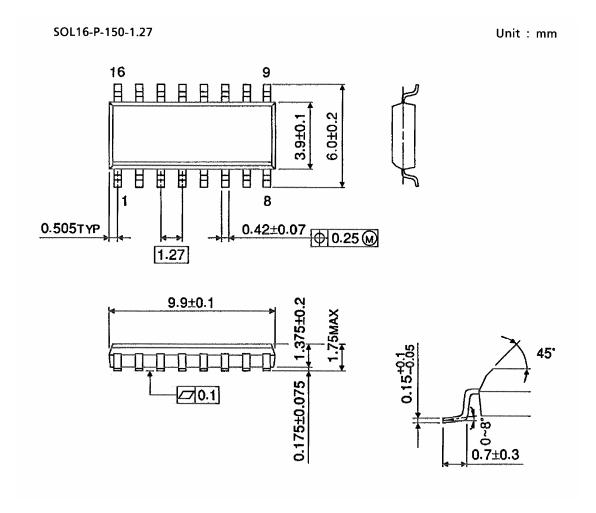
Package Dimensions



Weight: 0.18 g (typ.)



Package Dimensions (Note)



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Note: Lead (Pb)-Free Packages

DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27

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