

N-Channel Power MOSFET

600V, 4.0A, 2.5Ω

FEATURES

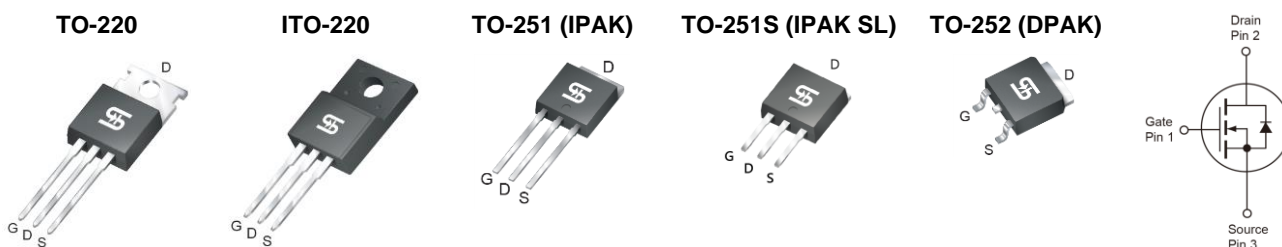
- 100% Avalanche Tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	2.5	Ω
Q_g	14.5	nC

APPLICATION

- Power Supply
- Lighting



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	TO-220	UNIT
Drain-Source Voltage	V_{DS}	600			V
Gate-Source Voltage	V_{GS}	±30			V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$			A
		$T_C = 100^\circ\text{C}$			
Pulsed Drain Current ^(Note 2)	I_{DM}	16			A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	50	25	70	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	70			mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	4			A
Repetitive Avalanche Energy ^(Note 2)	E_{AR}	5			mJ
Peak Diode Recovery ^(Note 4)	dV/dt	4.5			V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150			°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	TO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	5	1.78	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	83	62.5	62.5	°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 5)						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2.5	3.5	4.5	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 2.0\text{A}$	$R_{DS(on)}$	--	2.2	2.5	Ω
Forward Transfer Conductance	$V_{DS} = 40\text{V}, I_D = 2\text{A}$	g_{fs}	--	2.6	--	S
Dynamic (Note 6)						
Total Gate Charge	$V_{DS} = 480\text{V}, I_D = 4.0\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	14.5	--	nC
Gate-Source Charge		Q_{gs}	--	3.4	--	
Gate-Drain Charge		Q_{gd}	--	7	--	
Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	500	--	pF
Output Capacitance		C_{oss}	--	53.2	--	
Reverse Transfer Capacitance		C_{rss}	--	7	--	
Switching (Note 7)						
Turn-On Delay Time	$V_{DD} = 300\text{V},$ $R_{GEN} = 25\Omega,$ $I_D = 4.0\text{A}, V_{GS} = 10\text{V},$	$t_{d(on)}$	--	11	--	ns
Turn-On Rise Time		t_r	--	20	--	
Turn-Off Delay Time		$t_{d(off)}$	--	30	--	
Turn-Off Fall Time		t_f	--	19	--	
Source-Drain Diode (Note 5)						
Forward On Voltage	$I_S = 4.0\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.13	V
Reverse Recovery Time	$V_{GS} = 0\text{V}, I_S = 2\text{A}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	522	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.6	--	μC
Source Current	Integral reverse diode in the MOSFET	I_S	--	--	4	A
Source Current (Pulse)		I_{SM}	--	--	16	A

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 8\text{mH}, I_{AS} = 4.0\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
100% Eas Test Condition: $L = 8\text{mH}, I_{AS} = 2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 4\text{A}, dI/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

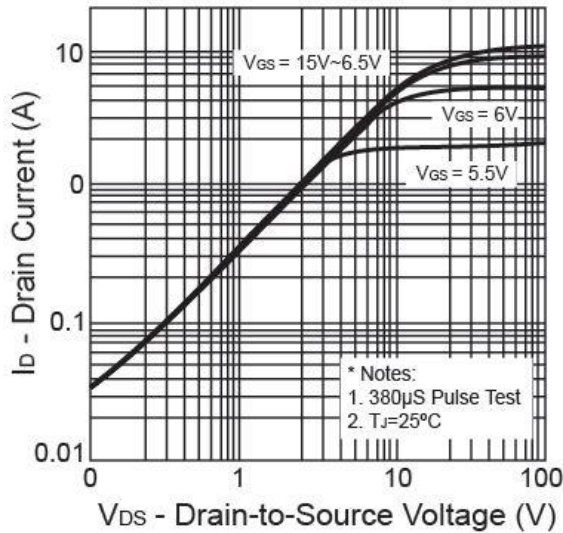
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM4NB60CZ C0G	TO-220	50pcs / Tube
TSM4NB60CI C0G	ITO-220	50pcs / Tube
TSM4NB60CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM4NB60CH X0G	TO-251S (IPAK SL)	75pcs / Tube
TSM4NB60CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

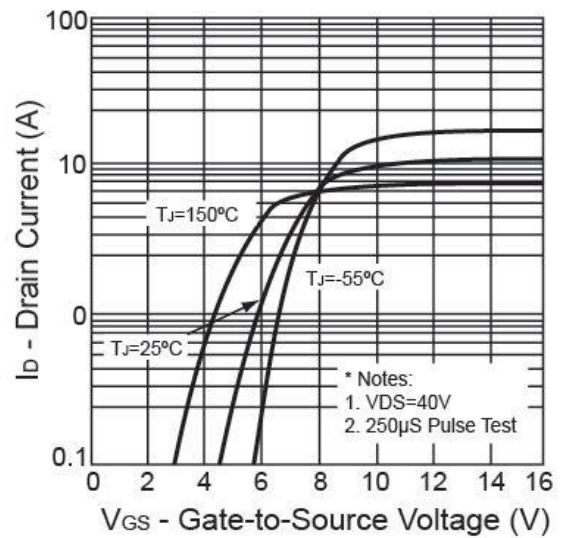
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

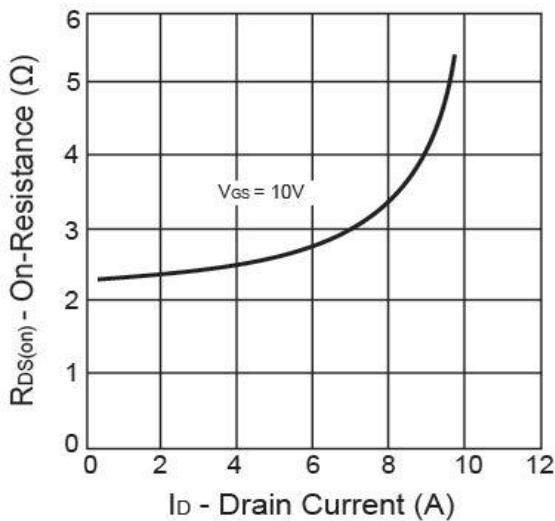
Output Characteristics



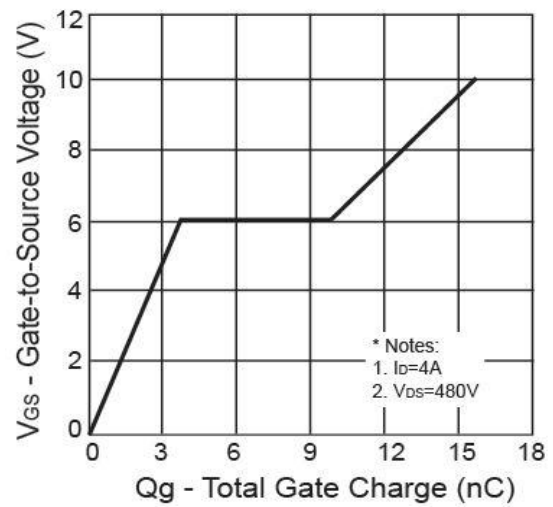
Transfer Characteristics



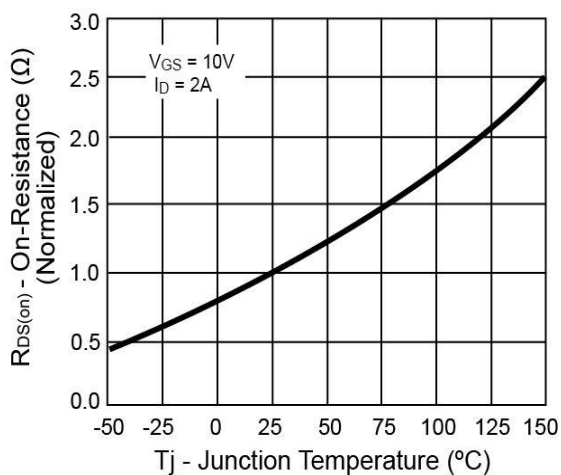
On-Resistance vs. Drain Current



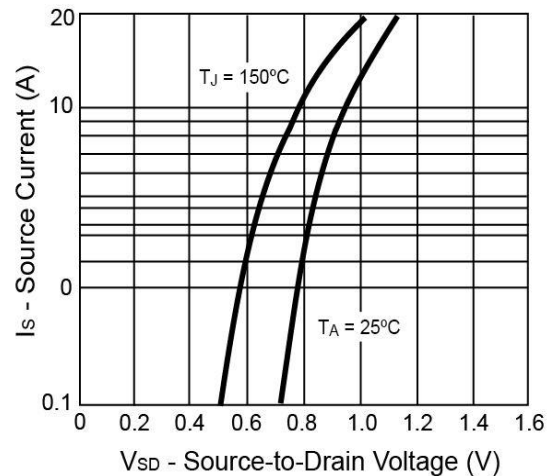
Gate Charge



On-Resistance vs. Junction Temperature



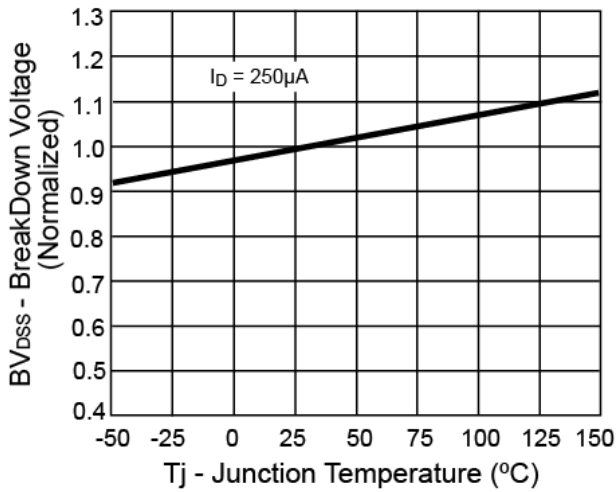
Source-Drain Diode Forward Voltage



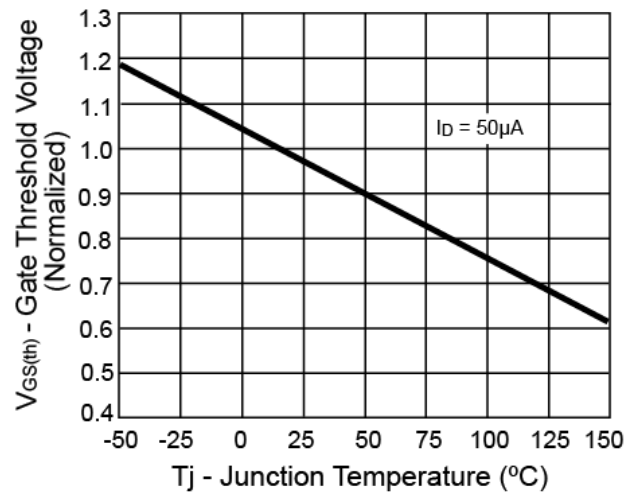
CHARACTERISTICS CURVES

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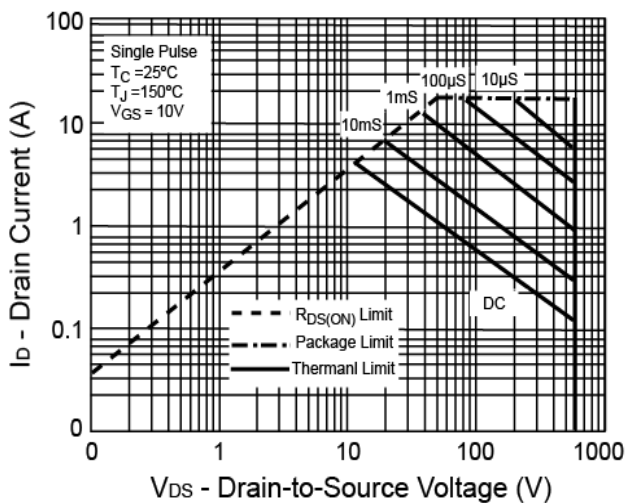
Breakdown Voltage vs. Temperature



Threshold Voltage vs. Temperature



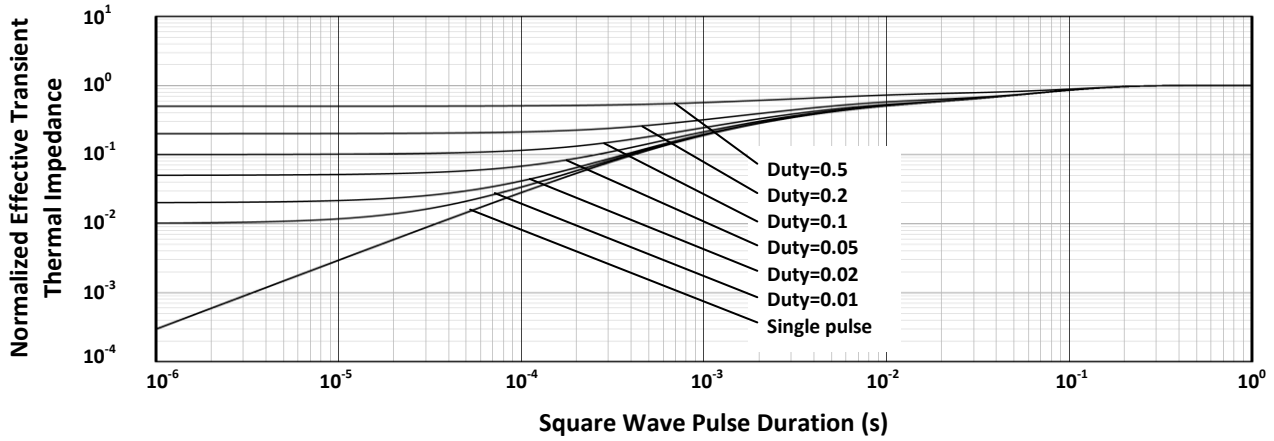
Maximum Safe Operating Area



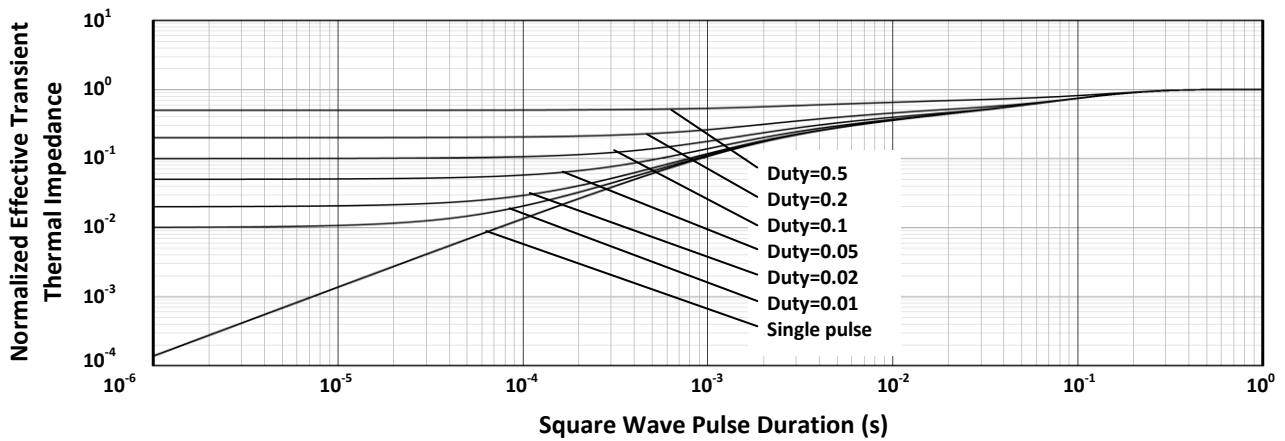
ELECTRICAL CHARACTERISTICS CURVES

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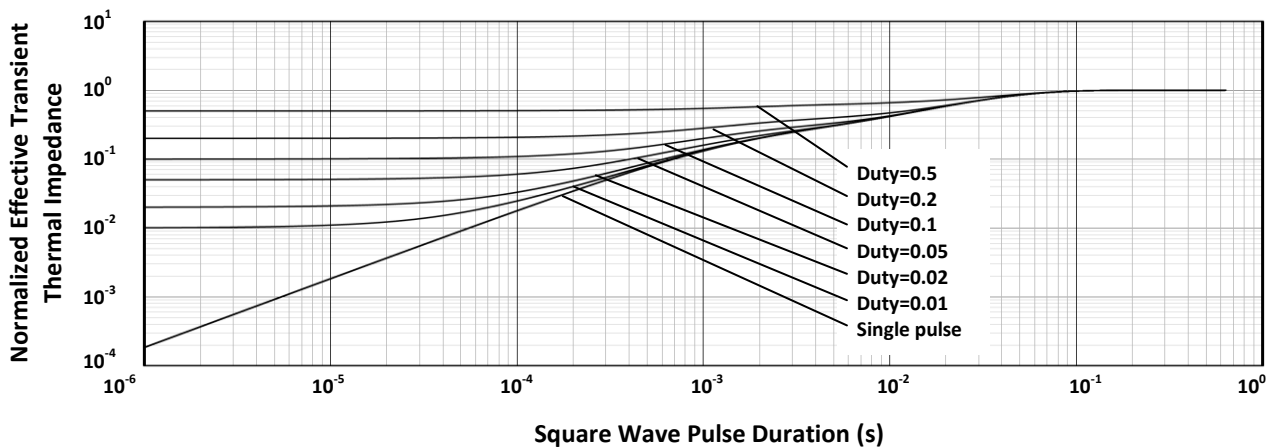
Normalized Thermal Transient Impedance, Junction-to-Case (TO-220)



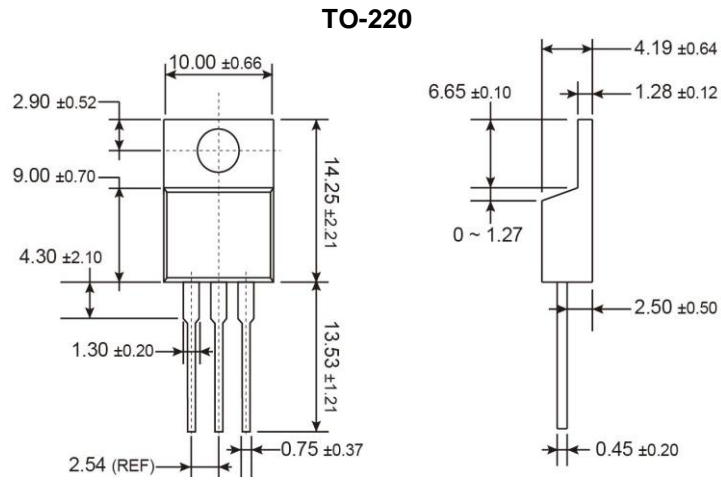
Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)



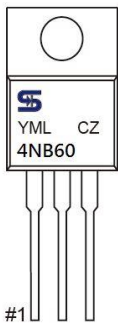
Normalized Thermal Transient Impedance, Junction-to-Case (DPAK/IPAK)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

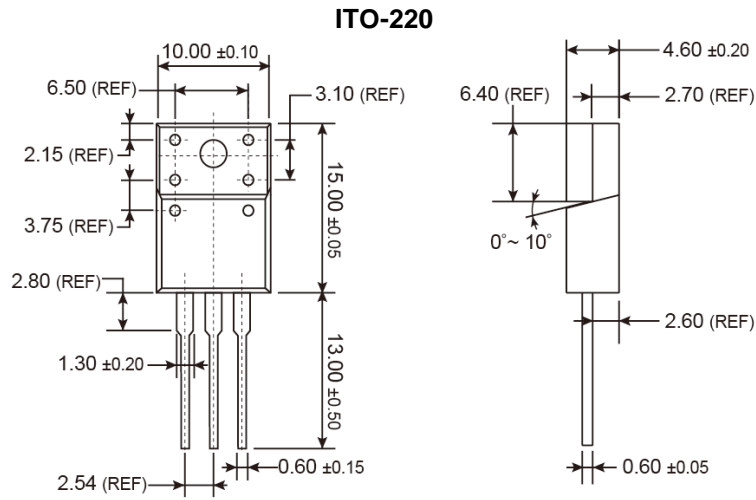


MARKING DIAGRAM

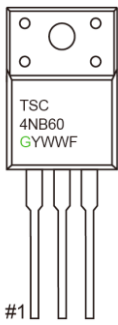


- Y** = Year Code
- M** = Month Code for Halogen Free Product
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



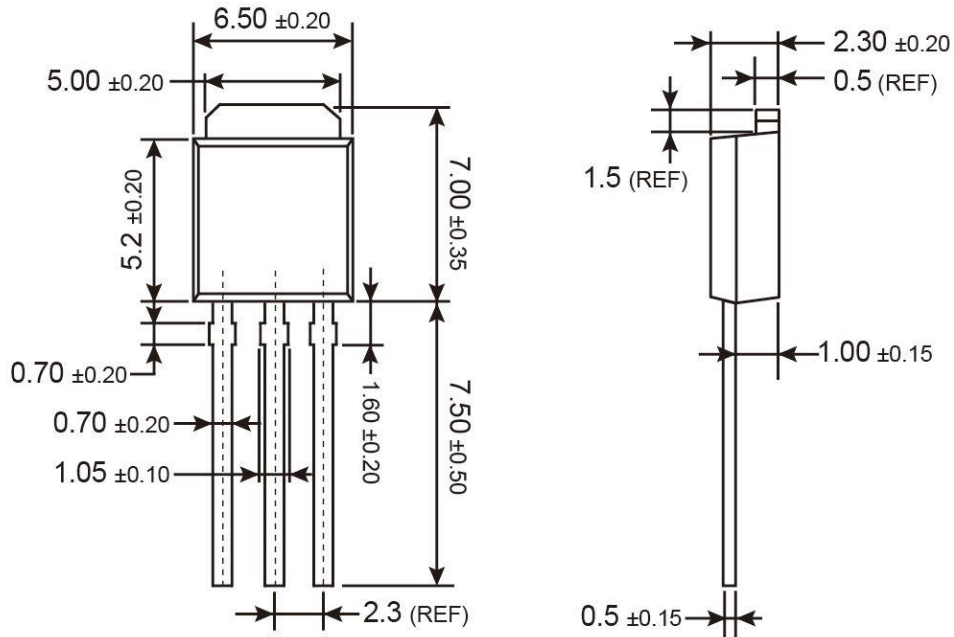
MARKING DIAGRAM



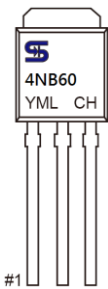
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251

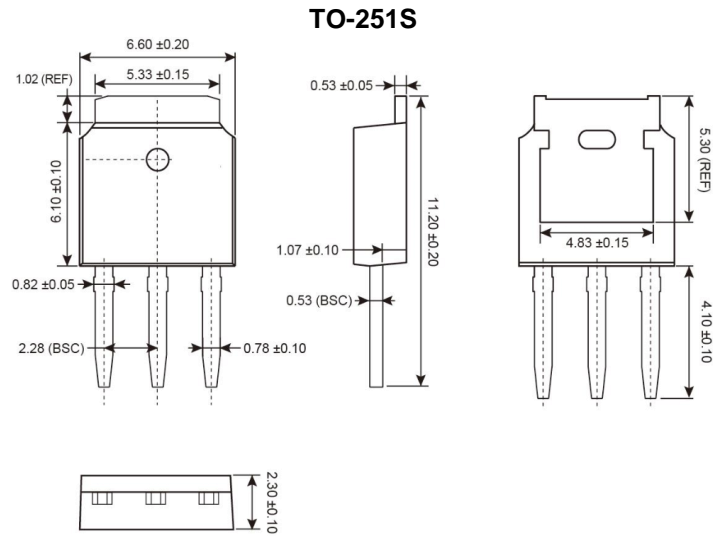


MARKING DIAGRAM

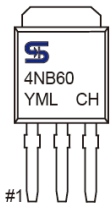


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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



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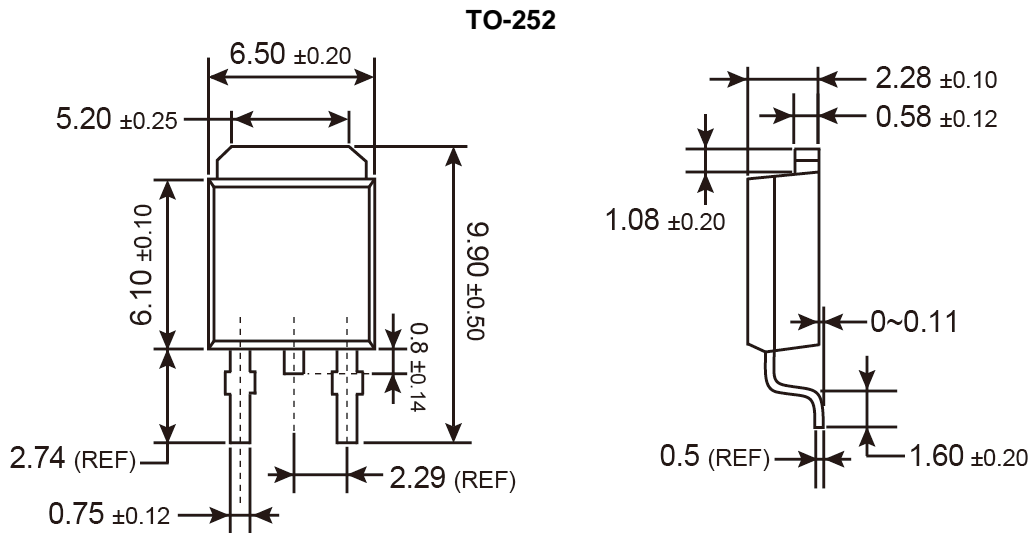
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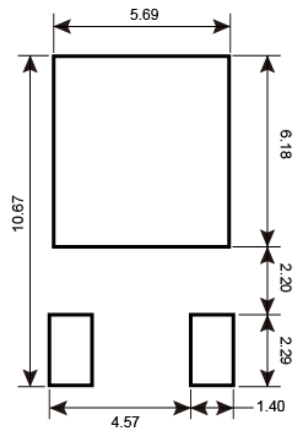
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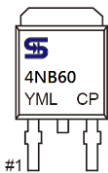
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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