

DSA63XX

Ultra-Small, Ultra-Low Power MEMS Oscillator with Spread Spectrum for Automotive

Features

- Automotive AEC-Q100 Qualified
- Output Frequency: 1 MHz to 100 MHz LVCMOS
- · Spread Spectrum Options:
 - Center-Spread: ±0.25%, ±0.5%, ±1.0%, ±1.5%, ±2.0%, ±2.5%
 - Down-Spread: -0.25%, -0.5%, -1.0%, -1.5%, -2.0%, -3.0%
- Ultra-Low Power Consumption: 3 mA (Active), 1µA (Standby)
- · Ultra-Small Package Sizes:
 - 1.6 mm x 1.2 mm VFLGA
 - 2.0 mm x 1.6 mm VFLGA
 - 2.5 mm x 2.0 mm VLGA
 - 3.2 mm x 2.5 mm VDFN
 - 5.0 mm x 3.2 mm VDFN
 - 7.0 mm x 5.0 mm VDFN
- · Excellent Shock and Vibration Immunity
 - Qualified to MIL-STD-883
- · High Reliability
 - 20x Better MTF Than Quartz Oscillators
- · Lead Free and RoHS Compliant

Applications

- · Automotive Infotainment
- Automotive ADAS
- · Automotive Camera Module

Benefits

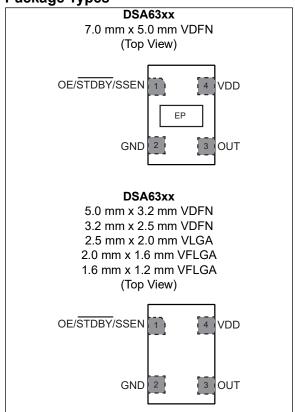
 Replace High-Temperature Crystals and Quartz Oscillators

General Description

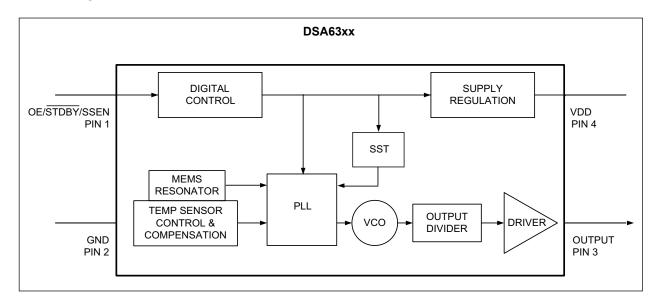
The DSA63xx series of clock generators uses a proven silicon MEMS technology to provide excellent frequency stability over a wide range of temperatures as well as small size. Available in three different package sizes with operating current as low as 3 mA, the smallest 4-pin package is a mere 1.6 mm x 1.2 mm in size. The devices support up to ±2.5% or -3% spread spectrum that can achieve up to 15 dB electromagnetic interference (EMI) reduction. Because of industry standard package and pin options, customers can solve last minute EMI problems simply by placing the new DSA63xx on their current board layout with no redesign required.

The DSA63xx family is available in 1.6 mm x 1.2 mm & 2.0 mm x 1.6 mm VFLGA, 7.0 mm x 5.0 mm, 5.0 mm x 3.2 mm & 3.2 mm x 2.5 mm VDFN, and 2.5 mm x 2.0 mm VLGA packages. These packages are "drop-in" replacements for standard 4-pin CMOS quartz crystal oscillators.

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage	
nput Voltage (V _{IN})	
ESD Protection	4 kV HBM, 400V MM, 2 kV CDM

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = 1.8V - 5\%$ to $3.3V + 10\%$, $T_A = -40$ °C to $+125$ °C.							
Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions	
Supply Voltage	V_{DD}	1.71		3.63	V	Note 1	
Power Supply Ramp	t _{PU}	0.1	1	100	ms	_	
Active Supply Current	I _{DD}	_	3.0	_	mA	f_{OUT} = 27 MHz, V_{DD} = 1.8V, No Load	
Ctondby Cymaly Cymant	la-ny.	_	1	_		V _{DD} = 1.8/2.5V Note 2	
Standby Supply Current	I _{STBY}	_	1.5	1	μA	V _{DD} = 3.3V Note 2	
Output Duty Cycle	SYM	45	1	55	%	_	
Frequency	f_0	1	_	100	MHz	_	
Frequency Stability	Δf	_	_	±20 ±25 ±50	ppm	All temp ranges, Note 3, Spread Spectrum is off.	
		_	_	±5		1st year @25°C	
Aging	Δf	_	_	±1	ppm	Per year after first year	
Startup Time	t _{SU}	_	ı	1.5	ms	From 90% V _{DD} to valid clock output, T = 25°C	
lanuat Lania Laurala	V_{IH}	0.7 x V _{DD}	_	_	V	Input Logic High, Note 4	
Input Logic Levels	V_{IL}	_	1	0.3 x V _{DD}	V	Input Logic Low, Note 4	
Output Disable Time	t _{DA}	_		200 + 2 Periods	ns	Note 5	
Output Enable Time	t _{EN}	_	_	1	μs	Note 6	
OE/STDBY/SSEN Pull-Up Resistor	_	_	300	_	kΩ	If configured, Note 7	

- Note 1: Pin 4 V_{DD} should be filtered with 0.1 μF capacitor.
 - 2: Not including current through pull-up resistor on EN pin (if configured).
 - 3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
 - 4: Input waveform must be monotonic with rise/fall time < 10 ms
 - **5:** Output Disable time takes up to two periods of the output waveform + 200 ns.
 - 6: For parts configured with OE, not Standby.
 - **7:** Output is enabled if pad is floated or not connected.
 - 8: Time to reach 90% of target V_{DD} . Power ramp rise must be monotonic.

DSA63XX

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V _{DD} = 1.8V –5% to 3.3V +10%, T _A = –40°C to +125°C.								
Parameters	Sym.	Min.	Тур.	Max.	Units	Con	ditions	
	.,	0.8 x V			V	Output Logic High, I = 3 mA, Std. Drive		
Output Logic Lovels	V _{OH}	0.8 x V _{DD}	_	_	V	Output Logic I High Drive	High, I = 6 mA,	
Output Logic Levels	V			0.2 × V	V	Output Logic L Std. Drive	low, $l = -3 mA$,	
	V _{OL}	_	_	0.2 x V _{DD}	V	Output Logic L High Drive	low, $l = -6 mA$,	
	+ /+	_	1	1.5		DSA63x2 High Drive,	V _{DD} = 1.8V	
Output Transition Time	t _{RX} /t _{FX}	_	0.5	1.0	ns	20% to 80% C _L = 15 pF	V _{DD} = 2.5V/3.3V	
Rise Time/Fall Time	t _{RY} /t _{FY}	_	1.2	2.0	ns	DSA63x1 Std. Drive, 20% to 80% C _L = 10 pF	V _{DD} = 1.8V	
		_	0.6	1.2			V _{DD} = 2.5V/3.3V	
Desired litter DMC		_	8.5	_		f _{OUT} = 27 MHz Spread Off	V _{DD} = 1.8V	
Period Jitter, RMS	J _{PER}	_	7	_	ps _{RMS}		V _{DD} = 2.5V/3.3V	
Cycle to Cycle litter Book	1	_	50	70		f _{OUT} =	V _{DD} = 1.8V	
Cycle-to-Cycle Jitter, Peak	J _{Cy–Cy}	_	35	60	ps	27 MHz Spread Off	V _{DD} = 2.5V/3.3V	
Period Jitter, Peak-to-Peak		_	70	_	ps	f _{OUT} =	V _{DD} = 1.8V	
	J _{PP}	_	60	_		27 MHz Spread Off	V _{DD} = 2.5V/3.3V	
Spread Spectrum Modulation Frequency	f _{SS}	_	33	_	kHz	_		

- Note 1: Pin 4 V_{DD} should be filtered with 0.1 μF capacitor.
 - 2: Not including current through pull-up resistor on EN pin (if configured).
 - 3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
 - 4: Input waveform must be monotonic with rise/fall time < 10 ms
 - **5:** Output Disable time takes up to two periods of the output waveform + 200 ns.
 - 6: For parts configured with OE, not Standby.
 - 7: Output is enabled if pad is floated or not connected.
 - 8: Time to reach 90% of target V_{DD} . Power ramp rise must be monotonic.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	TJ	-40	_	+150	°C	_
Storage Ambient Temperature Range	T _S	-55	_	+150	°C	_
Soldering Temperature	_	_	+260	_	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

SPREAD SPECTRUM

Ordering Code	Spread Percentage	Spread Type
A	±0.25%	Center-Spread
В	±0.5%	Center-Spread
С	±1.0%	Center-Spread
D	±1.5%	Center-Spread
E	±2.0%	Center-Spread
F	±2.5%	Center-Spread
G	-0.25%	Down-Spread
Н	-0.5%	Down-Spread
I	-1.0%	Down-Spread
J	-1.5%	Down-Spread
К	-2.0%	Down-Spread
L	-3.0%	Down-Spread
M	Custom	Center-Spread or Down-Spread

2.0 PIN DESCRIPTIONS

The DSA63xx is a highly configurable device and can be factory programmed in many different ways to meet the customer's needs. Microchip's ClockWorks[®] Configurator http://clockworks.microchip.com/Timing/ must be used to choose the necessary options, create the final part number, data sheet, and order samples. The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: DSA63XX PIN FUNCTION TABLE

Pin Number	Pin Name	Description
	OE	Output Enable: H = Active, L = Disabled (High Impedance).
(Note 1)	STDBY	Standby: H = Device is active, L = Device is in standby (Low Power Mode).
(Note 1)	SSEN	Spread Spectrum Enable: H = Enabled, L = Disabled.
2	GND	Ground.
3	OUTPUT	Oscillator clock output
4	VDD	Power Supply: 1.71V to 3.63V.

Note 1: DSA630x/1x/3x has a 300 k Ω internal pull-up resistor on Pin 1. DSA634x/5x/7x has no internal pull-up resistor on Pin 1 and needs an external pull-up or to be driven by another chip.

An explanation of the different options listed in Table 2-1 follows.

2.1 Pin 1

This is a control pin and may be configured to fulfill one of three different functions. If not actively driven, a 10 k Ω pull-up resistor is recommended.

2.1.1 OUTPUT ENABLE (OE)

Pin 1 may be configured as OE. Oscillator output may be turned on and off according to the state of this pin.

2.1.2 STDBY

Pin 1 may be configured as Standby. When the pin is low, both output buffer and PLL will be off and the device will enter a low power mode.

2.1.3 SPREAD SPECTRUM ENABLE (SSEN)

This pin, when high, enables spread spectrum modulation of the clock output. Various levels of center-spread and down-spread are available. For more details, see the Spread Spectrum section and the spread spectrum ordering codes in the Product Identification System.

2.2 Pins 2 through 4

Pins 2 and 4 are the supply terminals, GND and VDD respectively. Pin 3 is the clock output, programmable to Standard and High Drive strength settings. Visit ClockWorks[®] Configurator to customize your device.

2.3 Output Buffer Options

The DSA63xx family is available in multiple output driver configurations.

The standard-drive (63x1) and high-drive (63x2) deliver respective output currents of greater than 3 mA and 6 mA at 20%/80% of the supply voltage. For heavy loads of 15 pF or higher, the high-drive option is recommended.

3.0 DIAGRAMS

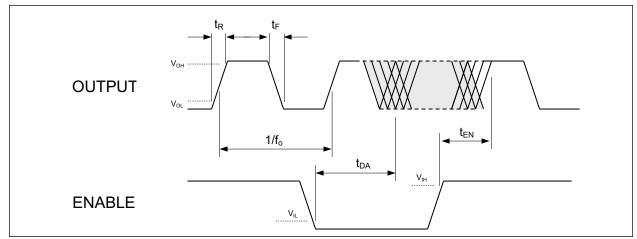


FIGURE 3-1: Output Waveform.

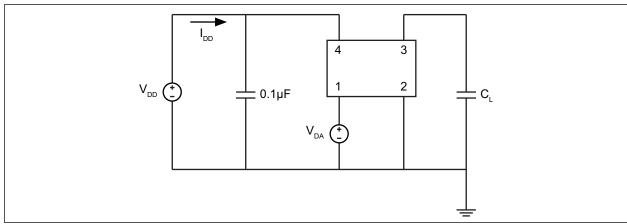


FIGURE 3-2: Test Circuit.

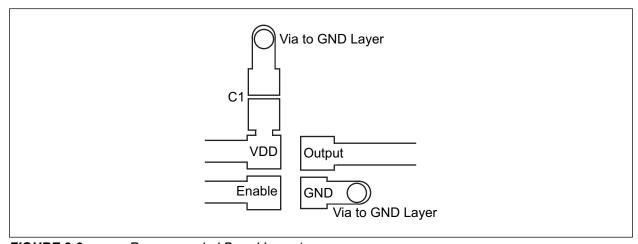


FIGURE 3-3: Recommended Board Layout.

4.0 SPREAD SPECTRUM

Spread spectrum is a slow modulation of the clock frequency over time. The PLL inside the MEMS oscillator is modulated with a triangular wave at 33 kHz. With such a slow modulation, the peak spectral energy of both the fundamental and all the harmonics is spread over a wider frequency range and such an energy is significantly reduced, thus providing an EMI reduction. The triangular wave is chosen because of its flat spectral density.

The DSA63xx MEMS oscillator family offers several modulation options: the spreading is either center-spread or down-spread with respect to the clock frequency. Center-spread ranges from $\pm 0.25\%$ to $\pm 2.5\%$, while down-spread ranges from -0.25% to -3%.

If the clock frequency is 100 MHz and center-spread with $\pm 1\%$ is chosen, the output clock will range from 99 MHz to 101 MHz. If down-spread with -2% is chosen, the output clock will range from 98 MHz to 100 MHz.

Figure 4-1 and Figure 4-2 show a spectrum example of the DSA6331 with a 33.333 MHz clock, modulated with center-spread of ±1%.

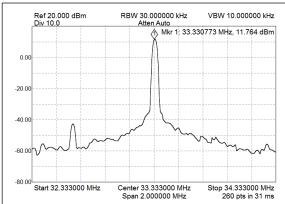


FIGURE 4-1: DSA6331 Spectrum at 33.333 MHz with Modulation Turned Off.

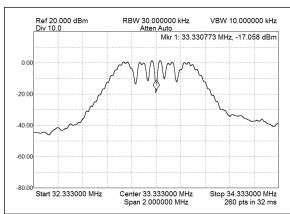


FIGURE 4-2: DSA6331 Spectrum at 33.333 MHz with Modulation Turned On.

It is noticeable that the spread spectrum provides a reduction of about 10 dB from the peak power. Such a reduction may also be estimated by the following equation:

EQUATION 4-1:

 $EMIReduction = 10 \times Log10(|S| \times fc \div RBW)$

Where:

S = Peak-to-peak spread percentage (0.01 in this example).

fc = Carrier frequency (33.333 MHz in this example). RBW = Resolution bandwidth of the spectrum analyzer (30 kHz in this example).

The theoretical calculation for this example provides 10.45 dB, which is consistent with the measurement.

Similarly to the fundamental frequency, all the harmonics are spread and attenuated in similar fashion. Figure 4-3 shows how the DSA6331 fundamental at 33.333 MHz and its odd harmonics are attenuated when various types of modulations are selected. For picture clarity, only the center-spread options are shown. However, down spread with corresponding percentage provides the same level of harmonic attenuation (e.g. center-spread of $\pm 1\%$ provides the same harmonics attenuation of down spread with -2%).

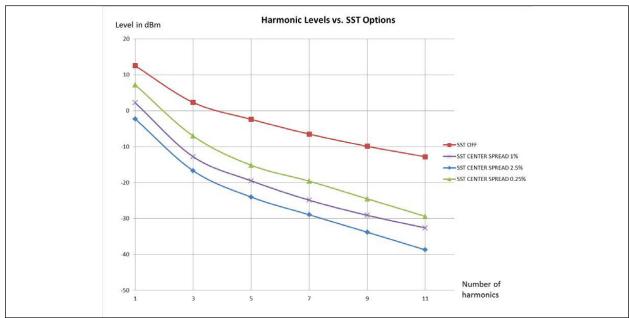


FIGURE 4-3: DSA6331 Harmonic Levels with Various Spread Spectrum Options.

DSA63XX

5.0 SOLDER REFLOW PROFILE

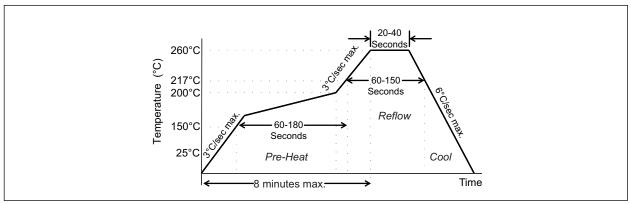


FIGURE 5-1: Solder Reflow Profile.

MSL 1 @ 260°C refer to JSTD-020C					
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.				
Preheat Time 150°C to 200°C	60 to 180 sec.				
Time maintained above 217°C	60 to 150 sec.				
Peak Temperature	255°C to 260°C				
Time within 5°C of actual Peak	20 to 40 sec.				
Ramp-Down Rate	6°C/sec. max.				
Time 25°C to Peak Temperature	8 minutes max.				

6.0 PACKAGING INFORMATION

6.1 Package Marking Information



7.0mm x 5.0mm VDFN* 5.0mm x 3.2mm VDFN*

3.2mm x 2.5mm VDFN*

2.5mm x 2.0mm VLGA*

Example

0400000

DAP1834

0287

XXXXXXX XXXYYWW 0SSS

•

4-Lead VFLGA* 2.0mm x 1.6mm 1.6mm x 1.2mm

Example

XXXX SSS



Legend: XX...X Product code or customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)

WW Week code (week of January 1 is week '01')

SSS Alphanumeric traceability code

e3 Pb-free JEDEC® designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

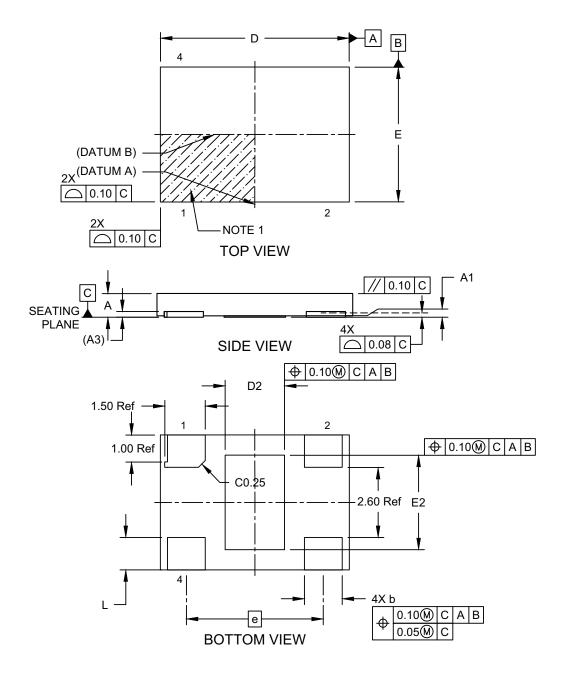
•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar () and/or Overbar () symbol may not be to scale.

4-Lead Very Thin Dual Flatpack, No Lead Package (JZA) - 7x5x0.9 mm Body [VDFN] With 2.2x3.5 mm Exposed Pad

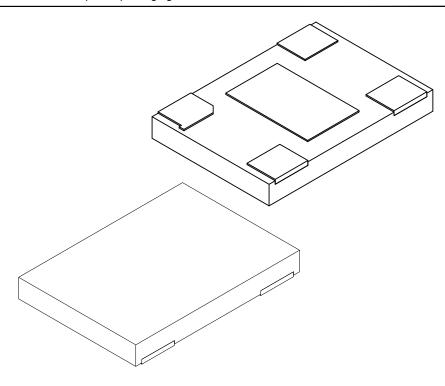
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1025-JZA Rev B Sheet 1 of 2

4-Lead Very Thin Dual Flatpack, No Lead Package (JZA) - 7x5x0.9 mm Body [VDFN] With 2.2x3.5 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			S
Dimension	Limits	MIN	NOM	MAX
Number of Terminals	N		004	
Pitch	е		5.08 Ref	
Overall Height	Α	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Terminal Thickness	A3	0.203 Ref		
Overall Length	D	6.90	7.00	7.10
Exposed Pad Length	D2	2.10	2.20	2.30
Overall Width	Е	4.90	5.00	5.10
Exposed Pad Width	E2	3.40	3.50	3.60
Terminal Width	b	1.35	1.40	1.45
Terminal Length	Ĺ	1.10	1.20	1.30

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the pin 1 area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

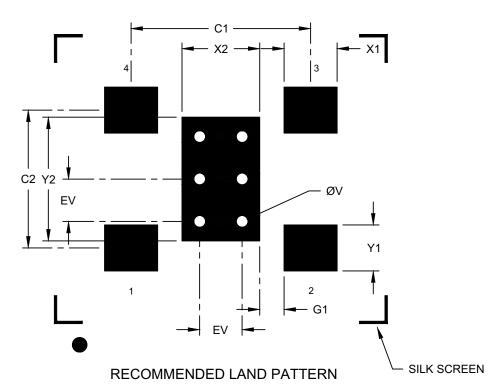
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1025-JZA Rev B Sheet 2 of 2

4-Lead Very Thin Dual Flatpack, No Lead Package [JZA] - 7x5x0.9 mm Body [VDFN] With 2.2x3.5 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Optional Center Pad Width	X2			2.30
Optional Center Pad Length	Y2			3.60
Contact Pad Spacing	C1		5.08	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (Xnn)	X1			1.50
Contact Pad Length (Xnn)	Y1			1.30
Contact Pad to Center Pad (Xnn)	G1	0.69		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

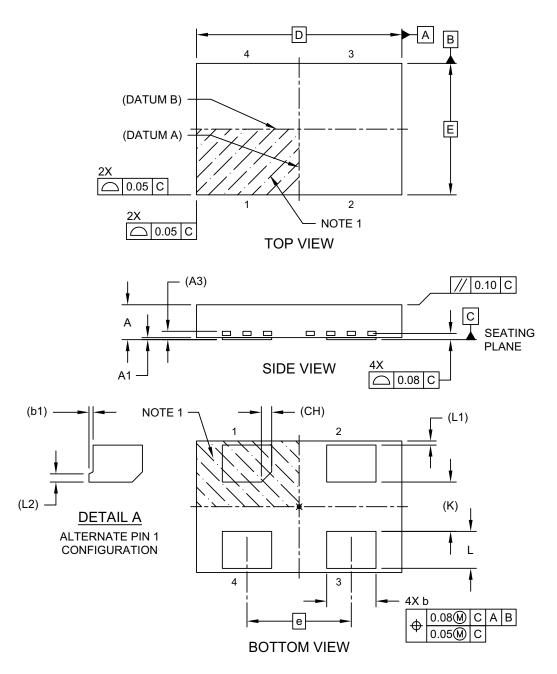
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3025-JZA Rev B

4-Lead Very Thin Plastic Dual Flat, No Lead Package (H6A) - 5x3.2 mm Body [VDFN]

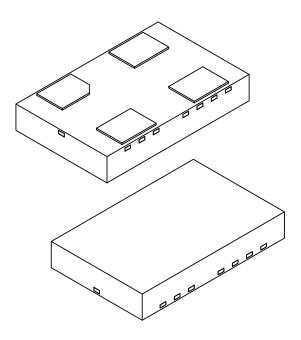
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1008-H6A Rev C Sheet 1 of 2

4-Lead Very Thin Plastic Dual Flat, No Lead Package (H6A) - 5x3.2 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			S	
Dimension	Limits	MIN	NOM	MAX	
Number of Terminals	N		4		
Pitch	е		2.54 BSC		
Overall Height	Α	0.80	0.85	0.90	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.20 REF			
Overall Length	D	5.00 BSC			
Overall Width	Е	3.20 BSC			
Terminal Width	b	1.15	1.20	1.25	
Terminal 1 Tab	b1		0.10 REF		
Terminal Length	L	0.80	0.90	1.00	
Terminal Pull Back	L1	0.10 REF			
Terminal 1 Tab	L2	0.20 REF			
Terminal 1 Chamfer	CH	0.25 REF			
Terminal Spacing	K		1.20 REF		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

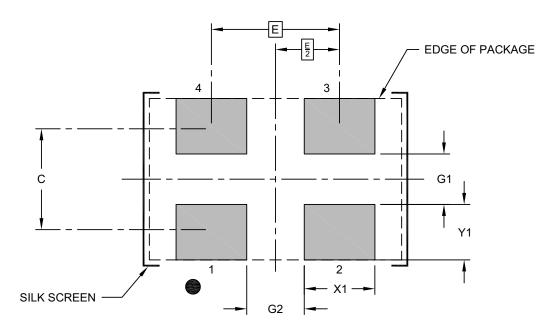
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1008-H6A Rev C Sheet 2 of 2

4-Lead Very Thin Plastic Dual Flat, No Lead Package (H6A) - 5x3.2 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	M	IILLIMETER:	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	Е		2.54	
Contact Pad Spacing	С		2.00	
Contact Pad Width (X4)	X1			1.40
Contact Pad Length (X4)	Y1			
Contact Pad to Center Pad (X2)	G1	1.00		1.10
Contact Pad to Contact Pad (X2)	G2	1.14		
Terminal 1 Contact Pad Chamfer	CH		0.30	

Notes:

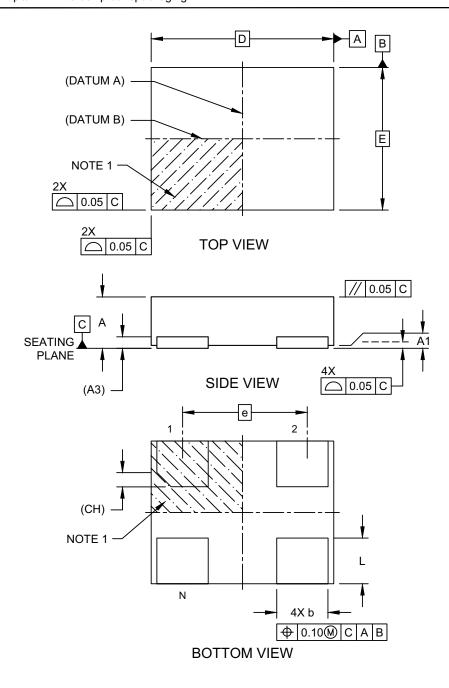
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3008 Rev C

4-Lead Very Thin Plastic Dual Flatpack No-Lead (H4A) - 3.2x2.5 mm Body [VDFN]

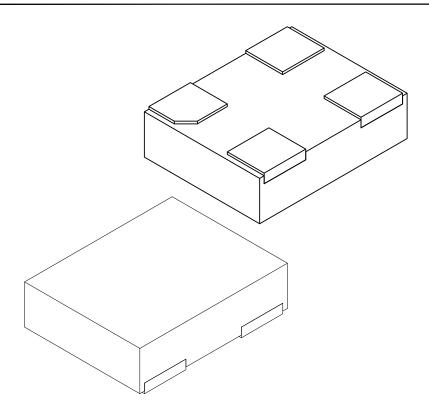
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1006-H4A Rev C Sheet 1 of 2

4-Lead Very Thin Plastic Dual Flatpack No-Lead (H4A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension	n Limits	MIN	NOM	MAX	
Number of Terminals	N		4		
Pitch	е	2.10 BSC			
Overall Height	Α	0.80 0.85 0.90			
Standoff	A1	0.00	0.02	0.05	
Overall Length	D	3.20 BSC			
Overall Width	E	2.50 BSC			
Terminal Width	b	0.85	0.90	0.95	
Terminal Length	L	0.70	0.80	0.90	
Terminal 1 Index Chamfer	CH	0.25 REF			

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated

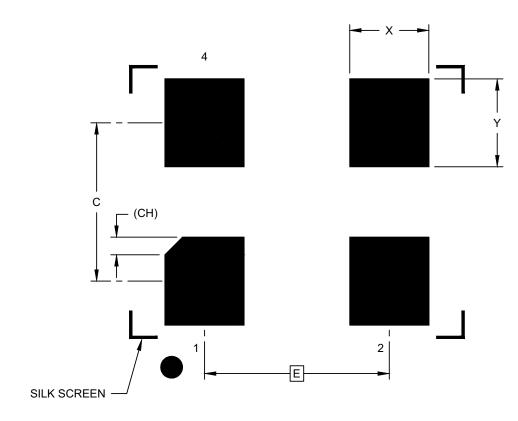
Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1006-H4A Rev C Sheet 2 of 2

4-Lead Very Thin Plastic Dual Flatpack No-Lead (H4A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	MILLIMETERS			
Dimension	MIN	NOM	MAX		
Contact Pitch		2.10 BSC			
Contact Pad Spacing	С		1.80		
Contact Pad Width (X4)	Х			0.90	
Contact Pad Length (X4)	Υ			1.00	
Contact 1 Index Chamfer	CH		0.20 REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M $\,$

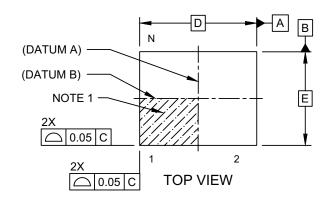
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

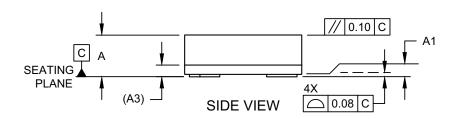
REF: Reference Dimension, usually without tolerance, for information purposes only.

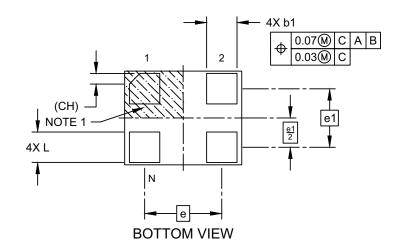
Microchip Technology Drawing C04-3006-H4A Rev C

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



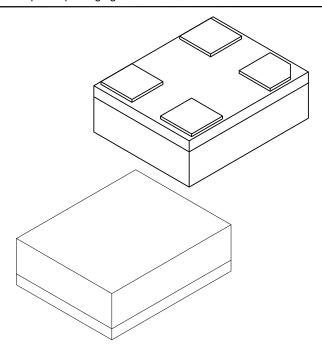




Microchip Technology Drawing C04-1202-AUA Rev C Sheet 1 of 2

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	N	IILLIMETER:	S			
Dimension	MIN	NOM	MAX			
Number of Terminals	N		4			
Terminal Pitch	е		1.65 BSC			
Terminal Pitch	e1	1.25 BSC				
Overall Height	Α	0.79	0.84	0.89		
Standoff	A1	0.00	0.02	0.05		
Substrate Thickness (with Terminals)	A3	0.20 REF				
Overall Length	D	2.50 BSC				
Overall Width	Е	2.00 BSC				
Terminal Width	b1	0.60	0.65	0.70		
Terminal Length	L	0.60	0.65	0.70		
Terminal 1 Index Chamfer	CH	-	0.225	-		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

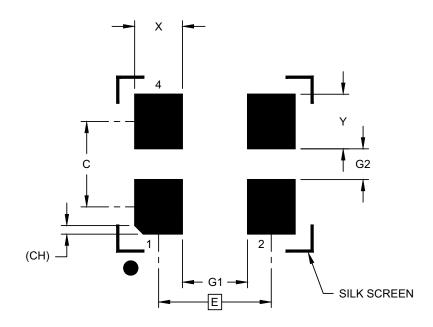
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1202-AUA Rev C Sheet 2 of 2

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	ntact Pitch E		1.65 BSC			
Contact Spacing	С					
Contact Width (X4)	Х			0.70		
Contact Pad Length (X4)				0.80		
Space Between Contacts (X2)	G1	0.95				
Space Between Contacts (X2)	G2	0.45				
Contact 1 Index Chamfer	C	.13 X 45° RE	F			

Notes:

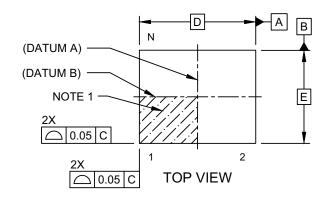
1. Dimensioning and tolerancing per ASME Y14.5M

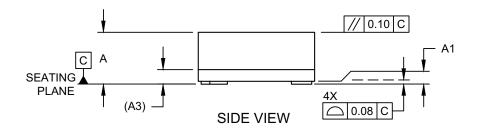
 ${\tt BSC: Basic \ Dimension. \ Theoretically \ exact \ value \ shown \ without \ tolerances.}$

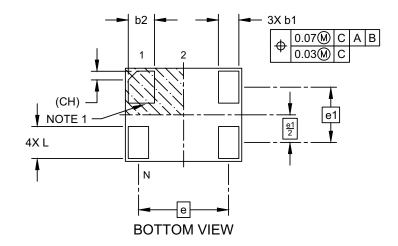
Microchip Technology Drawing C04-3202-AUA Rev C

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



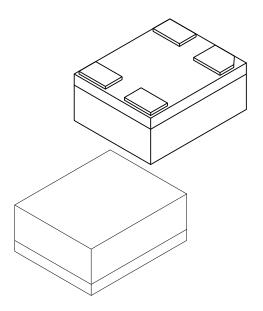




Microchip Technology Drawing C04-1200-ASA Rev E Sheet 1 of 2

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Terminals	4				
Terminal Pitch	е		1.55 BSC		
Terminal Pitch	e1		0.95 BSC		
Overall Height	Α	0.79	0.84	0.89	
Standoff	A1	0.00	0.02	0.05	
Substrate Thickness (with Terminals)	A3	0.20 REF			
Overall Length	D	2.00 BSC			
Overall Width	Е	1.60 BSC			
Terminal Width	b1	0.30	0.35	0.40	
Terminal Width	b2	0.40	0.45	0.50	
Terminal Length	L	0.50	0.55	0.60	
Terminal 1 Index Chamfer	CH	-	0.15	-	

Notes:

Note:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M $\,$

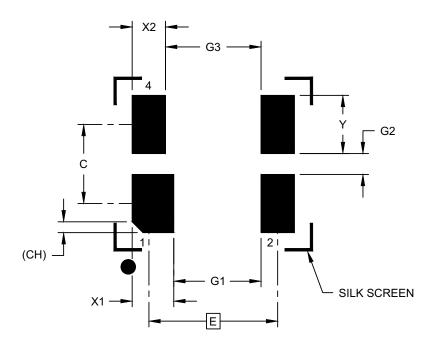
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1200-ASA Rev E Sheet 2 of 2

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units				
Dimension	Dimension Limits				
Contact Pitch	itch E		1.55 BSC		
Contact Spacing	С		0.95		
Contact Width (X1)	X1			0.50	
Contact Width (X3)	X2			0.40	
Contact Pad Length (X4)	Υ			0.70	
Space Between Contacts	G1	1.05			
Space Between Contacts	G2	0.25			
Space Between Contacts	G3	1.15			
Contact 1 Index Chamfer	ntact 1 Index Chamfer CH			F	

Notes:

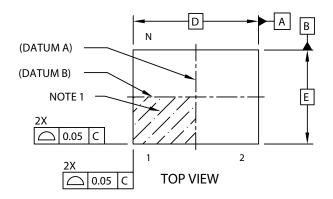
1. Dimensioning and tolerancing per ASME Y14.5M

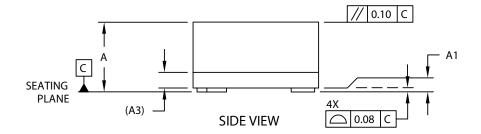
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

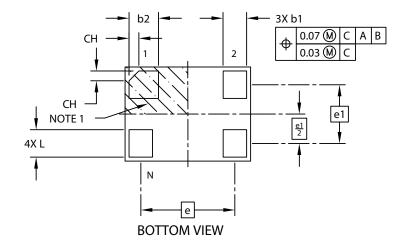
Microchip Technology Drawing C04-3200-ASA Rev E

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



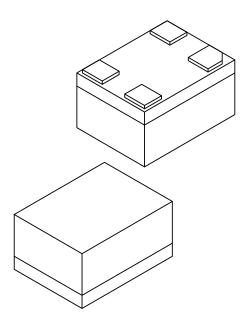




Microchip Technology Drawing C04-1199B Sheet 1 of 2

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		ALLINAETEDC		
	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Terminals		4			
Terminal Pitch	е		1.20 BSC		
Terminal Pitch	e1		0.75 BSC		
Overall Height	Α	0.79	0.84	0.89	
Standoff	A1	0.00	0.02	0.05	
Substrate Thickness (with Terminals)	hickness (with Terminals) A3 0.20 REF				
Overall Length	D	1.60 BSC			
Overall Width	E	1.20 BSC			
Terminal Width	b1	0.25	0.30	0.35	
Terminal Width	b2	0.325	0.375	0.425	
Terminal Length	L	0.30	0.35	0.40	
Terminal 1 Index Chamfer	CH	-	0.125	-	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

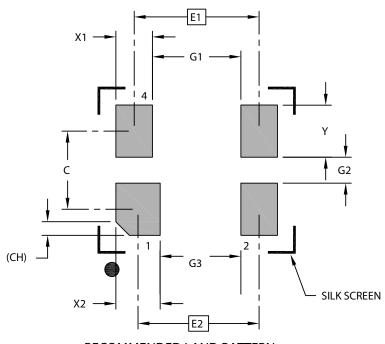
 ${\it BSC: Basic Dimension. Theoretically exact value shown without tolerances.}$

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1199B Sheet 2 of 2

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units		ALL LA ACTEDO			
	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	Contact Pitch E1		1.20 BSC			
C ontact Pitch	E2		1.16 BSC			
Contact S pacing	C		0.75			
Contact Width (X3)	X1			0.35		
Contact Width	X2			0.43		
Contact Pad Length (X4)	Υ			0.50		
Space Between Contacts	G1	0.85				
Space Between Contacts (X2)	52	0.25				
Space Between Contacts	G3	0.77				
Contact 1 Index Chamfer	0.13	X 45° REF				

Notes:

Note:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. The value in parenthesis, next to the item description is a unit multiplier.

Microchip Technology Drawing C04-3199B



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

 Initial creation of DSA63xx Microchip data sheet DS20006189A.

Revision B (May 2019)

- Ensured part number of DSA63xx is correctly reflected across entire document.
- Clarified Conditions for Frequency Stability in Electrical Characteristics table.
- Revised the Product Identification System section to better reflect the current naming convention.

Revision C (November 2022)

 Added the 7.0 mm x 5.0 mm VDFN, 5.0 mm x 3.2 mm VDFN and 3.2 mm x 2.5 mm VDFN package options throughout the document.

Revision D (June 2025)

- · Updated the Product Identification System.
- Updated the Package Marking Information drawing.
- Updated all the package outline drawings to reflect the most current version of each.



NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u>x</u>	<u>x</u>	<u>x</u>	<u>x</u>	<u>x</u>	<u>x</u>	<u>x</u>	- <u>xxx.xxxx</u>	<u>x</u>	<u>xxx</u>	
Device	Pin 1 Definition	Output Drive Strength	•	Temperature Range	Frequency Stability	Spread Spectrum	Revision	Frequency	Media Type	Automotive Suffix	
Device:	DS	A63:		all, Ultra-Low P with Spread S ve			a) DSA63	312JI2DB-100.0000			
Pin Definition: Output Drive Strength: Packages:	0 1 3 4 5 7 1 2 A B C J M H	= = = =	4-Lead 5.0 4-Lead 3.2 4-Lead 2.5 4-Lead 2.0 4-Lead 1.6	Internal Pull- Pull-up Pull-up None None None Mm x 5.0 mm mm x 3.2 mm mm x 2.5 mm mm x 2.6 mm mm x 1.6 mm mm x 1.2 mm	VDFN VDFN VDFN VLGA VFLGA VFLGA		Ultra-Small, Ultra-Low Power MEMS C tor with Spread Spectrum, Pin 1 = STI with Internal Pull-Up, High Drive Stren Lead 2.5 mm x 2.0 mm VLGA, Industr Temperature, ±25 ppm Stability, ±1.5% ter-Spread, Revision B, 100 MHz Frequ 140/Tube, Automotive Suffix b) DSA6301HE1LB-016.0000TVAO: Ultra-Small, Ultra-Low Power MEMS C tor with Spread Spectrum, Pin 1 = OE Internal Pull-Up, Standard Drive Stren Lead 1.6 mm x 1.2 mm VFLGA, Exten Commercial Temperature, ±50 ppm St ity, -3.0% Down-Spread, Revision B, 16 MHz Frequency, 1,000/Reel, Auton Suffix c) DSA6331MI2AB-050.5000BVAO: Ultra-Small, Ultra-Low Power MEMS C tor with Spread Spectrum, Pin 1 = SSI with Internal Pull-Up, Standard Drive Strength, 4-Lead 2.0 mm x 1.6 mm VF				
Range: Frequency Stability:	L I E 1 2 3	= = = =	–40°C to +7 –40°C to +8	105°C (Extende 85°C (Industria 70°C (Extended	ed Industrial) I)		Note 1:	Industrial Temper ±0.25% Center-S 50.5 MHz Freque tive Suffix Tape and Reel iden catalog part numbe used for ordering pr	Spread, Revisency, 3,000/R	ion B, eel, Automo- ears in the This identifier is	
Spread Spectro	um: ABCDEFGHIJKLM	= = = = = =	±0.25% Ce ±0.5% Cen ±1.0% Cen ±1.5% Cen ±2.0% Cen ±2.5% Cen -0.25% Do -0.5% Dow -1.0% Dow -1.5% Dow -2.0% Dow Custom	ter-Spread ter-Spread ter-Spread ter-Spread wn-Spread 'm-Spread 'm-Spread 'm-Spread 'm-Spread			Note:	used for ordering purposes and is not prin the device package. Check with your Micr Sales Office for package availability with th and Reel option. The: Please visit Microchip ClockV Configurator Website to configurate part number for customized free http://clockworks.microchip.com/ti			
Revision:	В	=	Revision B								
Frequency:	xxx			ed Frequency b MHz and 100.00							
Media Type:	 	ank>= ank>= ank>= ank>= =	72/Tube, 14 110/Tube (0 140/Tube (0	00 pce. min. (A 14 pce. min. (B C Package Opti I Package Opti & H Package	Package Op ion) ion)						
Automotive Su	ıffix: Vxx	(=	The "xx" is	assigned by Mi	icrochip.						



NOTES:

Microchip Information

Trademarks

The "Microchip" name and logo, the "M" logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries ("Microchip Trademarks"). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks.

ISBN: 979-8-3371-1380-7

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code.
 Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.