AM0010 TRM

Revision v.44

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Online version of this document:

https://wiki.trenz-electronic.de/display/PD/AM0010+TRM

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4 Overview

The Trenz Electronic AM0010 module is an industrial grade module based on AMD Xilinx.

Refer to http://trenz.org/am0010-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC**
  - Device: ZU1 / ZU2 / ZU3 / ZU4 / ZU5 [1)]
  - Engine: CG / EG / EV [1)]
  - Speedgrade: -1 / -2 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: SFVC784
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM with ECC [2)]
  - 8 GByte e.MMC [3)]
  - Optional HyperFlash [4)]
  - 2 x 64 MByte Serial Flash [5)]
  - EEPROM with MAC address
- **On Board**
  - Gigabit Ethernet Transceiver
  - USB Transceiver
  - OPTIGA Trust M
  - CryptoAuthentication
  - Oscillator
  - Analog Multiplexer
- **Interface**
  - 2 x B2B Connector (ADM6)
    - up to 204 PL IO
    - up to 22 PS MIO
    - 4 GTR
    - 4 GTH (with ZU4 and higher)
    - ETH, USB, I2C, JTAG, ...
- **Power**
  - 5 V ... 12 V power supply via B2B Connector needed.
- **Dimension**
  - 56.4 mm x 40 mm
- **Notes**

  [1)] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

  [2)] Up to 32 GByte are possible with a maximum bandwidth of 2400 MBit/s.

  [3)] Up to 64 GByte are possible.

  [4)] Up to 64 MByte are possible.

  [5)] Up to 2 x 256 MByte are possible.

4.2 Block Diagram

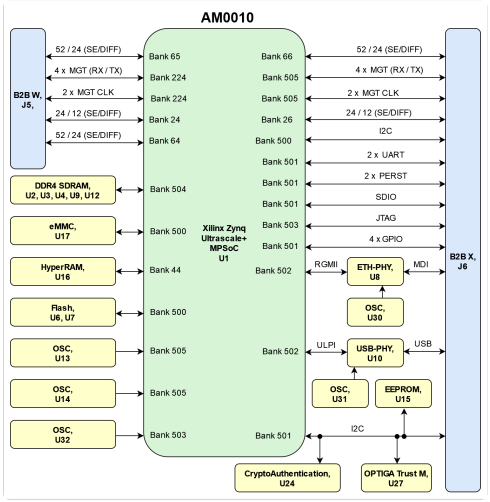

Figure 1: AM0010 block diagram

4.3 Main Components

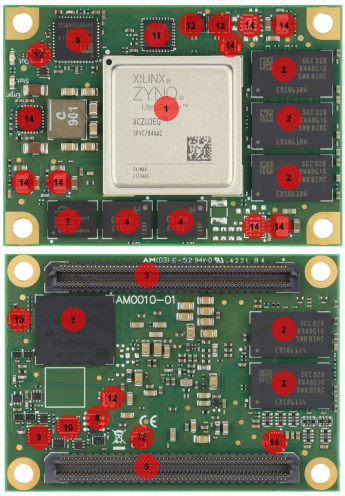

Figure 2: AM0010 main components

1. FPGA, U1
2. DDR4, U2, U3, U9, U12, U14
3. eMMC, U17
4. Quad SPI Flash, U6, U7
5. Connector, J5, J6
6. Ethernet Transceiver, U8
7. HyperFlash, U16
8. EEPROM, U15
9. OPTIGA Trust M, U27
10. CryptoAuthentication, U24
11. USB Transceiver, U10
12. Oscillator, U13, U14, U30, U31, U32
13. Analog Multiplexer, U38
14. Power Supply, U5, U11, U18, U19, U20, U21, U22, U23, U28

4.4 Initial Delivery State

Storage device name	Content	Notes
DDR4 SDRAM	not programmed	
eMMC	not programmed	
Quad SPI Flash	not programmed	
HyperFlash	not programmed	
EEPROM	not programmed besides factory programmed MAC address	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT [1)]	Notes
B2B	J5	HP	104 SE / 48 DIFF	
B2B	J5	MGT PL	4 x MGT (RX/TX)	
B2B	J5	MGT PL	2 x MGT CLK	
B2B	J5	HD	24 SE / 12 DIFF	
B2B	J6	HP	52 SE / 24 DIFF	
B2B	J6	MGT PS	4 x MGT (RX/TX)	
B2B	J6	MGT PS	2 x MGT CLK	
B2B	J6	HD	24 SE / 12 DIFF	
B2B	J6	MIO	2 x I2C	
B2B	J6	MIO	2 x UART	
B2B	J6	MIO	2 x PERST	
B2B	J6	MIO	SDIO	
B2B	J6	MIO	JTAG	
B2B	J6	MIO	4 x GPIO	
B2B	J6	ETH		
B2B	J6	USB		

Table 2: Board Connectors

[1)] IO CNT depends on assembly variant. E.g. the MGTs are not available for all FPGAs

5.2 Test Points

Test Point	Signal	Notes
TP1	PROG_B#	pulled-up to V_IO_CFG
TP2	VTT	
TP3	VTT	
TP4	VREFA	
TP5	VREFA	
TP6	0.85V	
TP7	0.85V	
TP8	DDR_1V2	
TP9	DDR_1V2	
TP10	MGTAVCC	
TP11	MGTAVCC	
TP12	DDR_2V5	
TP13	DDR_2V5	
TP14	PL_VCU_0V9	
TP15	PL_VCU_0V9	
TP16	1.8V	
TP17	1.8V	

Test Point	Signal	Notes
TP18	3.3V_SEQ	
TP19	3.3V_SEQ	
TP20	3.3V	
TP21	3.3V	

Table 3: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12, U14	SoC - PS	
eMMC	U17	SoC - PS	
Quad SPI Flash	U6, U7	SoC - PS	Booting.
Gigabit Ethernet Transceiver	U8	SoC - PS	
HyperFlash	U16	SoC - PL	
EEPROM	U15	SoC - PS	
OPTIGA Trust M	U27	SoC - PS	
CryptoAuthentication	U24	SoC - PS	
USB 2 Transceiver	U10	SoC - PS	
Oscillator	U13	SoC - PS	135 MHz

Chip/Interface	Designator	Connected To	Notes
Oscillator	U14	SoC - PS	100 MHz
Oscillator	U30	ETH PHY	25 MHz
Oscillator	U31	USB PHY	24 MHz
Oscillator	U32	SoC	33 MHz
Analog Multiplexer	U38	SoC	Voltage measuring with Xilinx internal ADC.

Table 4: On board peripherals

7 Configuration and System Control Signals

Connector. Pin	Signal Name	Direction[1)]	Description
J6.A59	V_BAT	IN	Input voltage for VCC_PSBATT [2) 3)].
J6.B58	RST_M2C#	OUT	Module reset for baseboard peripheral.
J6.C53	DONE	OUT	Signal PS_DONE [2)].
J6.C54 / J6.C55 / J6.C56 / J6.C57	MODE0..3	IN	Boot mode selection [2)]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
J6.C58	PS_SRST#	IN	SoC Soft Reset [2)].
J6.C59	PS_POR#	IN	SoC Power-on-reset [2)]. PWR_GOOD deasserts module reset.
J6.D56 / J6.D57	DX_P / DX_N	IN	Temperature sensing diode pin. When not used, tie to GND.
J6.D58	PWR_EN	IN / OUT	Power Enable. Controlled module internally. Can be used to delay power on sequencing or disable power. Tie only to GND or leave floating.
J6.D59	PWR_GOOD	OUT	Power good status.
J6.D51 / J6.D52 / J6.D54 / J6.D55	TDI/TCK/ TDO/TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: V_IO_CFG

Connector. Pin	Signal Name	Direction[1)]	Description
LED D1 / D2	ERR_STATUS / ERR_OUT	---	PS_STATUS_ERROR_OUT / PS_ERROR_OUT [2)].

Table 5: Controller signal.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2)] See UG1085 for additional information.

[3)] See Recommended Operating Conditions (see page 20).

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction[1)]	Notes
V_MOD1	J5.A7 / J5.A15 / J5.A47 / J5.A55 / J5.B5 / J5.B11 / J5.B17 / J5.B45 / J5.B51 / J5.B57 / J6.C5 / J6.C11 / J6.C17 / J6.D7 / J6.D15	IN	
1.8V	J5.C7 / J5.C15 / J6.B7 / J6.B15	OUT	
V_IO_W01	J5.D3 / J5.D17	IN	
V_IO_W3	J5.D40	IN	
V_IO_W45	J5.D43 / J5.D57	IN	
V_IO_X01	J6.A3 / J6.A17	IN	
V_BAT	J6.A59	IN	
V_IO_X3	J6.B35	IN	
3.3V	J6.B59	OUT	
V_IO_CFG	J6.C52	IN	

Table 6: Module power rails.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals (see page 13).
1 [1)]	V_BAT	3.3 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.
2	V_MOD1	12 V	-	Main Power supply.	Main module power supply. 3 A recommended. Power consumption depends mainly on design and cooling solution.
3 [1)]	PWR_EN	-	PU [2)], 3.3 V	Power release.	Controlled module internally. Can be used to delay power on sequencing or disable power. Tie only to GND or leave floating.
4	PWR_GOOD	-	PU [2)], 3.3 V	Power good status.	Module power on sequencing finished. Periphery and variable bank voltages can be enabled on carrier.
5 [1)]	3.3V / 1.8V	-	-	Module generated output voltages.	Voltages are available after PWR_GOOD deassertion. These voltages can be used ▪ to supply bank voltages,

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
					▪ to supply periphery and/ or ▪ as power good signal to enable external power regulators. Important: Consider maximum power consumption.
5	V_IO_W01 / V_IO_W45 / V_IO_X01 / V_IO_W3 / V_IO_X3 / V_IO_CFG	3)	-	Module bank voltages.	Enable bank voltages after PWR_GOOD deassertion. To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on it is recommended to enable bank voltages before or at the same time as external logic,
6 1)	-	-	-	Reset handling.	RST_M2C# delivers external periphery reset. See Configuration and System Control Signals (see page 13).

Table 7: Baseboard Design Hints

1) (optional)

2) (on module)

3) See DS925 for additional information.

9 Board to Board Connectors

The Andromeda modules use Samtec AcceleRate HD High-Density on bottom side.

- ADM6-60-01.5-L-4-2 (compatible to ADF6-60-03.5-L-4-2), (240 pins, "60" per row)

The Andromeda carriers use Samtec AcceleRate HD High-Density on top side.

- ADF6-60-03.5-L-4-2 (compatible to ADF6-60-01.5-L-4-2), (240 pins, "60" per row)

9.1 Features

- Board-to-Board Connector 240-pins, 60 contacts per row
- 0.025" (0.635 mm) pitch
- Data Rate: max 56 Gbps
- Mates with: ADM6/APF6
- Insulator Material: LCP, Black
- Contact Material: Copper Alloy
- Plating: Au or Sn over 50 µ" (1.27 µm) N
- Operating Temperature Range: -55 °C to +125 °C
- PCIe 5.0 capable: Yes
- Lead-Free Solderable: Yes
- RoHS Compliant: Yes

9.2 Connector Mating height

When using the same type on baseboard, the mating height is 5mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
30095	REF-30095	ADM6-60-01.5-L-4-2	5 mm
31137	REF-31137	ADF6-60-03.5-L-4-2	5 mm

Table 8: Connectors.
The module can be manufactured using other connectors upon request.

9.3 Connector Speed Ratings

The AcceleRate HD High-Density connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm	10/ 25/ 56 Gbps

Table 9: Speed rating.

9.4 Current Rating

Current rating of Samtec AcceleRate HD High-Density B2B connectors is 1.34 A per pin (4 pins powered)

9.5 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
V_MOD1	Main input power supply	-0.3	18	V
V_IO_W01	HP FPGA Bank 65 voltage	-0.500	2.000	V
V_IO_W3	HD FPGA Bank 24 voltage	-0.500	3.400	V
V_IO_W45	HP FPGA Bank 64 voltage	-0.500	2.000	V
V_IO_X01	HP FPGA Bank 66 voltage	-0.500	2.000	V
V_BAT 1)	FPGA Battery Voltage		6	V
V_IO_X3	HD FPGA Bank 24 voltage	-0.500	3.400	V
V_IO_CFG	PS FPGA Bank 501 and 503 Voltage	-0.3	3.630	V

Table 10: AM0010 absolute maximum ratings

1) It is possible to use a resistor instead of the LDO but then, consider the different min (-0.500 V) / max (2.000 V) values.

*) Stresses beyond those listed under Absolute Maximum Ratings (see page 0) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition (see page 0). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information[1]

1 https://wiki.trenz-electronic.de/display/PD/Article+Number+Information

- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

Parameter	Min	Max	Units	Reference Document
V_MOD1	4.5	16	V	See TPS54A24 and FS1406 datasheets.
V_IO_W01	0.950	1.900	V	See FPGA datasheet.
V_IO_W3	1.140	3.400	V	See FPGA datasheet.
V_IO_W45	0.950	1.900	V	See FPGA datasheet.
V_IO_X01	0.950	1.900	V	See FPGA datasheet.
V_BAT [1)]	2.0	5.5	V	See AP7354D datasheet.
V_IO_X3	1.140	3.400	V	See FPGA datasheet.
V_IO_CFG	1.710	3.465	V	See FPGA datasheet.

Table 11: Recommended operating conditions.

[1)] Using a resistor instead of the LDO is possible which leads to different min (1.2 V) / max (1.89 V) values.

10.3 Physical Dimensions

- Module size: 56.4 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 2 mm.

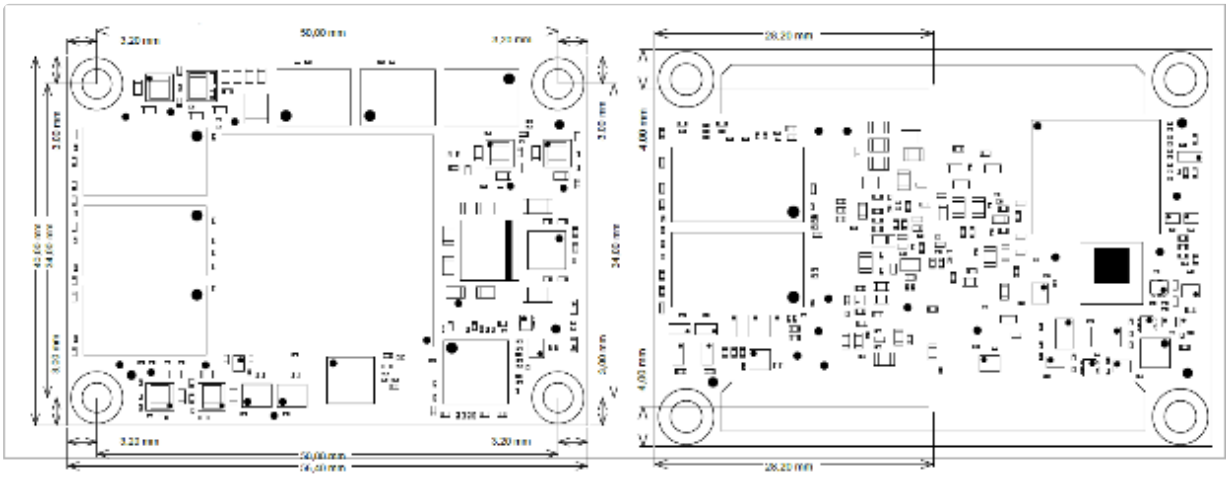

Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop AM0010 overview page	
English page[2]	German page[3]

Table 12: Trenz Electronic Shop Overview

2 https://shop.trenz-electronic.de/en/search?sSearch=AM0010
3 https://shop.trenz-electronic.de/de/search?sSearch=AM0010

12 Revision History

12.1 Hardware Revision History

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Link
-	REV01	First Production Release	REV01[4]

Table 13: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

12.2 Document Change History

Date	Revision	Contributor	Description
2024-07-31	v.44 (see page 5)	John Hartfiel[5]	• Fix PDF Download Link
2023-02-08	v.43	ED	• Recommended Power up Sequencing modified
2022-03-11	v.42	ED	• Initial Document
--	all	ED[6] , John Hartfiel[7]	• --

Table 14: Document change history.

4 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5.64/AM0010/REV01/Documents
5 https://wiki.trenz-electronic.de/display/~j.hartfiel
6 https://wiki.trenz-electronic.de/display/~e.dyck
7 https://wiki.trenz-electronic.de/display/~j.hartfiel

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13.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH[8]. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List[9] are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)[10].

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2019-06-07

8 http://guidance.echa.europa.eu/
9 https://echa.europa.eu/candidate-list-table
10 http://www.echa.europa.eu/