16-Bit, 250kSPS, Serial, CMOS, Sampling ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS8519

FEATURES

- **0V to 8.192V, ±5V, and ±10V Input Ranges**
- **93dB SNR with 20kHz Input**
- **±1.5LSB Max INL**
- **±1LSB Max DNL; 16 Bits, No Missing Codes**
- **SPI™-Compatible Serial Output with Daisy-Chain (TAG) Feature and 3-State Bus**
- **5V Analog Supply, 1.65V to 5.25V I/O Supply**
- **Pinout Similar to 16-Bit ADS7809 (Low-Speed) and 12-Bit ADS7808 and ADS8508**
- **No External Precision Resistors Required**
- **Uses Internal or External Reference**
- **110mW Typ Power Dissipation at 250kSPS**
- **28-Pin SSOP Package**
- **Simple DSP Interface**

APPLICATIONS

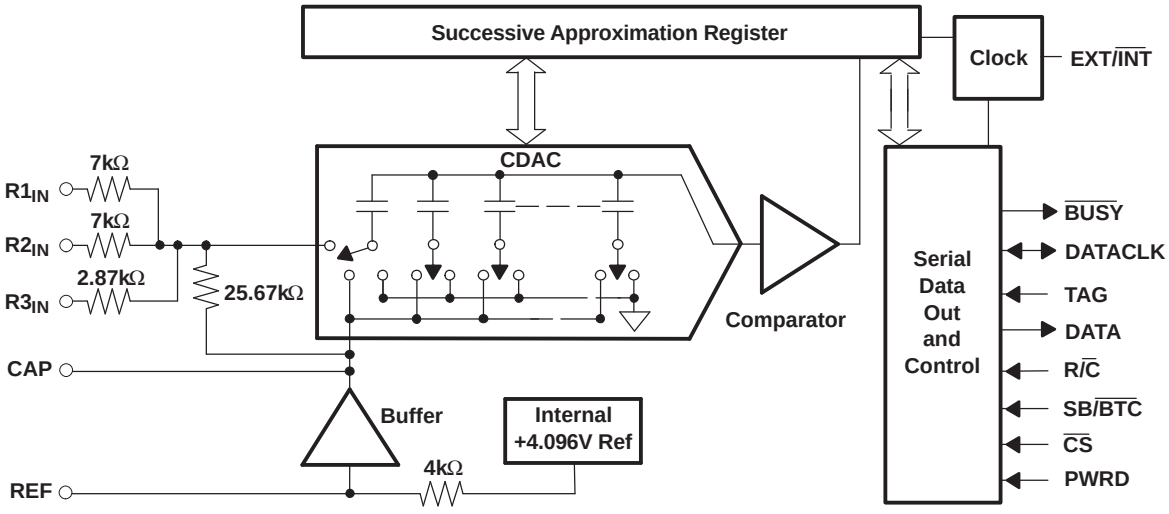
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Digital Signal Processing**
- **Medical Equipment**
- **Instrumentation**

DESCRIPTION

The ADS8519 is a complete 16-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or synchronized to an external data clock. The ADS8519 also provides an output synchronization pulse for ease-of-use with standard DSP processors.

The ADS8519 is specified at a 250kSPS sampling rate over the full temperature range. Internal precision resistors provide various input ranges including ±10V, ±5V, and 0V to 8.192V, while the innovative design allows operation from a single 5V supply with power dissipation under 125mW.

The ADS8519 is available in a 28-pin SSOP package, and is fully specified for operation over the industrial –40°C to +85°C temperature range.



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All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM INL (LSB)	NO MISSING CODES	MINIMUM SINAD (dB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8519IB	±1.5	16-Bit	90	–40°C to +85°C	SSOP-28	DB	ADS8519IBDB	Tube, 50
							ADS8519IBDBR	Tape and Reel, 2000
ADS8519I	±3	15-Bit	87	–40°C to +85°C	SSOP-28	DB	ADS8519IDB	Tube, 50
							ADS8519IDBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Over operating free-air temperature range (unless otherwise noted).

		UNIT
Analog inputs	$R1_{IN}$	±25V
	$R2_{IN}$	±25V
	$R3_{IN}$	±25V
	REF	$+V_{ANA}$ + 0.3V to AGND2 – 0.3V
Ground voltage differences	DGND, AGND2	±0.3V
	V_{ANA}	6V
	V_{DIG}	6V
Digital inputs		$–0.3V$ to $+V_{DIG}$ + 0.3V
Internal power dissipation		700mW
Maximum junction temperature		+165°C
Lead temperature (soldering, 10s)		+300°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, f_s = 250kSPS, and $V_{DIG} = V_{ANA}$ = 5V, using internal reference (unless otherwise specified).

PARAMETER	TEST CONDITIONS	ADS8519I			ADS8519IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
ANALOG INPUT								
Voltage ranges(1)								
Impedance(1)								
Capacitance			50			50		pF
THROUGHPUT SPEED								
Conversion cycle time	Acquire and convert			4			4	µs
Throughput rate		250			250			kSPS

(1) ±10V, ±5V, 0V to 8.192V, etc. (see Table 2)

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, f_s = 250kSPS, and V_{DIG} = V_{ANA} = 5V, using internal reference (unless otherwise specified).

PARAMETER			TEST CONDITIONS	ADS8519I			ADS8519IB			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY										
INL	Integral linearity error			–3		3	–1.5		1.5	LSB(2)
DNL	Differential linearity error			–2		2	–1		1	LSB
	No missing codes			15			16			Bits
	Transition noise(3)				0.67			0.67		LSB
	Full-scale error(4) (5)	±10V range	Internal reference	–0.5		0.5	–0.25		0.25	%FSR
		All other ranges	Internal reference	–0.5	–0.05	0.5	–0.5	–0.05	0.5	
	Full-scale error drift		Internal reference		±7			±7		ppm/°C
	Full-scale error(4) (5)	±10V range	External reference	–0.05	0.003	0.05	–0.05	0.003	0.05	%FSR
		All other ranges	External reference	–0.5		0.5	–0.5		0.5	
	Full-scale error drift		External reference		±2			±2		ppm/°C
	Bipolar zero error(4)			–4		4	–2		2	mV
	Bipolar zero error drift				±2			±2		ppm/°C
	Unipolar zero error(4)	8.192V		–20	6	20	–20	6	20	mV
	Unipolar zero error drift				±0.4			±0.4		ppm/°C
	Recovery to rated accuracy after power down		1µF capacitor to CAP		1			1		ms
	Power supply sensitivity (V_{DIG} = V_{ANA} = V_D)		+4.75V < V_D < +5.25V	–8		8	–8		8	LSB
AC ACCURACY										
SFDR	Spurious-free dynamic range		f_I = 20kHz	95	100		97	100		dB(6)
THD	Total harmonic distortion		f_I = 20kHz		–96	–94		–98	–96	dB
SINAD	Signal-to-(noise+distortion)		f_I = 20kHz	87	91		90	92		dB
			–60dB Input		30			32		dB
SNR	Signal-to-noise ratio		f_I = 20kHz	88	92		91	93		dB
	Full-power bandwidth(7)				500			500		kHz
SAMPLING DYNAMICS										
	Aperture delay				5			5		ns
	Transient response		FS step			2			2	µs
	Overvoltage recovery(8)				150			150		ns
REFERENCE										
	Internal reference voltage		No load	4.076	4.096	4.116	4.076	4.096	4.116	V
	Internal reference source current (must use external buffer)				1			1		µA
	Internal reference drift				8			8		ppm/°C
	External reference voltage range for specified linearity			3.9	4.096	4.2	3.9	4.096	4.2	V
	External reference current drain		External 4.096V ref.			100			100	µA

(2) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV.
(3) Typical rms noise at worst-case transitions and temperatures.
(4) As measured with circuit shown in Figure 29 and Figure 30.
(5) For bipolar input ranges, full-scale error is the worst case of –Full-Scale or +Full-Scale uncalibrated deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.
(6) All specifications in dB are referred to a full-scale ±10V input.
(7) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

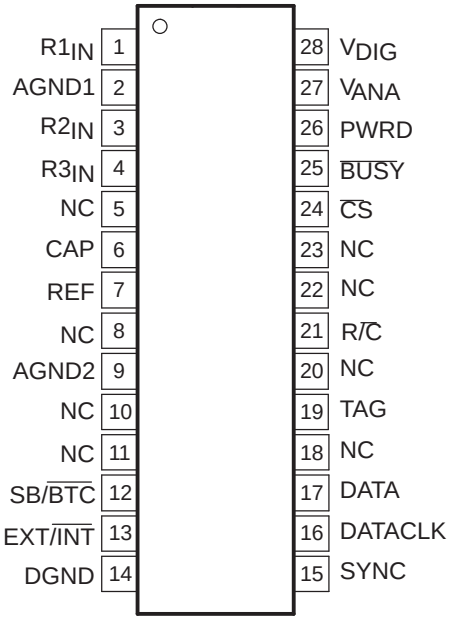
At T_A = –40°C to +85°C, f_S = 250kSPS, and V_{DIG} = V_{ANA} = 5V, using internal reference (unless otherwise specified).

PARAMETER		TEST CONDITIONS	ADS8519I			ADS8519IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
	Logic levels								
V_{IL}	Low-level input voltage(9)	V_{DIG} = 1.65V to 5.25V	–0.3		0.6	–0.3		0.6	V
V_{IH}	High-level input voltage(9)	V_{DIG} = 1.65V to 5.25V	0.5 x V_{DIG}		V_{DIG} + 0.3	0.5 x V_{DIG}		V_{DIG} + 0.3	V
I_{IL}	Low-level input current	V_{IL} = 0V			±10			±10	µA
I_{IH}	High-level input current	V_{IH} = 5V			±10			±10	µA
DIGITAL OUTPUTS									
	Data format		Serial, 16-bits			Serial, 16-bits			
	Data coding		Binary 2's complement or straight binary			Binary 2's complement or straight binary			
	Pipeline delay		Conversion results only available after completed conversion			Conversion results only available after completed conversion			
	Data clock		Selectable for internal or external data clock			Selectable for internal or external data clock			
	Internal clock (output only when transmitting data)	EXT/$\overline{INT}$ low		9			9		MHz
	External clock (can run continually but not recommended for optimum performance)	EXT/$\overline{INT}$ high	0.1		26	0.1		26	MHz
V_{OL}	Low-level output voltage	I_{SINK} = 1.6mA, V_{DIG} = 1.65V to 5.25V			0.45			0.45	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500µA, V_{DIG} = 1.65V to 5.25V	V_{DIG} – 0.45			V_{DIG} – 0.45			V
	Leakage current	Hi-Z state, V_{OUT} = 0V to V_{DIG}			±5			±5	µA
	Output capacitance	Hi-Z state			15			15	pF
POWER SUPPLIES									
V_{DIG}	Digital input voltage	Must be ≤ V_{ANA}	1.65		5.25	1.65		5.25	V
V_{ANA}	Analog input voltage	Must be ≤ V_{ANA}	4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital input current	Must be ≤ V_{ANA}		0.1	1		0.1	1	mA
I_{ANA}	Analog input current	Must be ≤ V_{ANA}		22	25		22	25	mA
POWER DISSIPATION									
	PWRD Low	f_S = 250kSPS		110	125		110	125	mW
	PWRD High			20			20		µW
TEMPERATURE RANGE									
	Specified performance		–40		+85	–40		+85	°C
	Derated performance(10)		–55		+125	–55		+125	°C
	Storage		–65		+150	–65		+150	°C
θ_{JA}	Thermal resistance			67			67		°C/W

(9) TTL-compatible at 5V supply.
(10) The internal reference may not be started correctly beyond the industrial temperature range (–40°C to +85°C); therefore, use of an external reference is recommended.

PIN CONFIGURATION

DB PACKAGE
(TOP VIEW)



Pin Assignments

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND1	2	–	Analog ground. Used internally as ground reference point. Minimal current flow.
AGND2	9	–	Analog ground
$\overline{BUSY}$	25	O	Busy output. Falls when a conversion is started, and remains low until the conversion is completed and the data are latched into the output shift register.
$\overline{CS}$	24	–	Chip select. Internally ORed with R/$\overline{C}$.
CAP	6		Reference buffer capacitor, 2.2μF tantalum capacitor to ground.
DATA	17	O	Serial data output. Data are synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADS8519 outputs the level input on TAG as long as $\overline{CS}$ is low and R/$\overline{C}$ is high (see Figure 8 and Figure 9). If EXT/$\overline{INT}$ is low, data are valid on both the rising and falling edges of DATACLK, and between conversions DATA stays at the level of the TAG input when the conversion was started.
DATACLK	16	I/O	Either an input or an output, depending on the EXT/$\overline{INT}$ level. Output data are synchronized to this clock. If EXT/$\overline{INT}$ is low, DATACLK transmits 16 pulses after each conversion, and then remains low between conversions.
DGND	14	–	Digital ground
EXT/$\overline{INT}$	13	–	Selects external or internal clock for transmitting data. If high, data are output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
NC	5, 8, 10, 11, 18, 20, 22, 23	–	Not connected
PWRD	26	I	Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
R/$\overline{C}$	21	I	Read/convert input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is low, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is high, a rising edge on R/$\overline{C}$ with $\overline{CS}$ low, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ high, initiates the transmission of data from the previous conversion.
REF	7	I/O	Reference input/output. Outputs internal 4.096V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF tantalum capacitor.
$R1_{IN}$	1	I	Analog input. See Table 2 for input range connections.
$R2_{IN}$	3	I	Analog input. See Table 2 for input range connections.
$R3_{IN}$	4	I	Analog input. See Table 2 for input range connections.
SB/$\overline{BTC}$	12	I	Select straight binary or binary two's complement data output format. If high, data are output in a straight binary format. If low, data are output in a binary two's complement format.
SYNC	15	O	Sync output. This pin is used to supply a data synchronization pulse when the EXT level is high and at least one external clock pulse has occurred when not in the read mode. See the *External DATACLK* section for the external clock mode description.
TAG	19	I	Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that depends on the external clock mode. See Figure 8 and Figure 9.
V_{ANA}	27	I	Analog supply input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
V_{DIG}	28	I	Digital supply input. Connect directly to pin 19.

TIMING REQUIREMENTS, T_A = –40°C to +85°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, convert	40			ns
t_{d1}	Delay time, $\overline{BUSY}$ from R/$\overline{C}$ low		6	20	ns
t_{w2}	Pulse duration, $\overline{BUSY}$ low			2.2	µs
t_{d2}	Delay time, $\overline{BUSY}$, after end of conversion		5		ns
t_{d3}	Delay time, aperture		5		ns
t_{conv}	Conversion time			2.2	µs
t_{acq}	Acquisition time	1.8			µs
$t_{conv} + t_{acq}$	Cycle time			4	µs
t_{d4}	Delay time, R/$\overline{C}$ Low to internal DATACLK output		270		ns
t_{c1}	Cycle time, internal DATACLK		110		ns
t_{d5}	Delay time, data valid to internal DATACLK high	15	35		ns
t_{d6}	Delay time, data valid after internal DATACLK low	20	35		ns
t_{c2}	Cycle time, external DATACLK	35			ns
t_{w3}	Pulse duration, external DATACLK high	15			ns
t_{w4}	Pulse duration, external DATACLK low	15			ns
t_{su1}	Setup time, R/$\overline{C}$ rise/fall to external DATACLK high	15			ns
t_{su2}	Setup time, R/$\overline{C}$ transition to $\overline{CS}$ transition	10			ns
t_{d7}	Delay time, SYNC, after external DATACLK high	3		35	ns
t_{d8}	Delay time, data valid from external DATACLK high	2		13	ns
t_{d9}	Delay time, $\overline{CS}$ rising edge to external DATACLK rising edge	10			ns
t_{d10}	Delay time, previous data available after $\overline{CS}$, R/$\overline{C}$ low	2			µs
t_{su3}	Setup time, $\overline{BUSY}$ transition to first external DATACLK	5			ns
t_{d11}	Delay time, final external DATACLK to $\overline{BUSY}$ rising edge			1	µs
t_{su4}	Setup time, TAG valid	0			ns
t_{h1}	Hold time, TAG valid	2			ns

TIMING DIAGRAMS

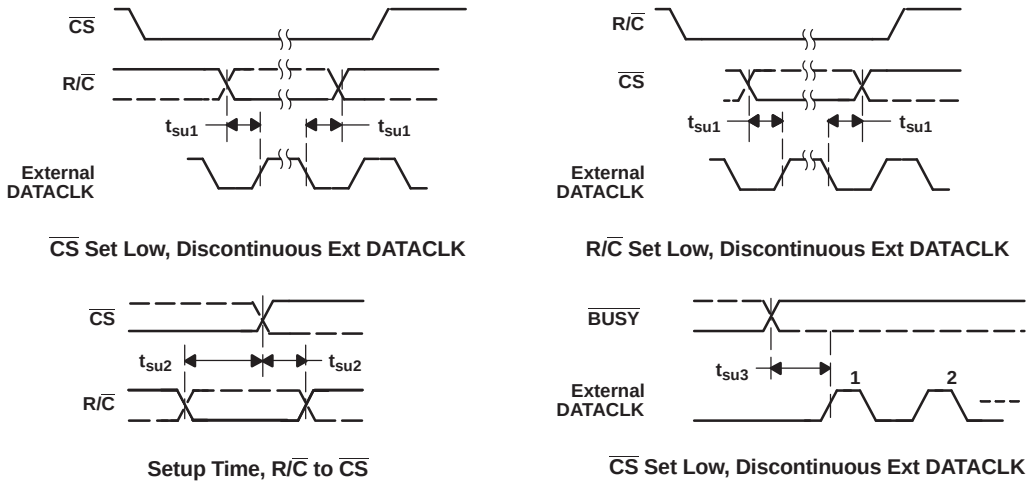


Figure 1. Critical Timing

TIMING DIAGRAMS (continued)

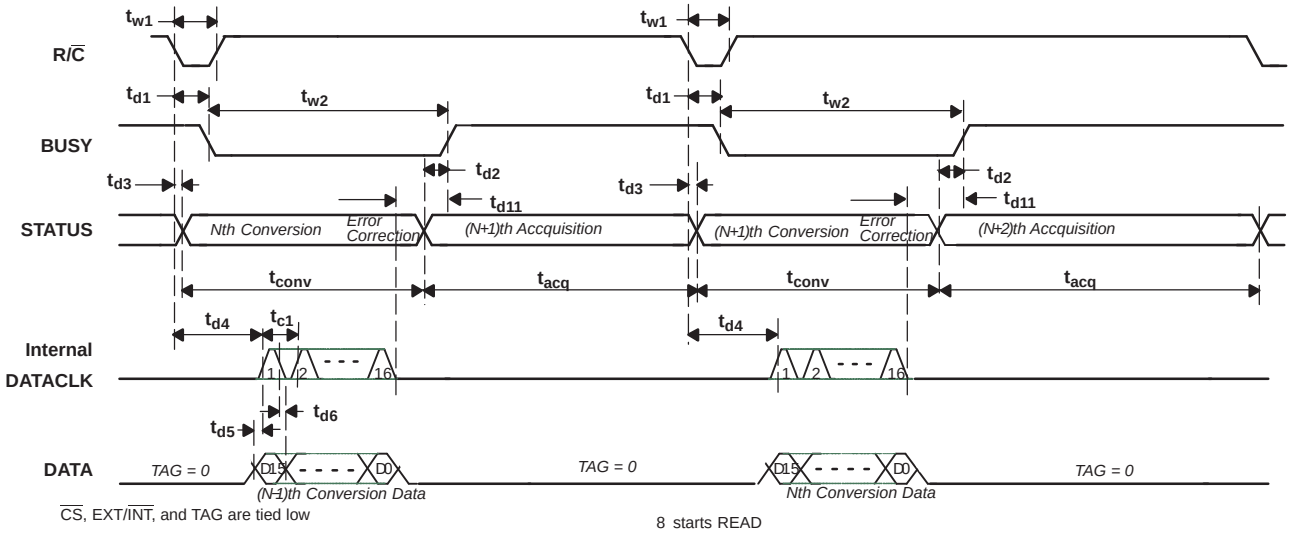


Figure 2. Basic Conversion Timing: Internal DATACLK (Read Previous Data During Conversion)

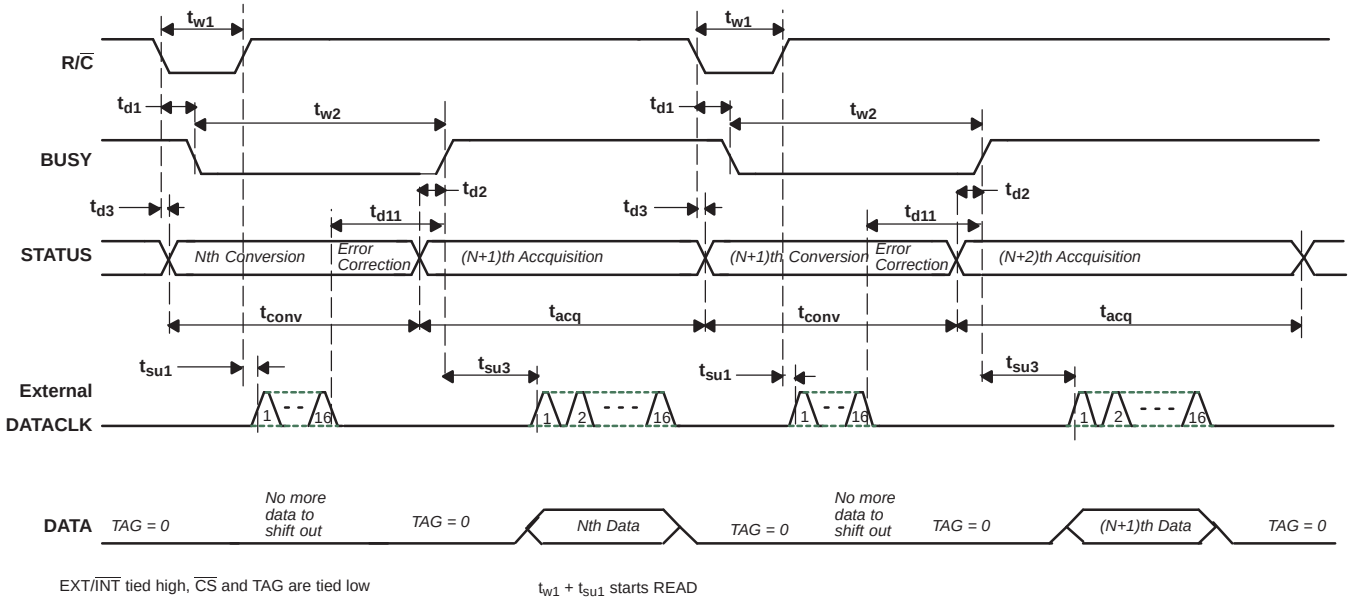


Figure 3. Basic Conversion Timing: External DATACLK

TIMING DIAGRAMS (continued)

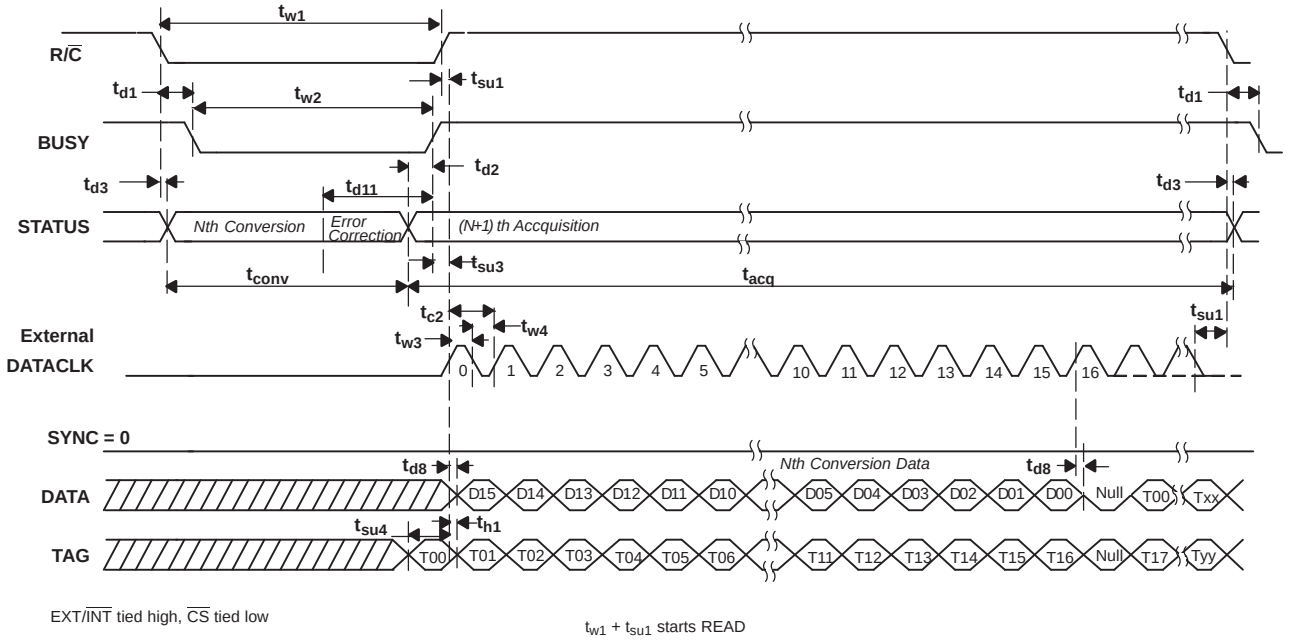


Figure 4. Read After Conversion (Discontinuous External DATACLK)

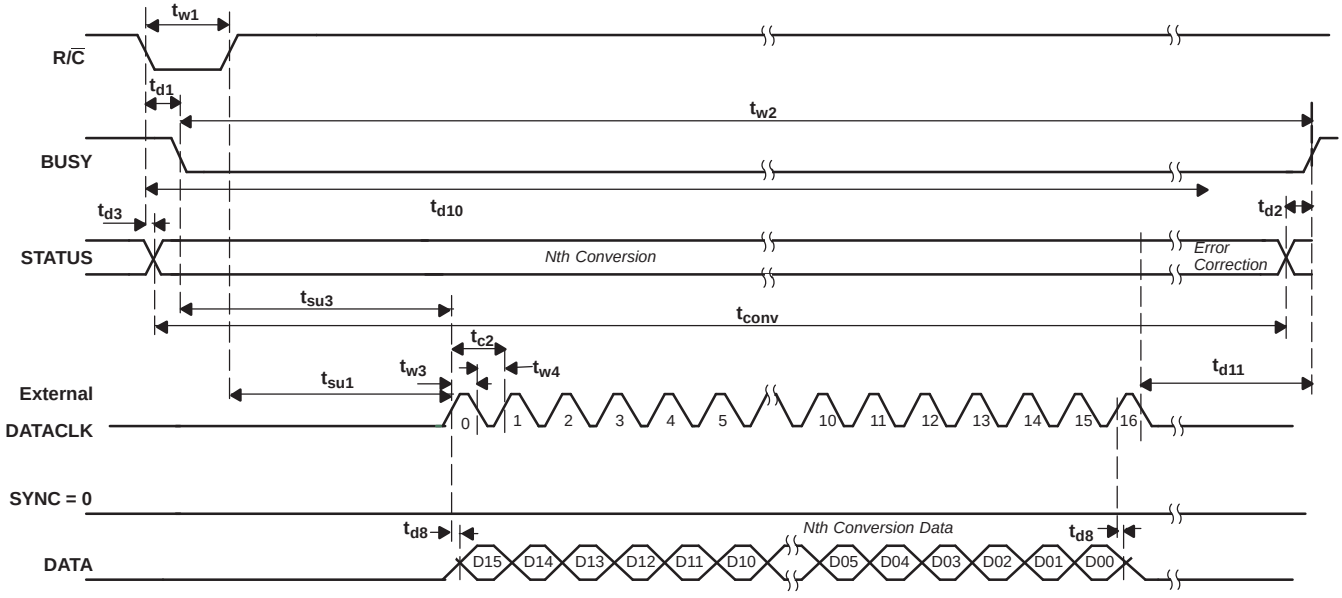
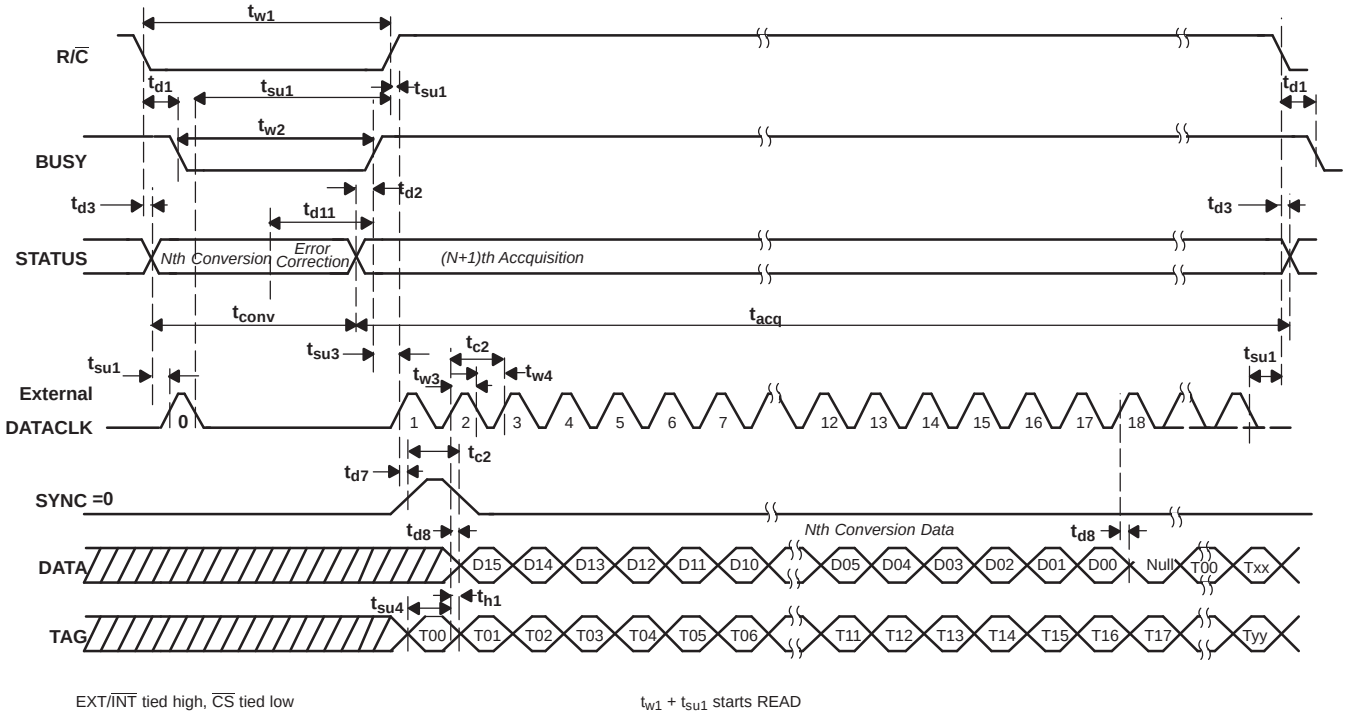


Figure 5. Read During Conversion (Discontinuous External DATACLK)

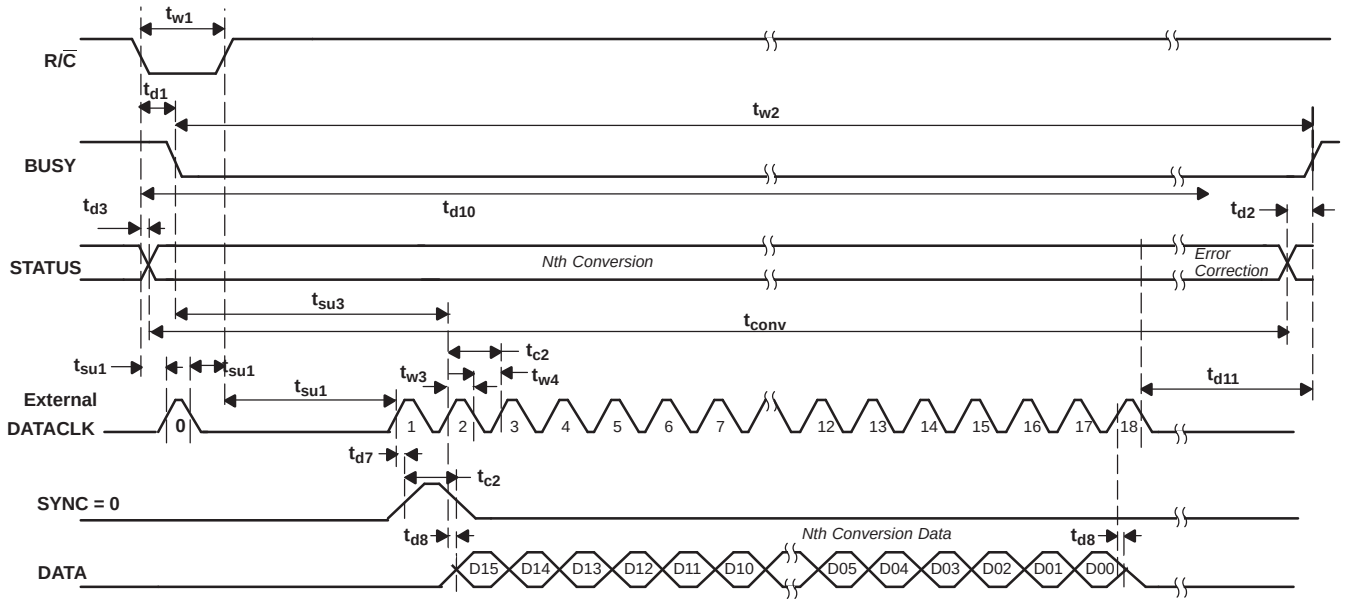
TIMING DIAGRAMS (continued)



EXT/$\overline{INT}$ tied high, $\overline{CS}$ tied low

t_{w1} + t_{su1} starts READ

Figure 6. Read After Conversion With SYNC (Discontinuous External DATACLK)



EXT/$\overline{INT}$ tied high, $\overline{CS}$ and TAG tied low

t_{w1} + t_{su1} Starts READ
TAG is not recommended for this mode. There is not enough time to do so without violating t_{d11}.

Figure 7. Read During Conversion With SYNC (Discontinuous External DATACLK)

TIMING DIAGRAMS (continued)

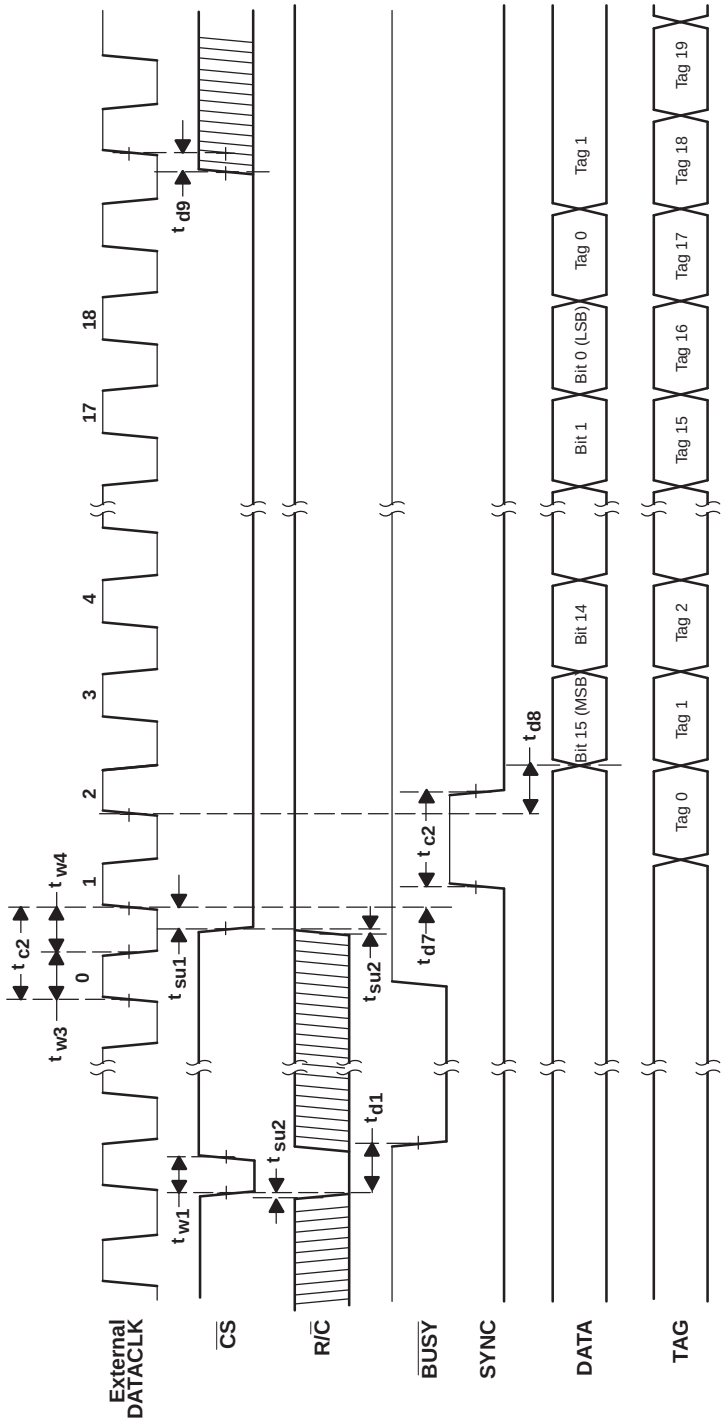


Figure 8. Conversion and Read Timing with Continuous External DATACLK (EXT/$\overline{INT}$ Tied High) Read After Conversions (Not Recommended)

TIMING DIAGRAMS (continued)

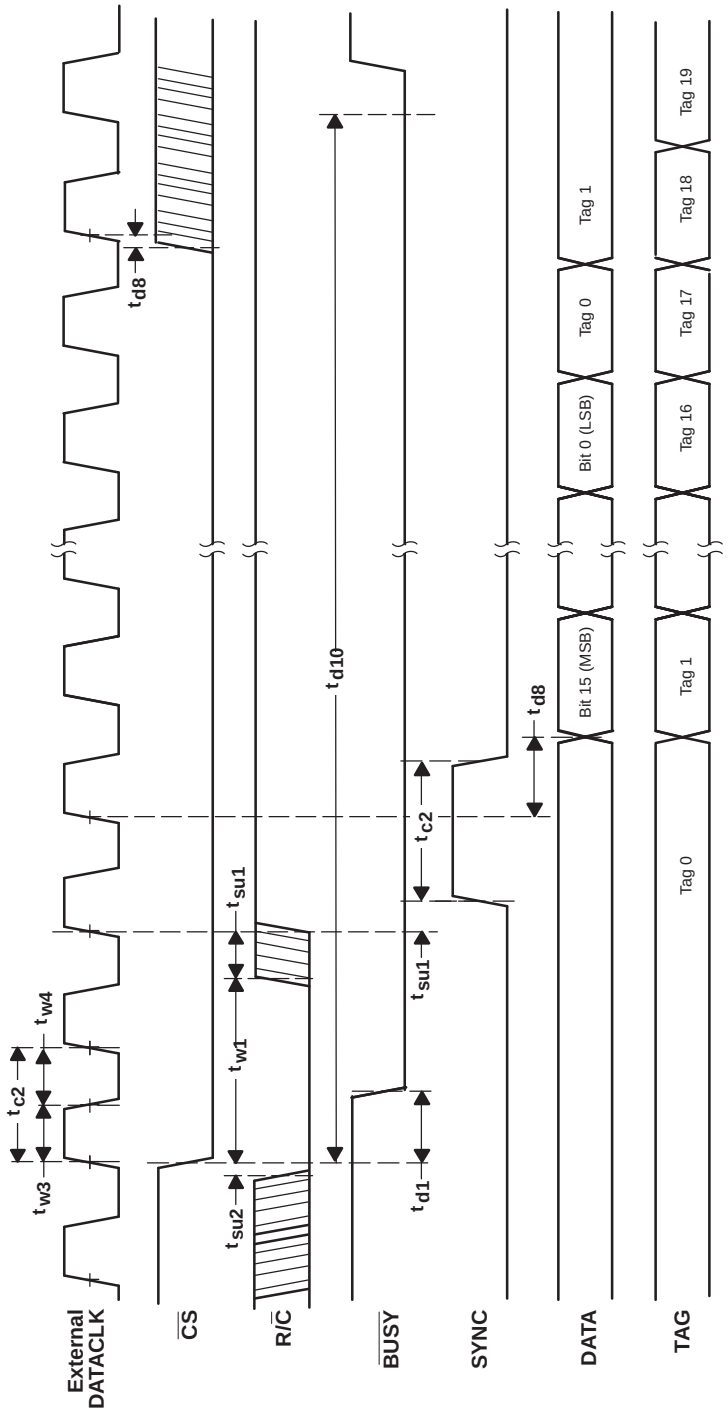


Figure 9. Conversion and Read Timing with Continuous External DATACLK (EXT/$\overline{INT}$ Tied High) Read Previous Conversion Results During Conversion (Not Recommended)

TYPICAL CHARACTERISTICS

HISTOGRAM

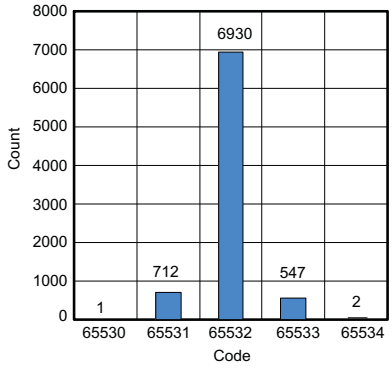


Figure 10.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

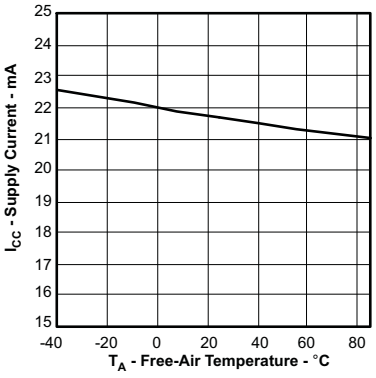


Figure 11.

INTERNAL VOLTAGE REFERENCE vs FREE-AIR TEMPERATURE

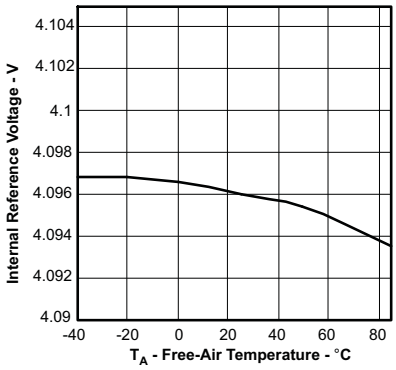


Figure 12.

BIPOLAR ZERO ERROR vs FREE-AIR TEMPERATURE

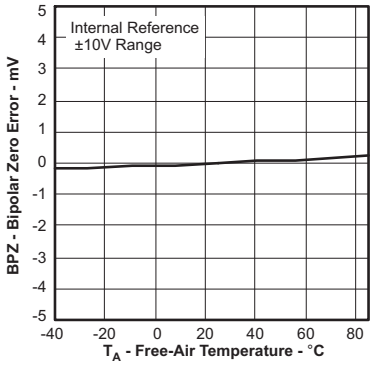


Figure 13.

POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

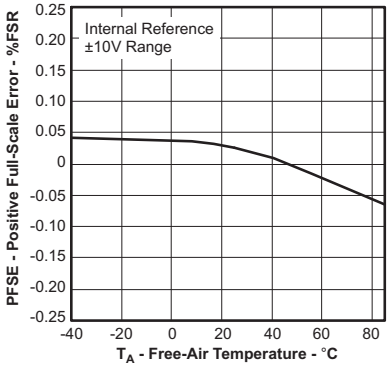


Figure 14.

NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

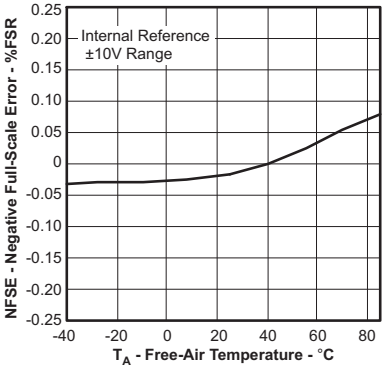


Figure 15.

POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

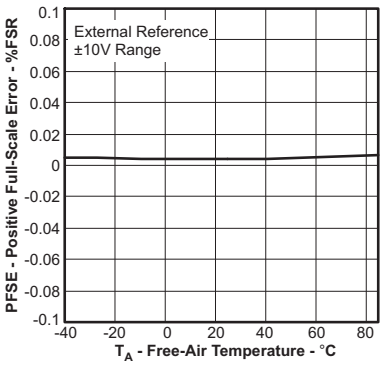


Figure 16.

NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

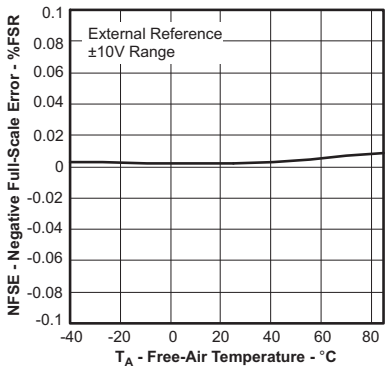


Figure 17.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

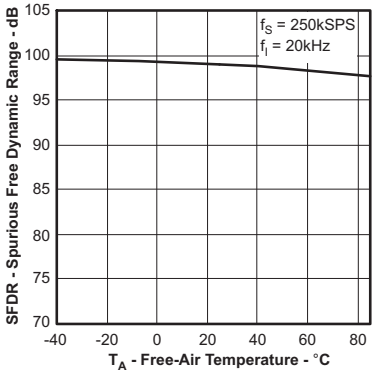


Figure 18.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

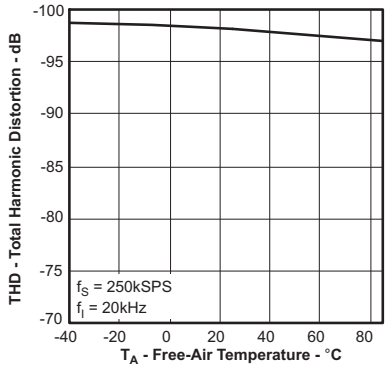


Figure 19.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

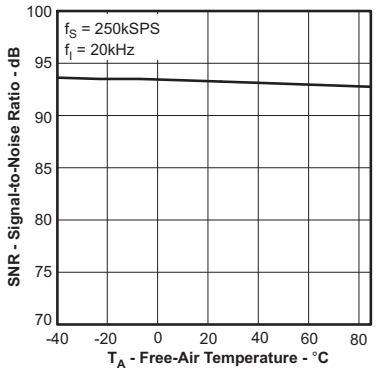


Figure 20.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

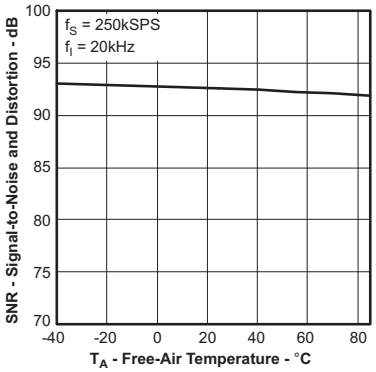


Figure 21.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

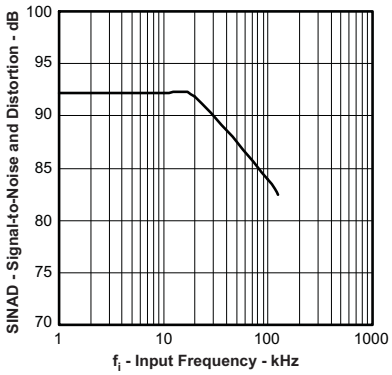


Figure 22.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

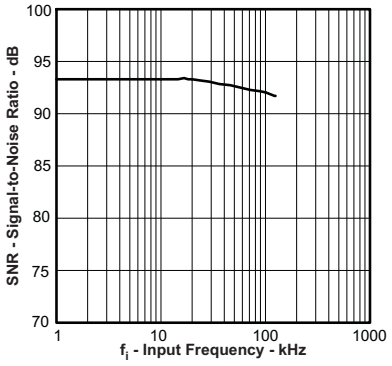


Figure 23.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

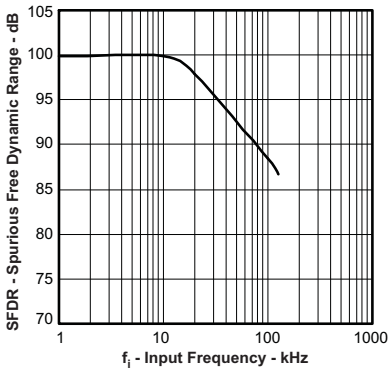


Figure 24.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

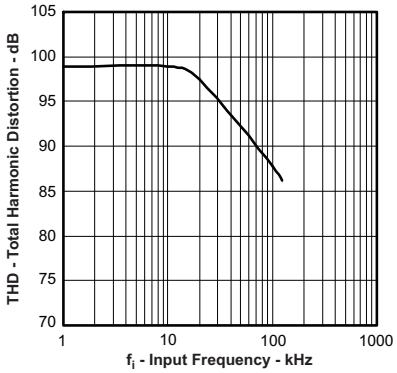


Figure 25.

TYPICAL CHARACTERISTICS (continued)

INL

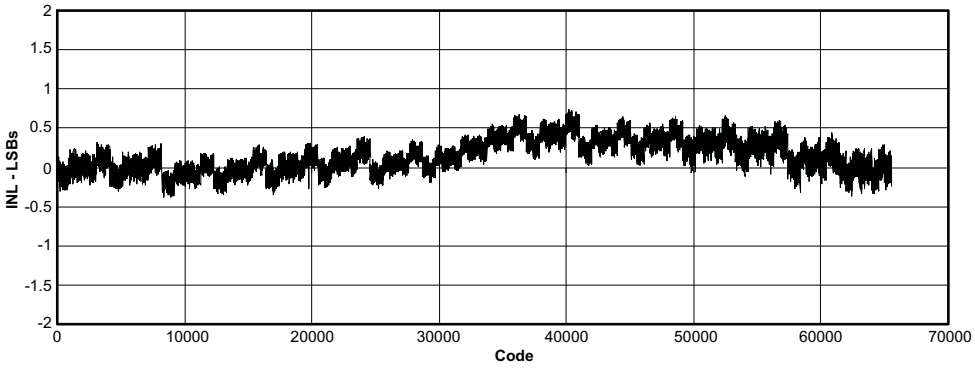


Figure 26.

DNL

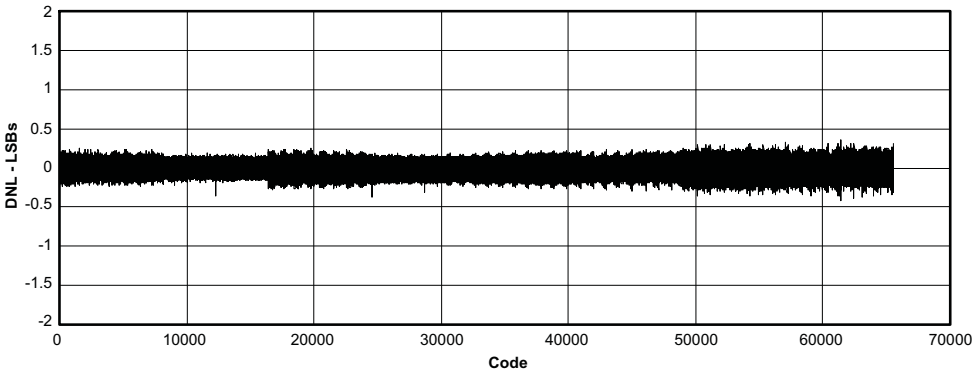


Figure 27.

BASIC OPERATION

Two signals control conversion in the ADS8519: $\overline{CS}$ and R/$\overline{C}$. These two signals are internally ORed together. To start a conversion, the chip must be selected ($\overline{CS}$ low) and the conversion signal must be active (R/$\overline{C}$ low). Either signal can be brought low first. Conversion starts on the falling edge of the second signal. $\overline{BUSY}$ goes low when conversion starts and returns high after the data from that conversion are shifted into the internal storage register. Sampling begins when $\overline{BUSY}$ goes high.

To reduce the number of control pins, $\overline{CS}$ can be tied low permanently. The R/$\overline{C}$ pin then controls conversion and data reading exclusively. In the external clock mode, this configuration means that the ADS8519 clocks out data whenever R/$\overline{C}$ is brought high and the external clock is active. In the internal clock mode, data are clocked out every convert cycle, regardless of the states of $\overline{CS}$ and R/$\overline{C}$. The ADS8519 provides a TAG input for cascading multiple converters together.

READING DATA

The conversion result is available as soon as BUSY returns to high; therefore, data always represent the conversion previously completed, even when it is read during a conversion. The ADS8519 outputs serial data in either straight binary or binary two's complement format. The SB/$\overline{BTC}$ pin controls the format. data are shifted out MSB first. The first conversion immediately following a power-up does not produce a valid conversion result.

Data can be clocked out with either the internally-generated clock or with an external clock. The EXT/$\overline{INT}$ pin controls this function. If an external clock is used, the TAG input can be used to daisy-chain multiple ADS8519 data pins together.

INTERNAL DATACLK

In the internal clock mode, data for the previous conversion are clocked out during each conversion period. The internal data clock is synchronized to the internal conversion clock so that it does not interfere with the conversion process.

The DATACLK pin becomes an output when EXT/$\overline{INT}$ is low. 16 clock pulses are generated at the beginning of each conversion after timing t_{d4} is satisfied (that is, previous conversion results can only be read during the current conversion). DATACLK returns to low when it is inactive. The 16 bits of serial data are shifted out of the DATA pin synchronous to this clock, with each bit available on a rising and then a falling edge. The DATA pin then returns to the state of the TAG pin input sensed at the start of transmission.

EXTERNAL DATACLK

The external clock mode offers several ways to retrieve conversion results. However, care must be taken to avoid corrupting the data because the external clock cannot be synchronized to the internal conversion clock.

When EXT/$\overline{INT}$ is set high, the R/$\overline{C}$ and $\overline{CS}$ signals control the read state. When the read state is initiated, the result from the previously completed conversion is shifted out of the DATA pin synchronous to the external clock that is connected to the DATACLK pin. Each bit is available on a falling and then a rising edge. The maximum external clock speed of 28.5MHz allows data to be shifted out quickly either at the beginning of conversion or the beginning of sampling.

There are several modes of operation available when using an external clock. It is recommended that the external clock run only while reading data. This mode is the discontinuous clock mode. Because the external clock is not synchronized to the internal clock that controls conversion, slight changes in the external clock can cause conflicts that can corrupt the conversion process. Specifications with a continuously running external clock cannot be ensured. It is especially important that the external clock does not run during the second half of the conversion cycle (approximately the time period specified by t_{d11}; see the *Timing Requirements* table).

In the discontinuous clock mode, data can be read during conversion or during sampling, with or without a SYNC pulse. Data read during a conversion must meet the t_{d11} timing specification. Data read during sampling must be complete before starting a conversion.

Whether reading during sampling or during conversion, a SYNC pulse is generated whenever at least one rising edge of the external clock occurs while the device is not in the read state. In the *Discontinuous External Clock with SYNC* mode, a SYNC pulse follows the first rising edge after the read command. Data are shifted out after the SYNC pulse. The first rising clock edge after the read command generates a SYNC pulse. The SYNC pulse can be detected on the next falling edge and then the next rising edge. Successively, each bit can be read first on the falling edge and then on the next rising edge. Thus, 17 clock pulses after the read command are required to read on the falling edge; 18 clock pulses are necessary to read on the rising edge.

If the clock is entirely inactive when not in the read state, no SYNC pulse is generated. In this case, the first rising clock edge shifts out the MSB. The MSB can be read on the first falling edge or on the next rising edge. In this *Discontinuous External Clock with No SYNC* mode, 16 clocks are necessary to read the data on the falling edge and 17 clocks for reading on the rising edge. Data always represent the conversion already completed. Table 1 summarizes the required DATACLK pulses.

Table 1. DATACLK Pulses

DESCRIPTION	DATACLK PULSES REQUIRED	
	WITH SYNC	WITHOUT SYNC
Read on falling edge of DATACLK	17	16
Read on rising edge of DATACLK	18	17

TAG FEATURE

The TAG feature allows the data from multiple ADS8519 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs, as illustrated in Figure 28. The DATA pin of the last converter drives the processor serial data input. Data are then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous, external data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see External DATACLK section). The sampling period must be sufficiently long to allow all data words to be read before starting a new conversion.

In Figure 28, note that a null bit separates the data word from each converter. The state of the DATA pin at the end of a read cycle reflects the state of the TAG pin at the start of the cycle. This condition is true in all read modes, including the internal clock mode. For example, when a single converter is used in the internal clock mode, the state of the TAG pin determines the state of the DATA pin after all 16 bits have shifted out. When multiple converters are cascaded together, this state forms the null bit that separates the words. Thus, with the TAG pin of the first converter grounded as shown in Figure 28, the null bit becomes a zero between each data word.

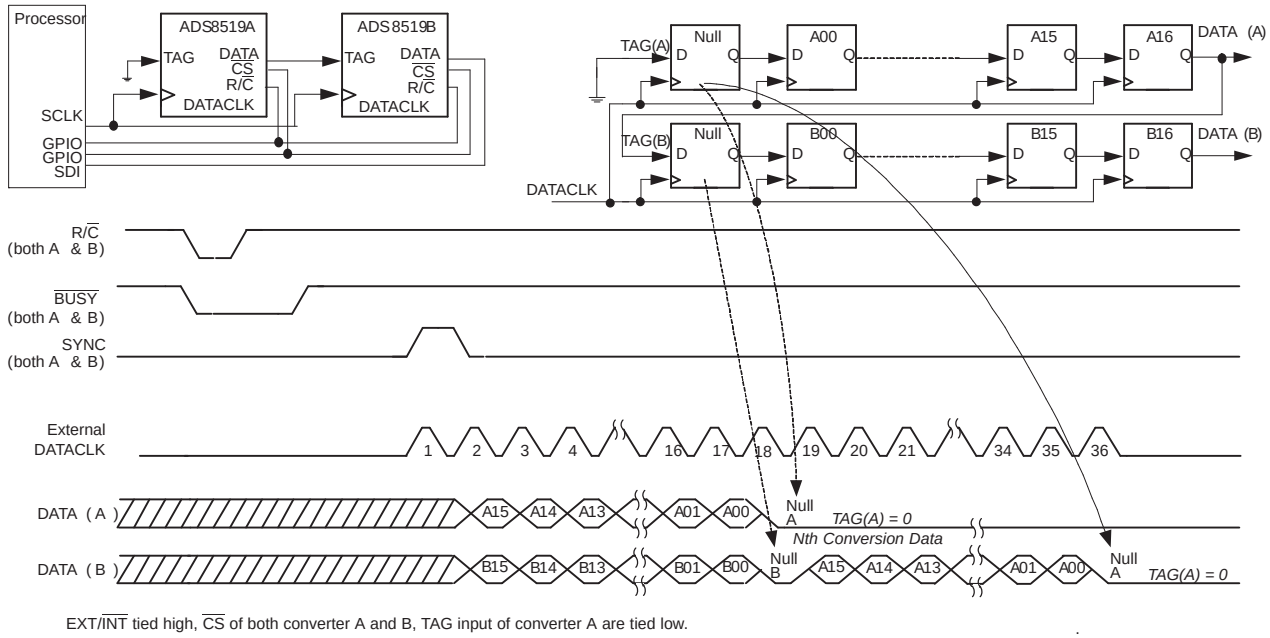


Figure 28. Timing of TAG Feature With Single Conversion (Using External DATACLK)

ANALOG INPUTS

The ADS8519 has three analog input ranges, as shown in Table 2. The offset specification is factory-calibrated with internal resistors. The gain specification is factory-calibrated with 0.1%, 0.25W, external resistors, as shown in Figure 29 and Figure 30. The external resistors can be omitted if a larger gain error is acceptable or if using software calibration. The hardware trim circuitry shown in Figure 29 and Figure 30 can reduce the error to zero.

Table 2. Input Range Connections
(see Figure 29 and Figure 30 for complete information)

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	8.88kΩ
±10V	AGND	V_{IN}	CAP	8.88kΩ
±5V	V_{IN}	V_{IN}	CAP	6.08kΩ
0V to 8.192V	AGND	AGND	V_{IN}	5.95kΩ

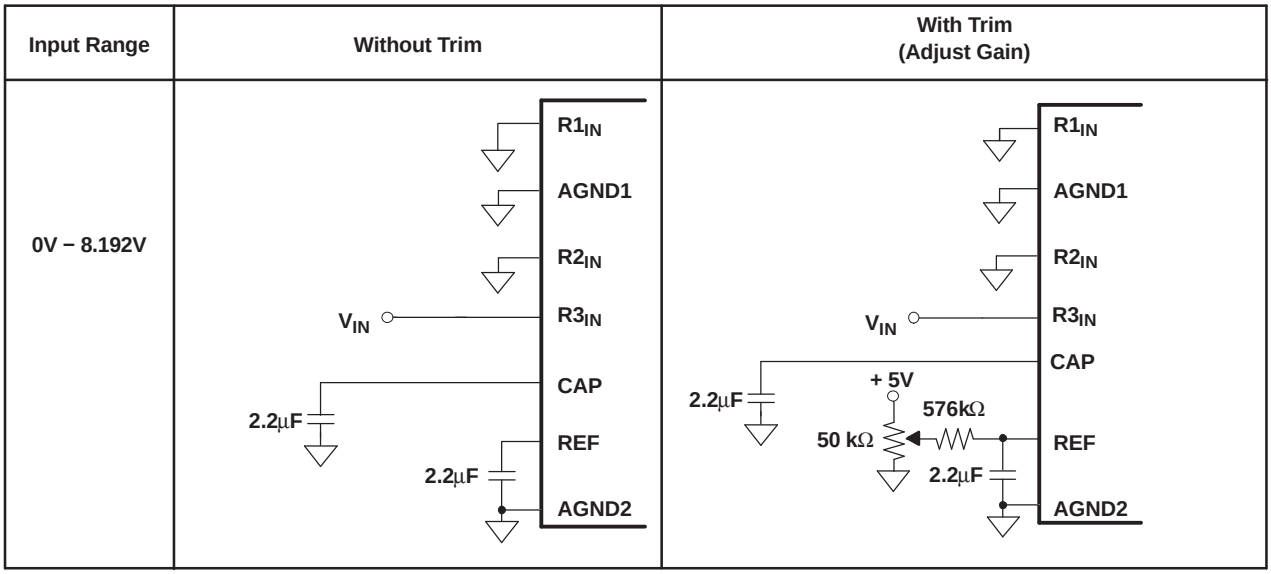


Figure 29. Offset/Gain Circuits for Unipolar Input Ranges

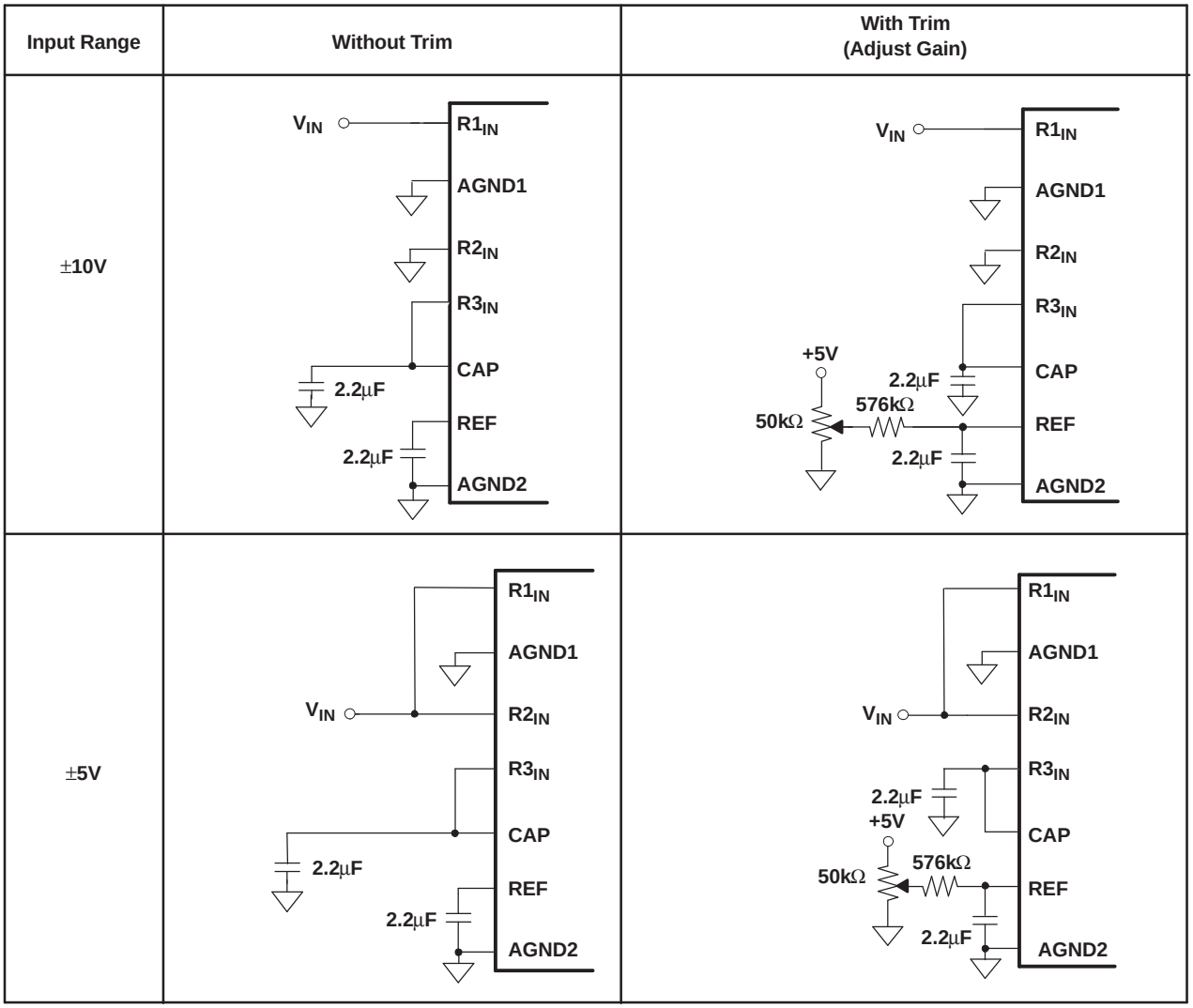


Figure 30. Offset/Gain Circuits for Bipolar Input Ranges

Analog input pins $R1_{IN}$, $R2_{IN}$, and $R3_{IN}$ have ±25V overvoltage protection. The input signal must be referenced to AGND1. This referencing minimizes the ground-loop problem typical to analog designs. The analog input should be driven by a low-impedance source. A typical driving circuit using the OPA627 or OPA132 is shown in Figure 30.

The ADS8519 can operate with its internal 4.096V reference or an external reference. An external reference connected to pin 7 (REF) bypasses the internal reference. The external reference must drive the 4kΩ resistor that separates pin 6 from the internal reference (see the illustration on page 1). The load varies with the difference between the internal and external reference voltages. The external reference voltage can vary from 3.9V to 4.2V. The internal reference is approximately 4.096V. The reference, whether internal or external, is buffered internally with the output on pin 6 (CAP).

The ADS8519 is factory-tested with 2.2µF capacitors connected to pin 6 (CAP) and pin 7 (REF). Each capacitor should be placed as close as possible to its pin. The capacitor on pin 7 band-limits the internal reference noise. A smaller capacitor can be used, but it may degrade SNR and SINAD The capacitor on pin 6 stabilizes the reference buffer and provides switching charge to the CDAC during conversion. Capacitors smaller than 1µF may cause the buffer to become unstable and not hold sufficient charge for the CDAC. The parts are tested to specifications with 2.2µF, so larger capacitors are not necessary. The equivalent series resistance (ESR) of these compensation capacitors is also critical. Keep the total ESR under 3Ω. See the *Typical Characteristics* section concerning how ESR affects performance.

Neither the internal reference nor the buffer should be used to drive an external load. Such loading can degrade performance. Any load on the internal reference causes a voltage drop across the 4kΩ resistor and affects gain. The internal buffer is capable of driving ±2mA loads, but any load can cause perturbations of the reference at the CDAC, degrading performance. It should be pointed out that, unlike other devices with a similar input structure, the ADS8519 does not require a second high-speed amplifier used as a buffer to isolate the CAP pin from the signal-dependent current in the $R3_{IN}$ pin, but can tolerate it if one does exist.

The external reference voltage can vary from 3.9V to 4.2V. The reference voltage determines the size of the least significant bit (LSB). The larger reference voltages produce a larger LSB, which can improve SNR. Smaller reference voltages can degrade SNR.

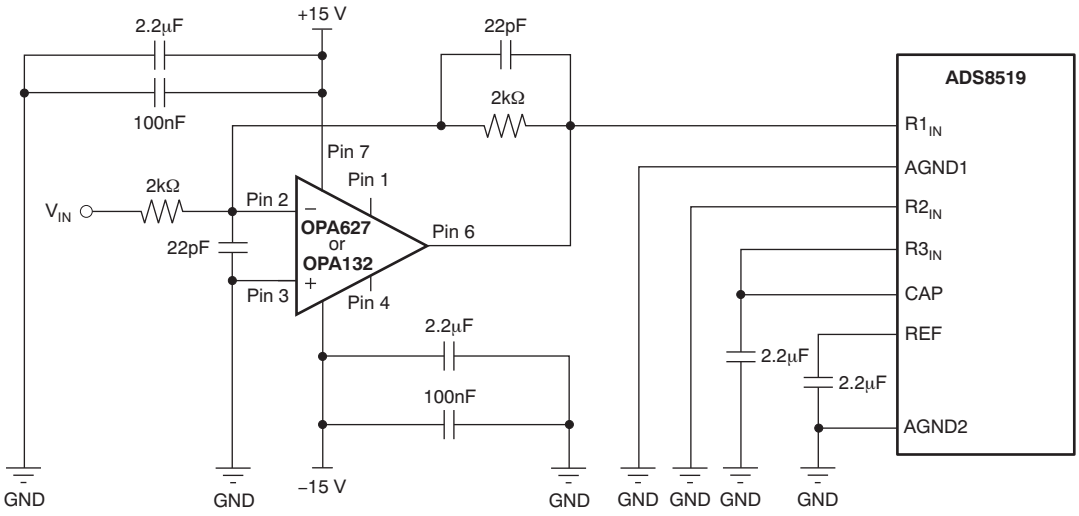


Figure 31. Typical Driving Circuitry (±10V, No Trim)

Table 3. Control Truth Table

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate conversion and output data using internal clock	1 > 0	0	1	0	Output	0	x	Initiates conversion *n*. Data from conversion *n - 1* clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	
Initiate conversion and output data using external clock	1 > 0	0	1	1	Input	0	x	Initiates conversion *n*.
	0	1 > 0	1	1	Input	0	x	Initiates conversion *n*.
	1 > 0	1	1	1	Input	x	x	Outputs data with or without SYNC pulse. See the *Reading Data* section.
	1 > 0	1	0	1	Input	0	x	Outputs data with or without SYNC pulse. See Reading Data section.
	0	0 > 1	0	1	Input	0	x	
No actions	0	0	0 > 1	x	x	0	x	This is an acceptable condition.
Power down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed..
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting output format	x	x	x	x	x	x	0	Serial data are output in binary twos complement format.
	x	x	x	x	x	x	1	Serial data are output in straight binary format.

Table 4. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT RANGE			DIGITAL OUTPUT			
Full-scale range	±10V	±5V	0V to 8.192V	BINARY TWOS COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
Least significant bit (LSB)	305μV	153μV	125μV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full-scale (FS – 1LSB)	9.999695V	4.999847V	8.191875V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	4.096V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB below midscale	–305μV	153μV	4.095975V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full scale	–10V	–5V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

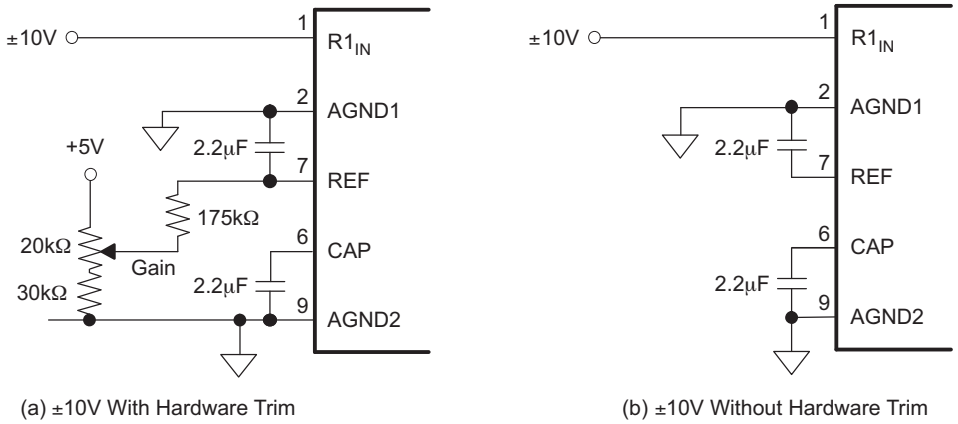


Figure 32. Gain Adjust Trim

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June, 2009) to Revision D **Page**

- Changed input/output description for SB/$\overline{\text{BTC}}$ pin (pin 12) 6

Changes from Revision B (October, 2008) to Revision C **Page**

- Changed external reference voltage range min value from 2.5V to 3.9V and max value from 4.1V to 4.2V 3
- Corrected pin names and numbers in paragraphs discussing internal and external reference operation and factory testing of device with 2.2μF capacitors. 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8519IBDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8519I B	Samples
ADS8519IBDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8519I B	Samples
ADS8519IBDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8519I B	Samples
ADS8519IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8519I	Samples
ADS8519IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8519I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

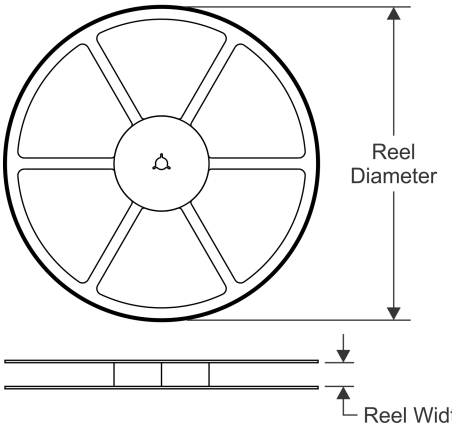
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

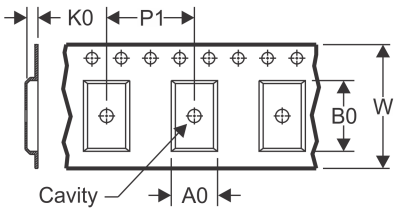
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

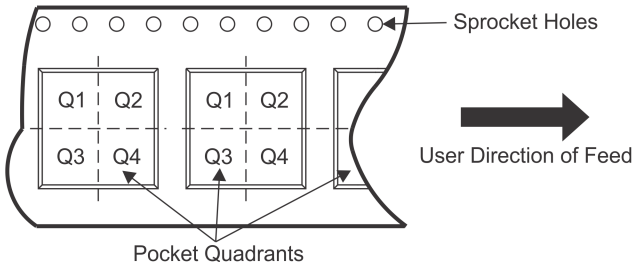


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

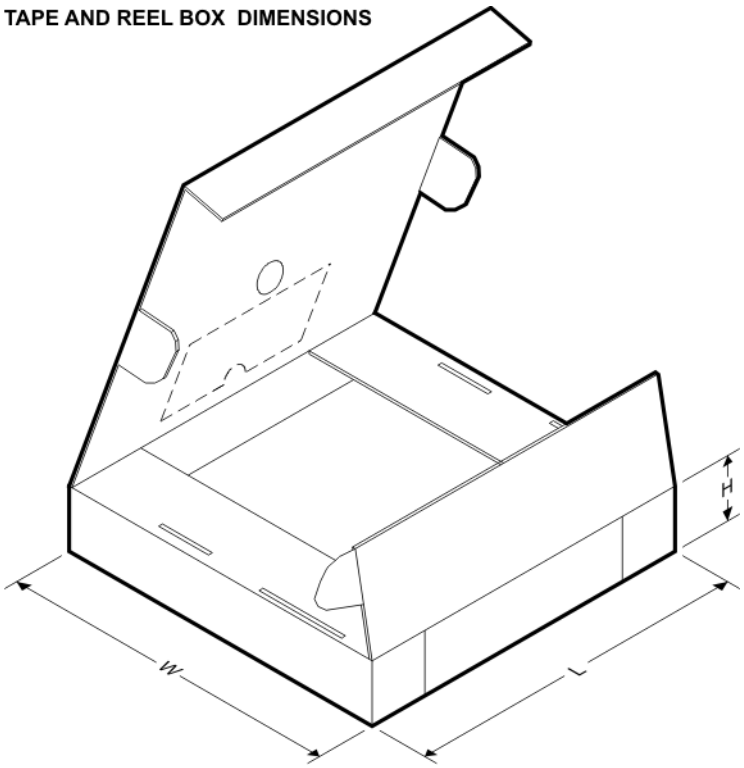
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8519IBDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
ADS8519IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

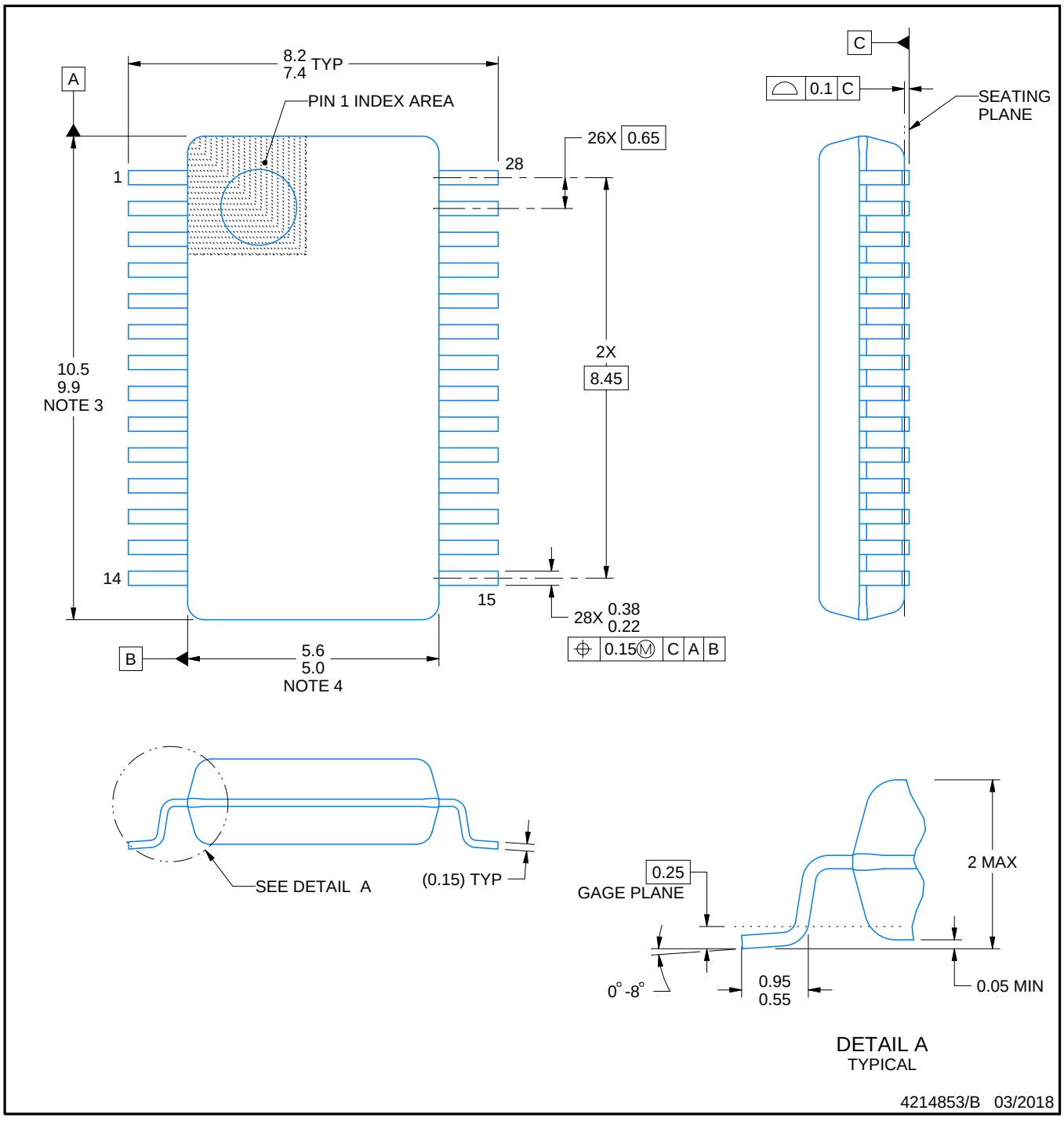
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8519IBDBR	SSOP	DB	28	2000	350.0	350.0	43.0
ADS8519IDBR	SSOP	DB	28	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DB0028A

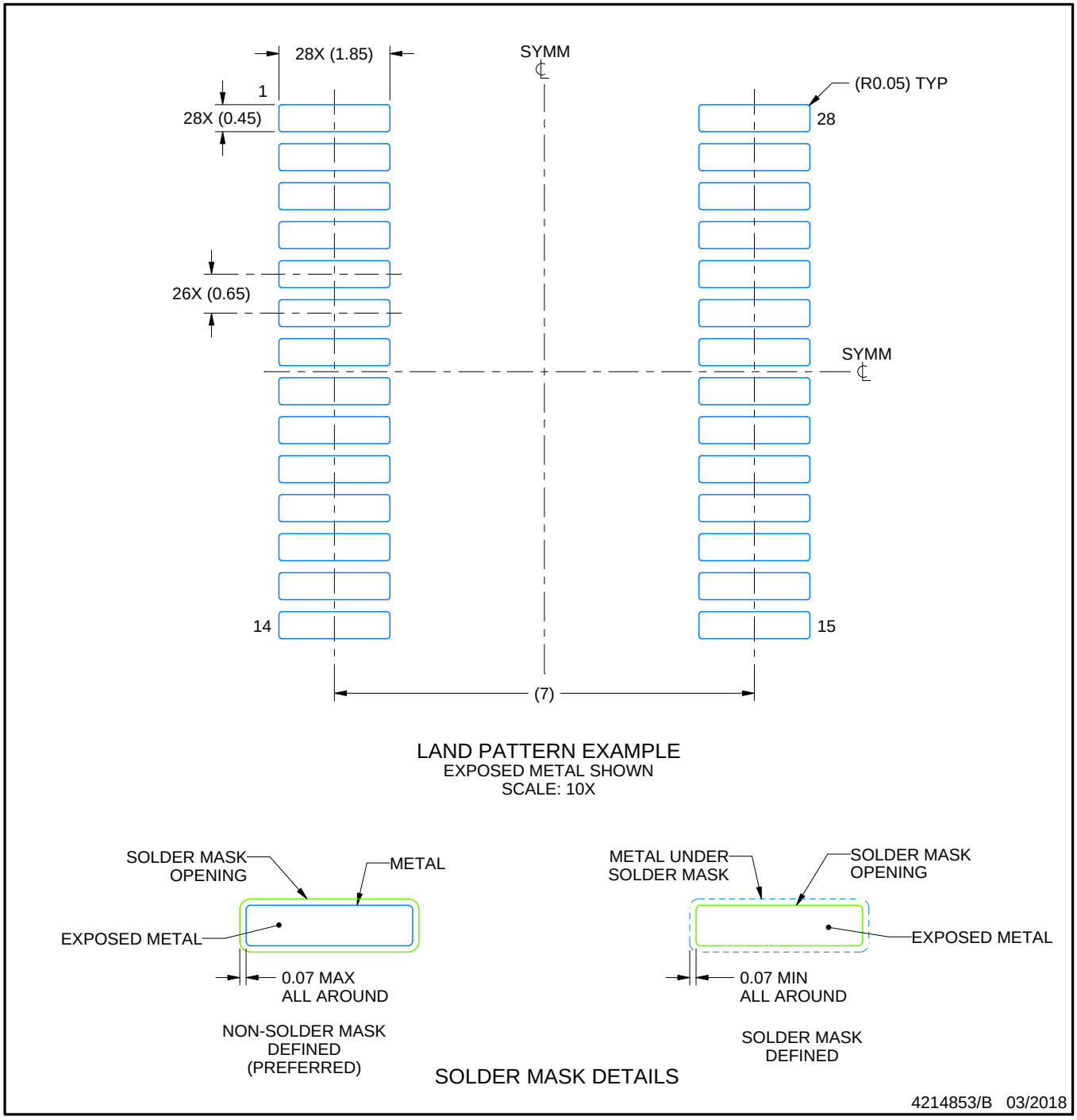
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



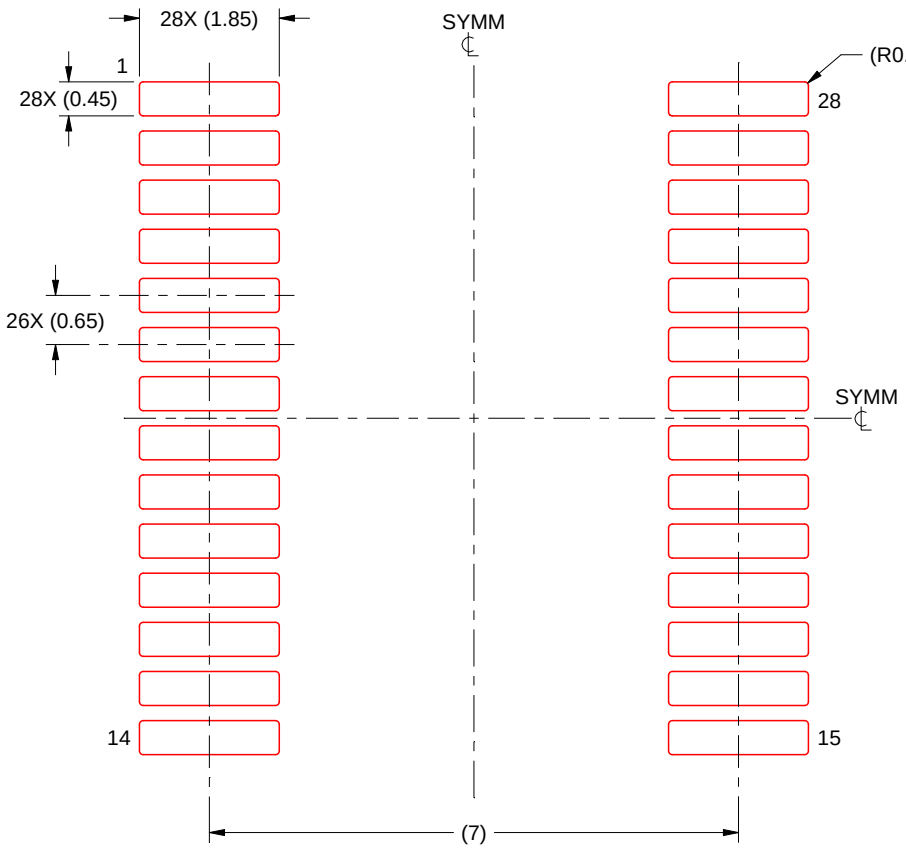
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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