High-Side and Low-Side Gate Drivers

MCP14LH2190, MCP14LH21904

Description

The MCP14LH2190 and the MCP14LH21904 are high-voltage, high-speed gate drivers capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. Microchips high voltage process enables the MCP14LH2190(4) high-side to switch to 600V in a bootstrap operation under high dV/dt conditions.

The MCP14LH2190(4) logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The MCP14LH2190 is offered in space-saving 8-pin SOIC and the MCP14LH21904 in the 14-pin SOIC and operates over an extended –40°C to +125°C temperature range.

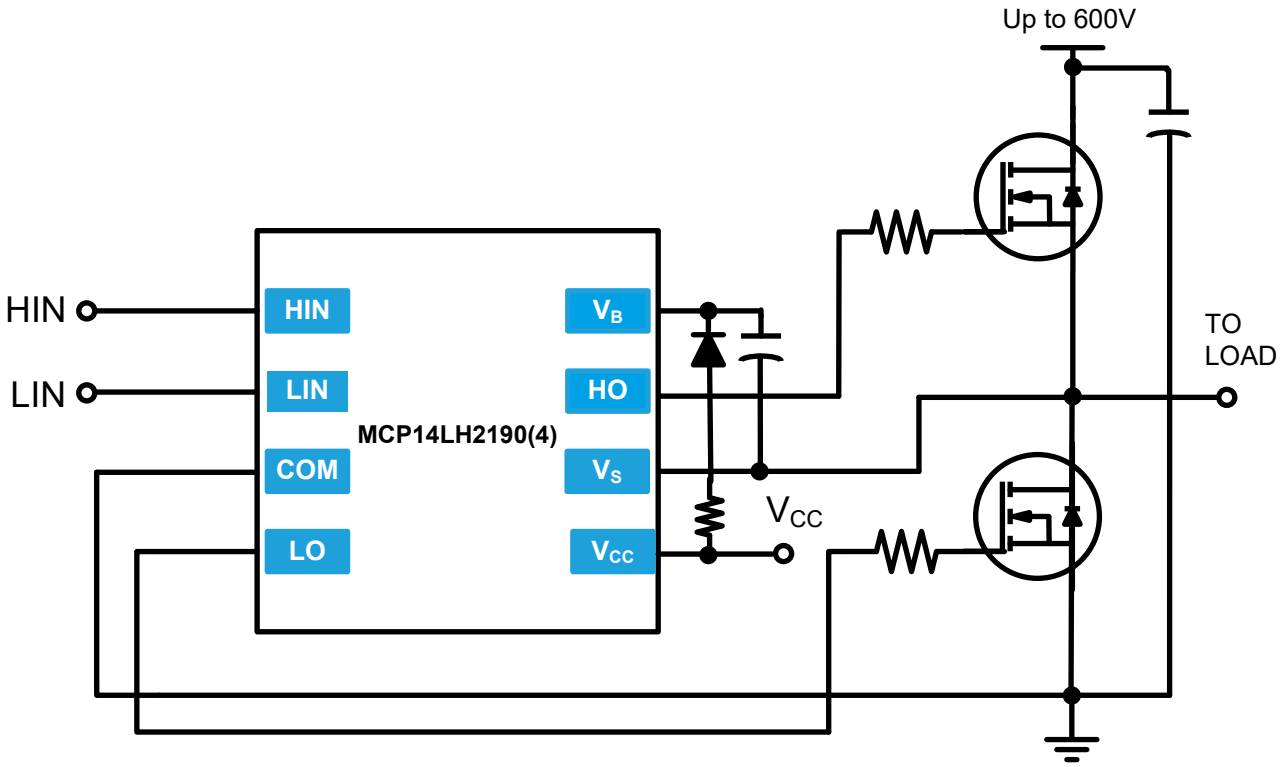
Features

- Floating High-Side Driver in Bootstrap Operation up to 600V
- Drives Two N-Channel MOSFETs or IGBTs in a Half-Bridge Configuration
- Output Drivers Capable of 4.5A/4.5A Typical Sink/Source
- Logic Input (HIN and LIN) 3.3V Capability
- Schmitt Triggered Logic Inputs With Internal Pull Down
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Extended Temperature Range: –40°C to +125°C

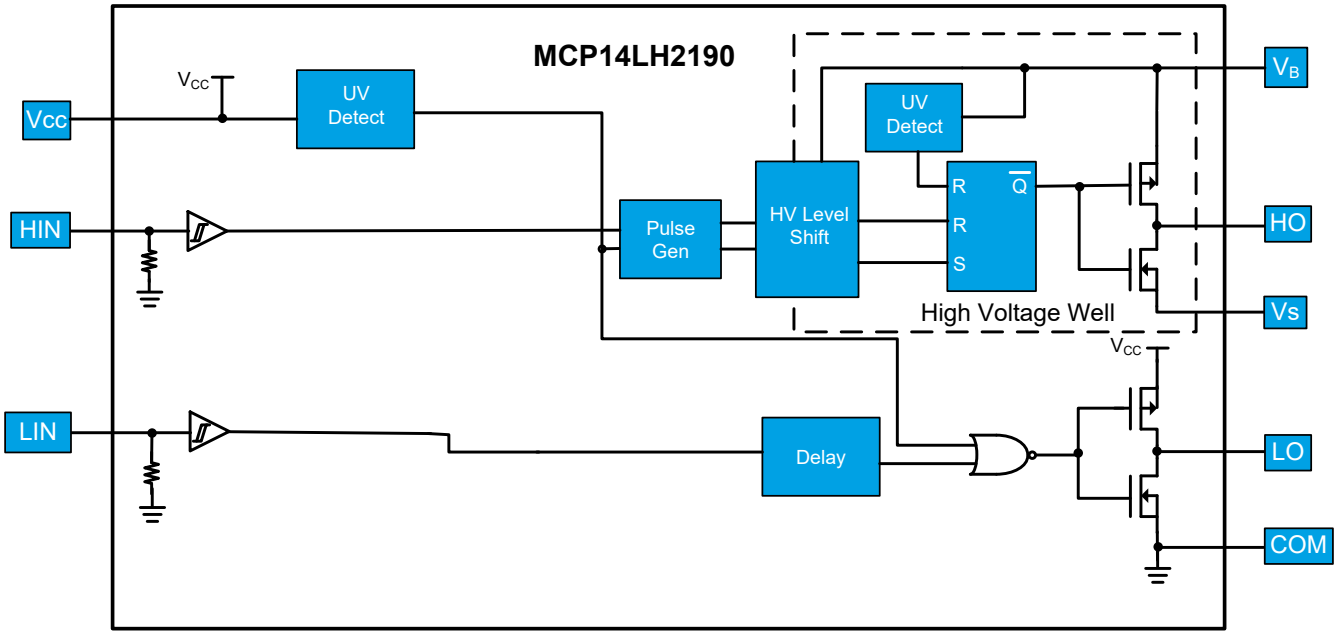
Applications

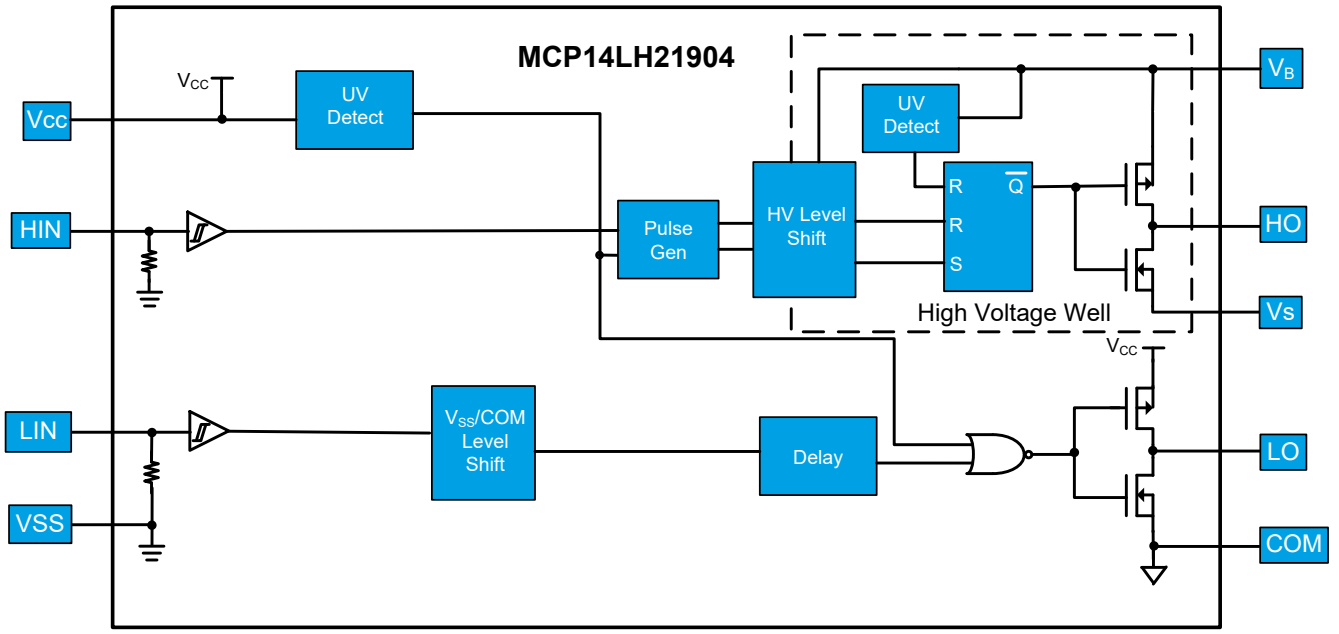
- Motor Controls
- DC-DC Converters
- AC-DC Inverters
- Class D Power Amplifiers

Typical Application



Block Diagrams





1. Pin Configuration

Pin No.	Pin Name MCP14LH2190	Pin Name MCP14LH21904	Pin Description
1	HIN	HIN	Logic input for high-side gate driver output, in phase with HO
2	LIN	LIN	Logic input for low-side gate driver output, in phase with LO
3	COM	—	Low-side and logic return
3	—	V_{SS}	Logic Ground
4	LO	—	Low-side gate drive output
4	—	NC	Not connected
5	VCC	—	Low-side and logic fixed supply
5	—	COM	Low-side and logic return
6	V_S	—	High-side floating supply return
6	—	LO	Low-side gate drive output
7	HO	—	High-side gate driver output
7	—	V_{CC}	Low-side and logic fixed supply
8	V_B	—	High-side floating supply
8, 9, 10, 14	—	NC	Not connected
11	—	V_S	High-side floating supply return
12	—	HO	High-side gate driver output
13	—	V_B	High-side floating supply

1.1. Package Types

Figure 1-1. SOIC-8 Package (MCP14LH2190 - Top View)

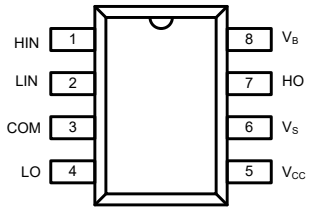
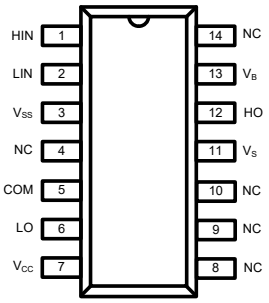


Figure 1-2. SOIC-14 Package (MCP14LH21904 - Top View)



2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
High-side Floating Supply Voltage	V_B	−0.3V	+624	V
High-side Floating Supply Offset Voltage	V_S	V_B − 24	V_B + 0.3	V
Logic Supply Offset Voltage	V_{SS}	V_{CC} − 24	V_{CC} + 0.3	V
High-side Floating Output Voltage	V_{HO}	V_S − 0.3	V_B + 0.3	V
Offset Supply Voltage Transient	dV_S/dt	—	50	V/ns
Low-side Fixed Supply Voltage	V_{CC}	−0.3V	24	V
Low-side Output Voltage	V_{LO}	−0.3V	V_{CC} + 0.3	V
Logic Input Voltage (HIN and LIN)	V_{IN}	−0.3V	V_{CC} + 0.3	V
SOIC-8 Package Power Dissipation at $T_A \leq 25°C$	P_D	—	0.625	W
SOIC-14 Package Power Dissipation at $T_A \leq 25°C$		—	0.862	W
SOIC-8 Thermal Resistance (see Note)	θ_{JA}	—	200	°C/W
	θ_{JC}	—	45	°C/W
SOIC-14 Thermal Resistance (see Note)	θ_{JA}	—	145	°C/W
Junction Operating Temperature	T_J	—	+150	°C
Lead Temperature (soldering, 10 seconds)	T_L	—	+300	°C
Storage Temperature Range	T_{STG}	−55	+150	°C

⚠ WARNING Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: When mounted on a standard JEDEC 2-layer FR-4 board.

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
High-side Floating Supply Absolute Voltage	V_B	V_S + 10	V_S + 20	V
High-side Floating Supply Offset Voltage	V_S	See Note	600	V
Logic ground (MCP14LH21904 only)	V_{SS}	−5	5	V
High-side Floating Output Voltage	V_{HO}	V_S	V_B	V
Low-side Fixed Supply Voltage	V_{CC}	10	20	V
Low-side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (HIN and LIN)	V_{IN}	0	5	V
Ambient Temperature	T_A	−40	125	°C

Note: Logic operational for V_S of −5V to +600V.

2.3. DC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25°C , unless otherwise specified.						
Parameter (Note 1)	Symbol	Min.	Typ.	Max.	Units	Conditions
Logic "1" Input Voltage	V_{IH}	2.5	—	—	V	V_{CC} = 10V to 20V (Note 2)
Logic "0" Input Voltage	V_{IL}	—	—	0.8	V	V_{CC} = 10V to 20V (Note 2)
High Level Output Voltage, V_{BIAS} – V_O	V_{OH}	—	—	0.1	V	I_O = 0 mA
Low Level Output Voltage, V_O	V_{OL}	—	—	0.035	V	I_O = 0 mA
Offset Supply Leakage Current	I_{LK}	—	—	50	µA	V_B = V_S = 600V
Quiescent V_{BS} Supply Current	I_{BSQ}	—	45	80	µA	V_{IN} = 0V or 5V
Quiescent V_{CC} Supply Current	I_{CCQ}	—	75	200	µA	V_{IN} = 0V or 5V
Logic "1" Input Bias Current	I_{IN+}	—	25	50	µA	V_{IN} = 5V
Logic "0" Input Bias Current	I_{IN-}	—	1.0	2.0	µA	V_{IN} = 0V
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.6	8.4	9.8	V	—
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	6.9	7.8	9.0	V	—
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.6	8.4	9.8	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	6.9	7.8	9.0	V	—
V_{CC} and V_{BS} Undervoltage Hysteresis	V_{CCUVH} V_{BSUVH}	—	0.6	—	V	—
Output High Short Circuit Pulsed Current	I_{O+}	3.5	4.5	—	A	V_O = 0V, PW ≤ 10 ms
Output Low Short Circuit Pulsed Current	I_{O-}	3.5	4.5	—	A	V_O = 15V, PW ≤ 10 ms

Notes:

1. The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: HIN and LIN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO-.
2. For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum, with a Pulse Width (PW) of 280 ns, minimum.

2.4. AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C , unless otherwise specified.						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Turn-on Propagation Delay	t_{on}	—	140	230	ns	V_S = 0V, see Figure 3-3.
Turn-off Propagation Delay	t_{off}	—	140	230	ns	V_S = 0V, see Figure 3-3.
Delay Matching, HS and LS Turn-on/Turn-off	t_{DM}	—	0	50	ns	See Figure 3-2.
Turn-on Rise Time	t_r	—	25	50	ns	V_S = 0V, see Figure 3-3.
Turn-off Fall Time	t_f	—	20	45	ns	V_S = 0V, see Figure 3-3.

3. Timing Waveforms

Figure 3-1. Input/Output Timing Diagram

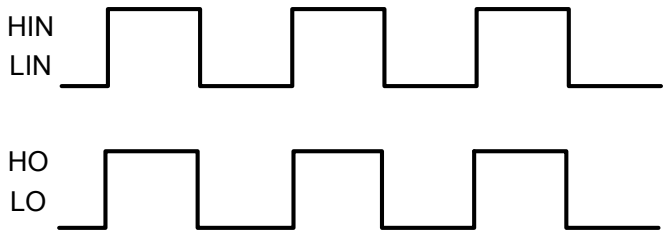


Figure 3-2. Delay Matching Waveform Definitions

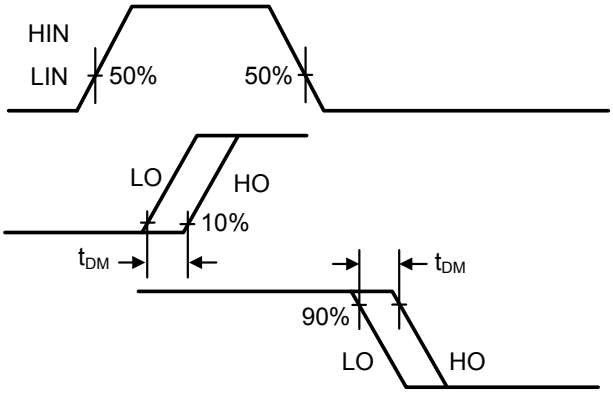
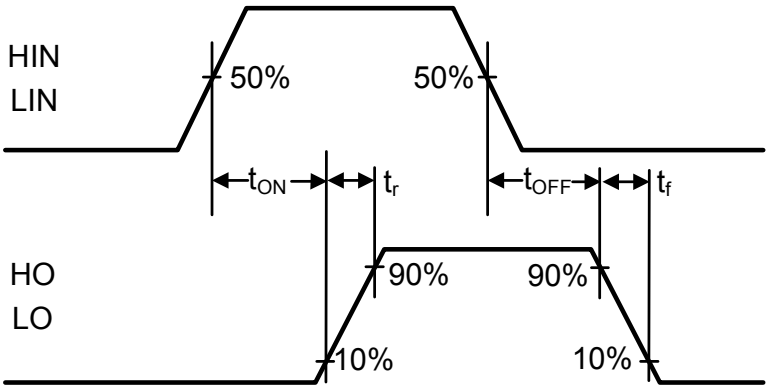


Figure 3-3. Switching Time Waveform Definitions



4. Typical Performance Curves

Figure 4-1. Output Source Current vs. Supply Voltage

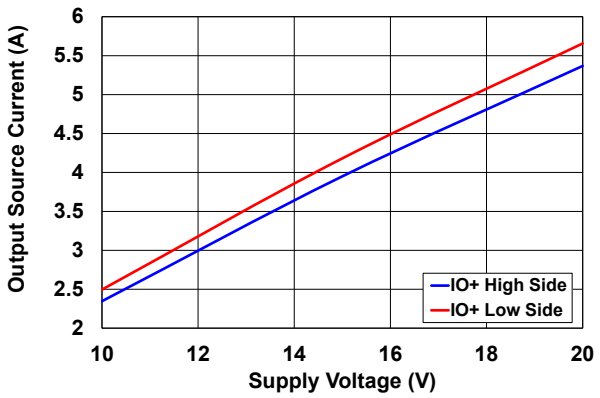


Figure 4-2. Output Source Current vs. Temperature

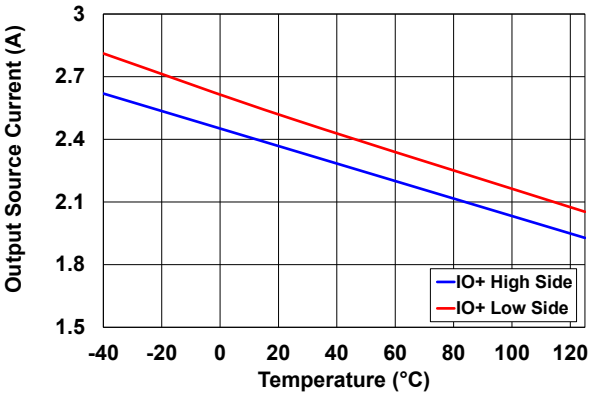


Figure 4-3. Output Sink Current vs. Supply Voltage

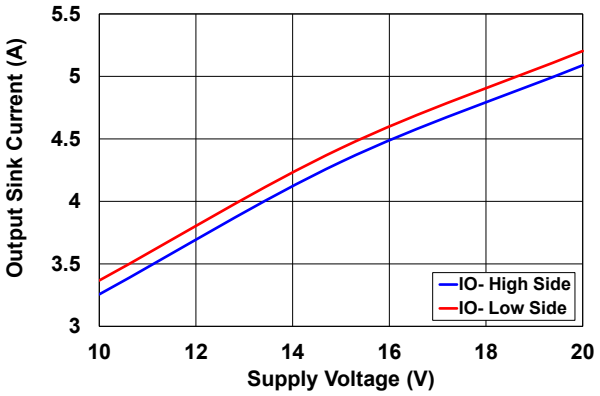


Figure 4-4. Output Sink Current vs. Temperature

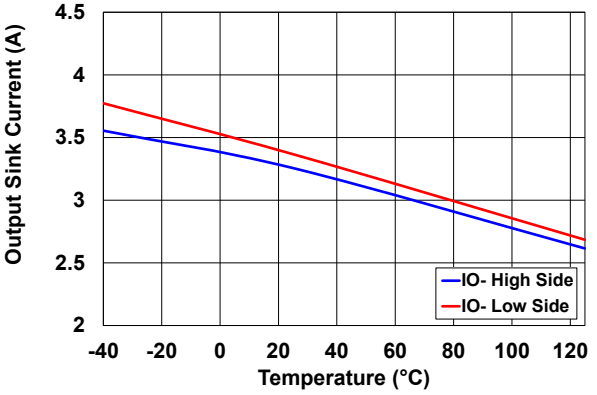


Figure 4-5. Logic 1 Input Voltage vs. Supply Voltage

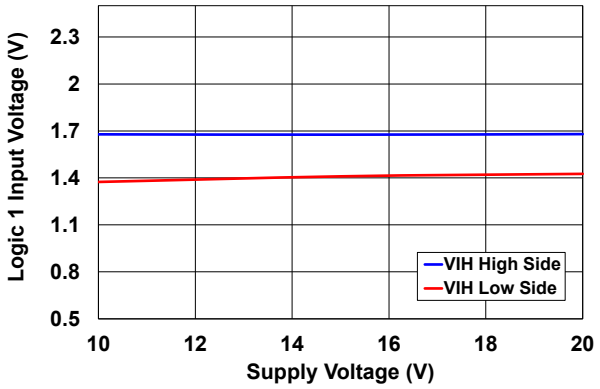


Figure 4-6. Logic 1 Input Voltage vs. Temperature

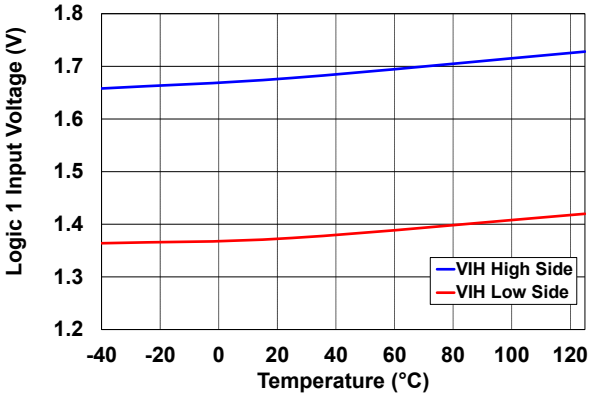


Figure 4-7. Logic 0 Input Voltage vs. Supply Voltage

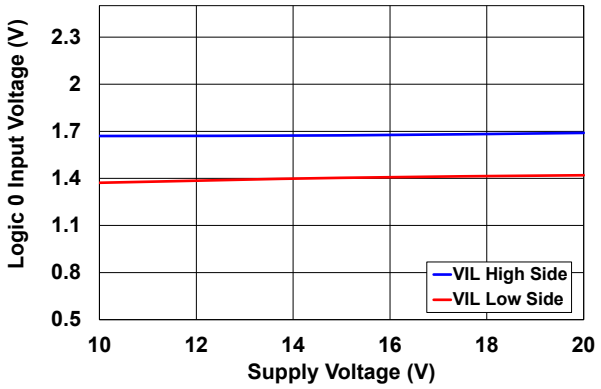


Figure 4-8. Logic 0 Input Voltage vs. Temperature

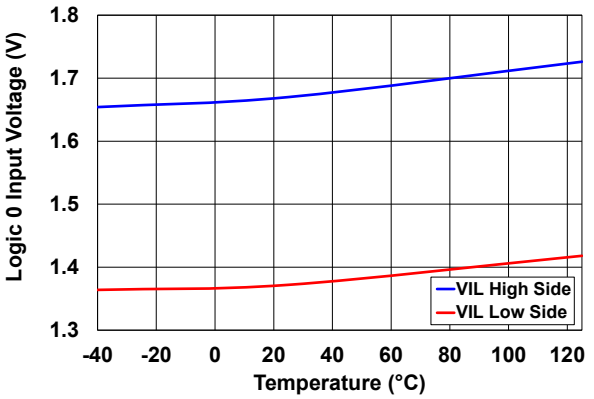


Figure 4-9. Quiescent Current vs. Supply Voltage

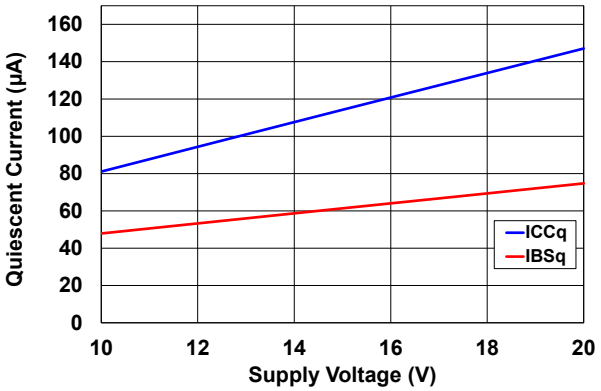


Figure 4-10. Quiescent Current vs. Temperature

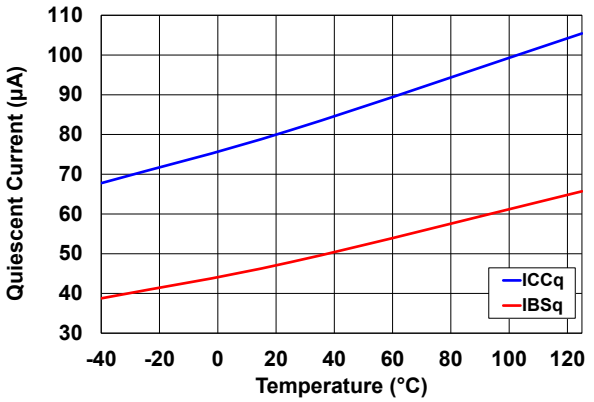


Figure 4-11. Turn-on Propagation Delay vs. Supply Voltage

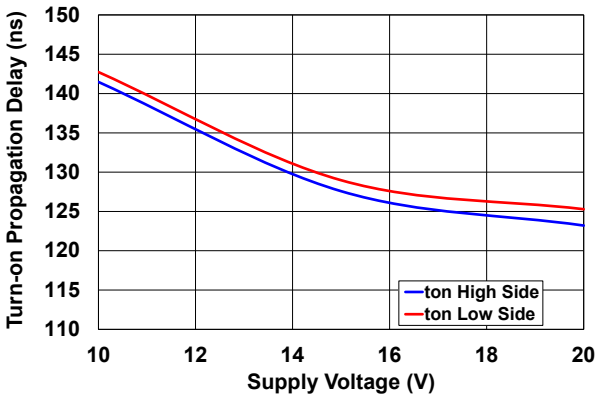


Figure 4-12. Turn-on Propagation Delay vs. Temperature

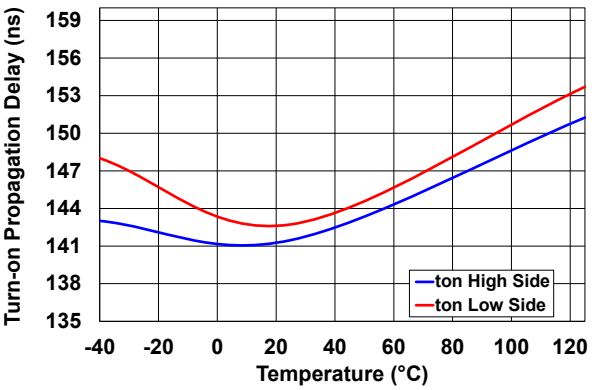


Figure 4-13. Turn-off Propagation Delay vs. Supply Voltage

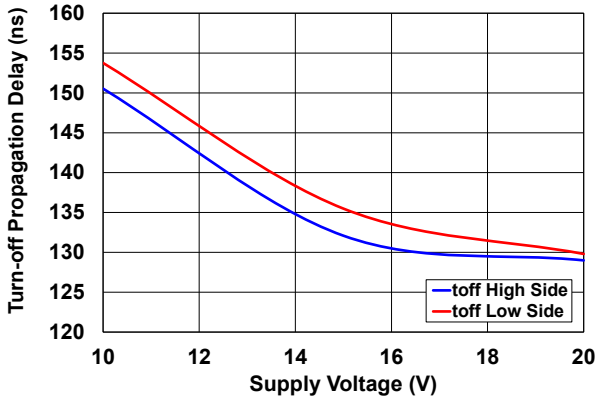


Figure 4-14. Turn-off Propagation Delay vs. Temperature

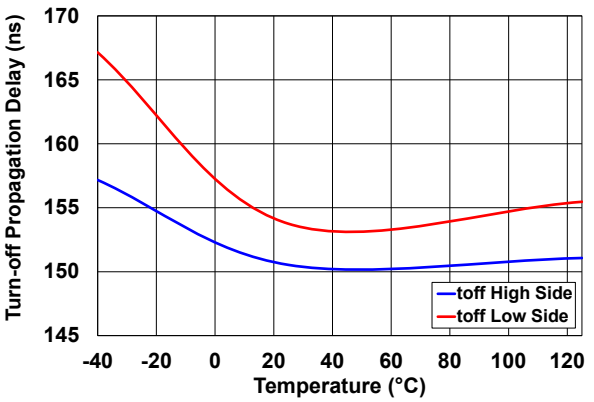


Figure 4-15. Rise Time vs. Supply Voltage

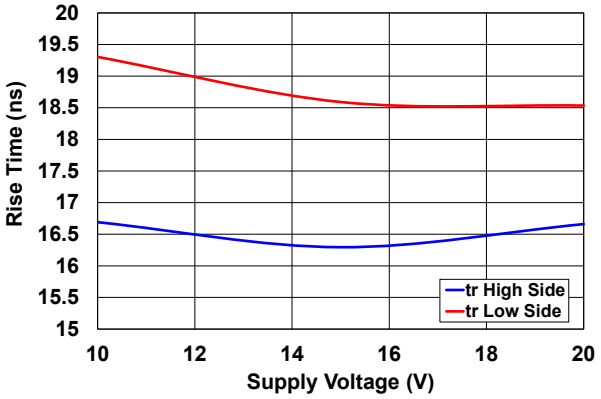


Figure 4-16. Rise Time vs. Temperature

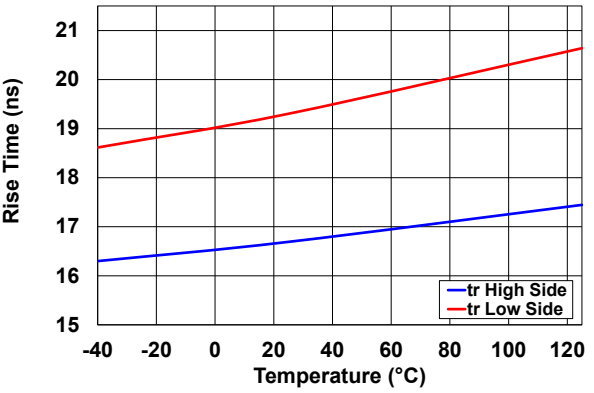


Figure 4-17. Fall Time vs. Supply Voltage

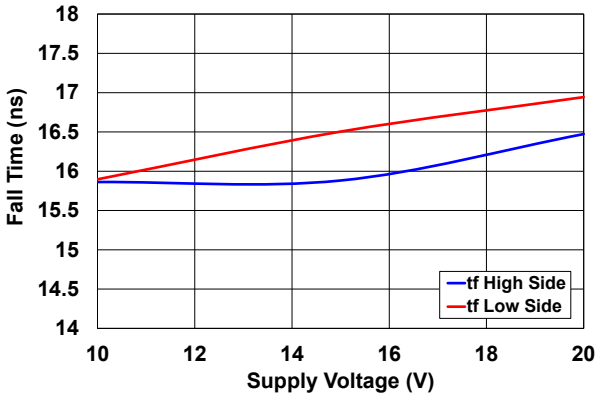


Figure 4-18. Fall Time vs. Temperature

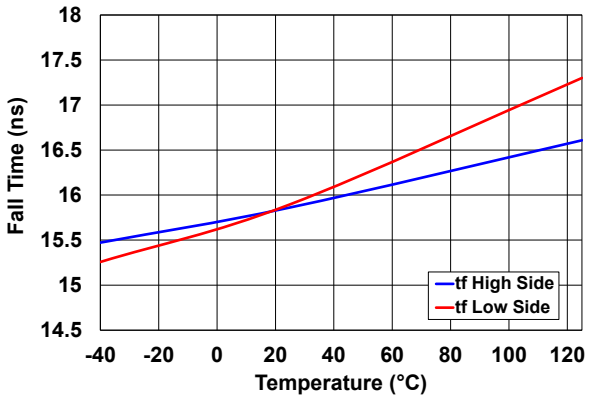


Figure 4-19. Delay Matching vs. Supply Voltage

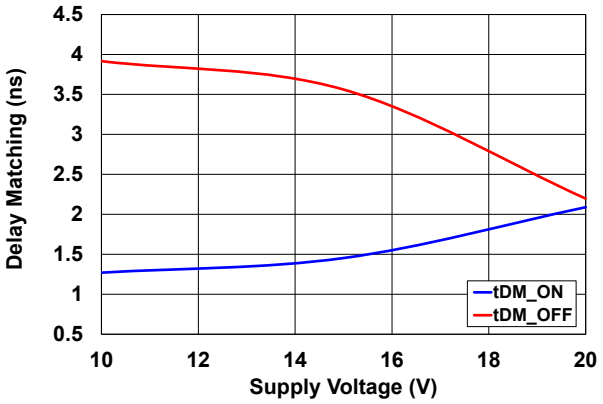


Figure 4-20. Delay Matching vs. Temperature

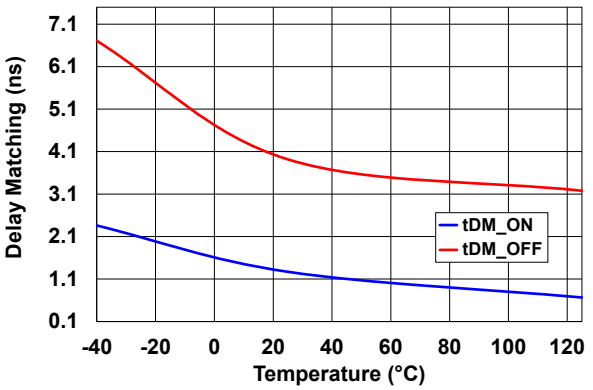


Figure 4-21. V_{CC} UVLO vs. Temperature

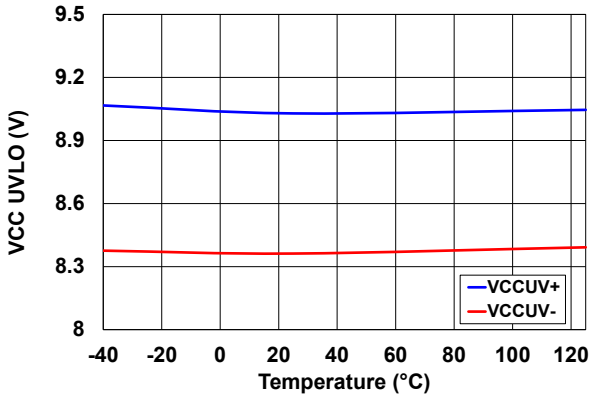


Figure 4-22. V_{BS} UVLO vs. Temperature

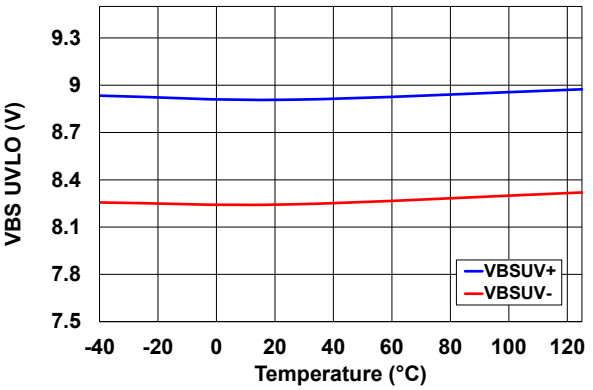
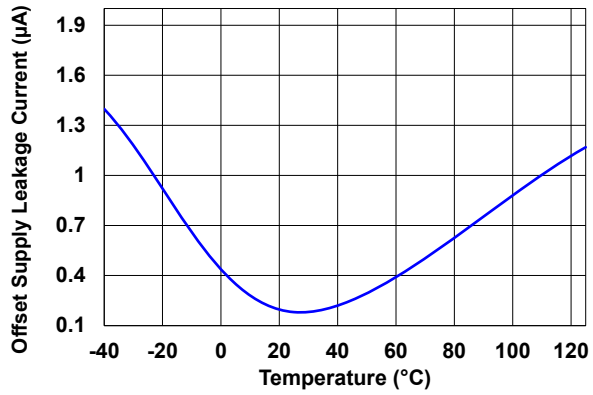


Figure 4-23. Offset Supply Leakage Current Temperature



5. Functional Description

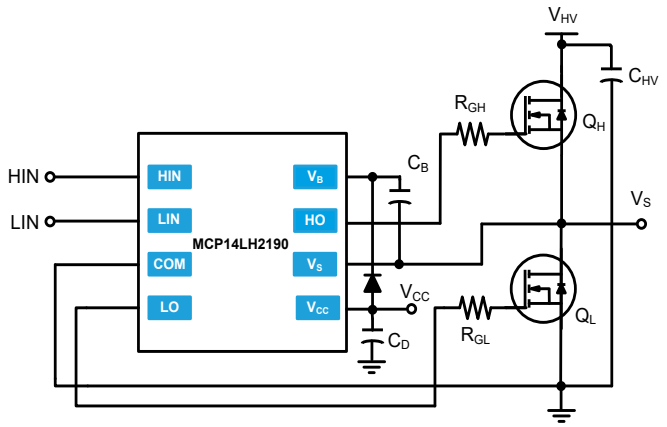
5.1. Half-bridge Configuration

A common configuration used for the MCP14LH2190(4) is a half-bridge (see Figure 5-1). In a half-bridge configuration, the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected. That line (V_S) is both the return for the high-side in the gate driver IC as well as the output of the half-bridge. When Q_H is ON and Q_L is OFF, V_S swings to high voltage, and when Q_H is OFF and Q_L is ON, V_S swings to GND. Hence, the output switches from GND to high voltage at the frequency of HIN and LIN. This line drives a transformer for a power supply or a coil on a motor.

In this half-bridge configuration, high voltage DC is input to the MOSFETs and converted to a high voltage switching signal to output to load (Figure 5-1). The MOSFETs operate in saturation mode and an important function of the gate driver is to turn ON the MOSFET quickly to minimize switching losses from the linear region of the MOSFET (turn ON and turn OFF); the MCP14LH2190(4) has a typical rise/fall time of 25 ns/20 ns into a 1 nF load.

Another important function of the gate driver IC in the half-bridge configuration is to convert the logic signals of control (MCP14LH2190(4) operates at logic 3.3V) to a voltage level and current capacity to drive the gate of the MOSFET and IGBT. This requires driving large currents initially to turn ON/turn OFF the MOSFET quickly. Also, the floating well of the high-side allows high voltage operation in the bootstrap operation.

Figure 5-1. MCP14LH2190 in a Half-bridge Configuration

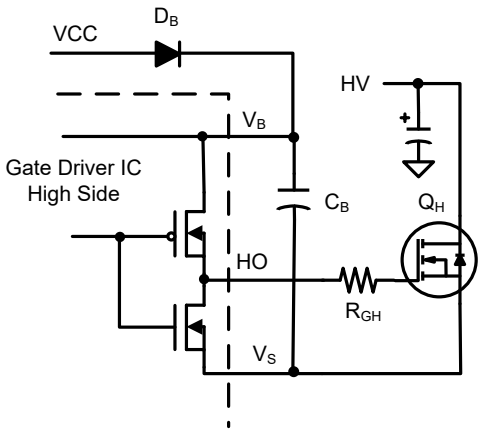


5.2. Bootstrap Operation

The supply for the MCP14LH2190(4) high-side is provided by the bootstrap capacitor C_B (see Figure 5-2). In the half-bridge configuration, V_S swings from 0V to V_{HV} depending on the PWM input of the IC. When V_S is 0V, V_{BS} will go below V_{CC} and V_{CC} will charge C_B . When HO goes high, V_S swings to V_{HV}, and V_{BS} remains at V_{CC} minus a diode drop (D_B) due to the voltage on C_B. This is the supply for the high-side gate driver and allows the gate driver to function with the floating well (V_S) at high voltage.

When considering the **value of the bootstrap capacitor C_B**, it is important that it is sized to provide enough energy to quickly drive the gate of Q_H . Values of 1 µF to 10 µF are recommended (the exact value depends on gate capacitance and the noise in the application). It is key to use a low-ESR capacitor that is placed close to the device. This will quickly supply charge to the gate of the MOSFET.

Figure 5-2. MCP14LH2190 High-side in Bootstrap Operation



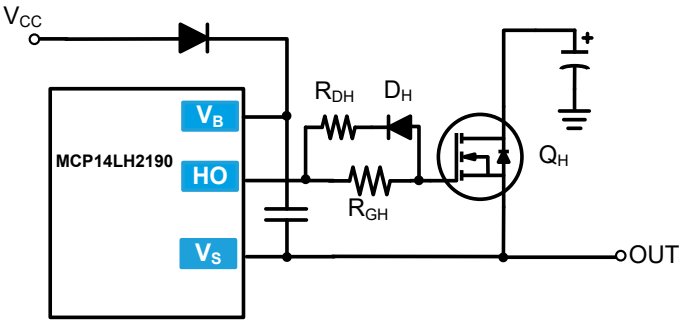
5.3. Gate Drive Control

The most crucial time for the gate drive is the turning ON and turning OFF of the MOSFET. Performing this function quickly, but with minimal noise and ringing, is key. If the rise/fall time is too fast, it can cause unnecessary ringing; if the rise/fall time is too slow, it will increase switching losses in the MOSFET.

An example of just the high-side gate driver is shown in Figure 5-3 (any selection of gate driver components should be the same for high-side and low-side drive); two extra components are seen: R_{DH} and D_H. With the careful selection of R_{GH} and R_{DH}, it is possible to selectively control the rise time and fall time of the gate drive. For turn ON, all current will go from the IC through R_{GH} and charge the MOSFET gate capacitor. Therefore, increasing or decreasing R_{GH} will increase or decrease rise time in the application. With the addition of D_H, the fall time can be separately controlled as the turn OFF current flows from the MOSFET gate capacitor, through D_H and R_{DH} to the driver in the IC to V_S. So increasing or decreasing R_{DH} will increase or decrease the fall time.

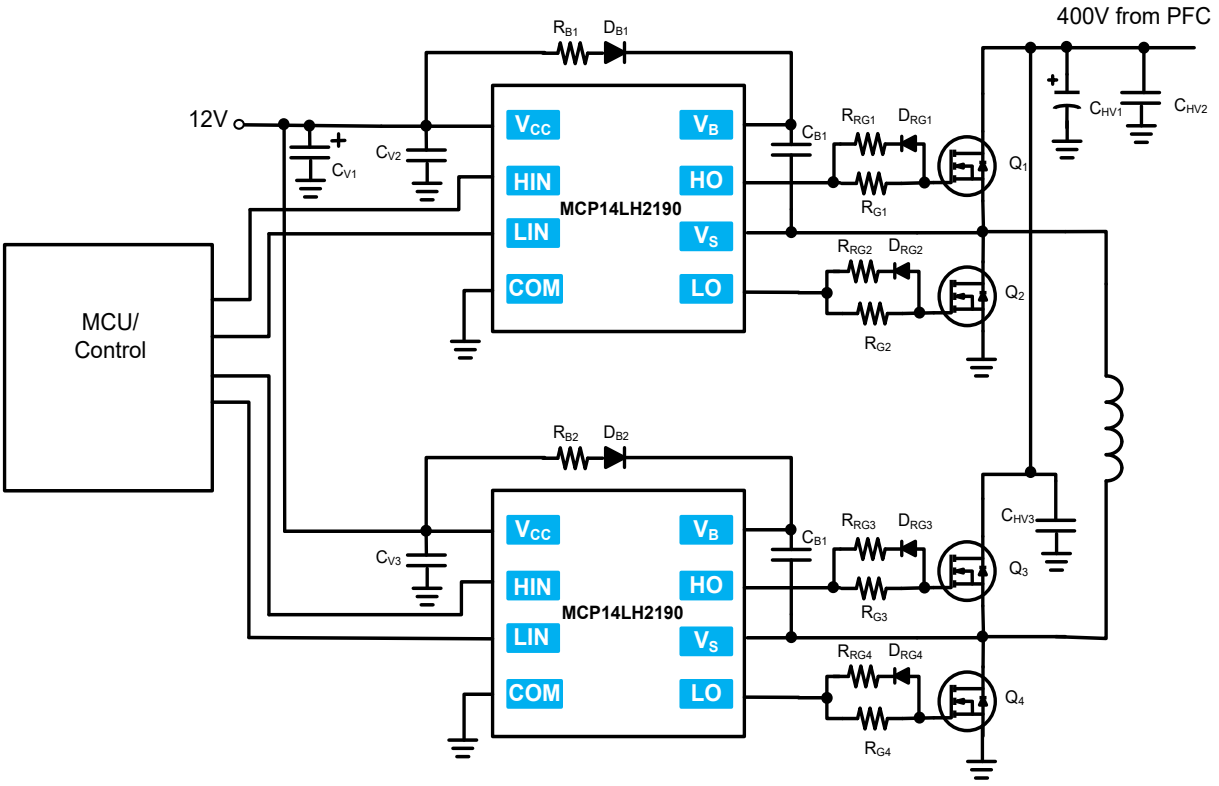
Increasing turn ON and turn OFF has the effect of limiting ringing and noise due to parasitic inductances. So, with a noisy environment, it may be necessary to increase the gate resistors. For **gate resistor value selection** the exact value depends on the type of application and desired level of noise and ringing expected. Generally, power supplies switch at fast speeds, and want to squeeze out efficiency of the MOSFETs, so lower values are recommended (for example, R_{GH} = 5Ω to 20Ω). For motors, the switching speed is generally slower, and the application has more inherent noise, so higher values are recommended (for example, R_{GH} = 20Ω to 100Ω).

Figure 5-3. Gate Drive Control



6. Application Information

Figure 6-1. Primary Side of Full-Bridge Converter Using the MCP14LH2190



- RRG1, RRG2, RRG3, and RRG4 values are typically between 0Ω and 10Ω. The exact value is decided based on the MOSFET junction capacitance and the drive current of gate driver. A value of 10Ω is used in this example.
- It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for V_{DD} = 15V) with a minimum pulse width of 280 ns.
- RG1, RG2, RG3, and RG4 values are typically between 20Ω and 100Ω. The exact value is decided based on the MOSFET junction capacitance and drive current of the gate driver. A value of 50Ω is used in this example.
- RB1 and RB2 values are typically between 3Ω and 20Ω. The exact value is calculated based on the bootstrap capacitor value and the amount of current limiting required for bootstrap capacitor charging. A value of 10Ω is used in this example. Also, DB1 and DB2 should be an ultra-fast diode with a minimum rating of 1A and a voltage rating greater than the system operating voltage.

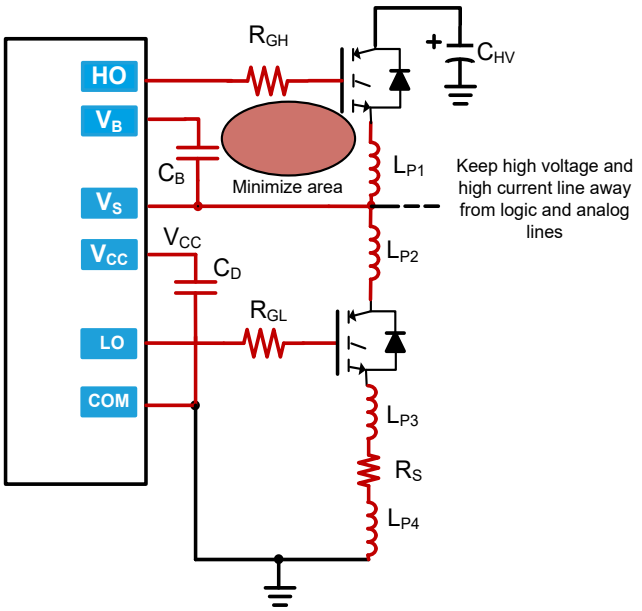
Layout Considerations

Layout plays a considerable role in noise and ringing in a circuit. Unwanted noise coupling, unpredicted glitches, and abnormal operation could arise due to poor layout of the associated components. Figure 6-2 shows a half-bridge schematic with parasitic inductances in the high-current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which is caused by inductance in the metal of the trace.

Considering Figure 6-2, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible. Low-ESR ceramic capacitors should be used to minimize inductance. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface-mount devices. These suggestions will reduce the parasitics due to the PCB traces.

Generally, for the **decoupling capacitor** (C_D), at least one low-ESR capacitor is recommended close to the V_{CC} pin. Recommended values are 1 µF to 10 µF. A second smaller decoupling capacitor is sometimes added to provide better high frequency response (for example, 0.1 µF).

Figure 6-2. Layout Suggestions for MCP14LH2190(4) in a Half-Bridge Configuration



Application Example

Figure 6-3. Three Phase Motor Driver using the MCP14LH2190

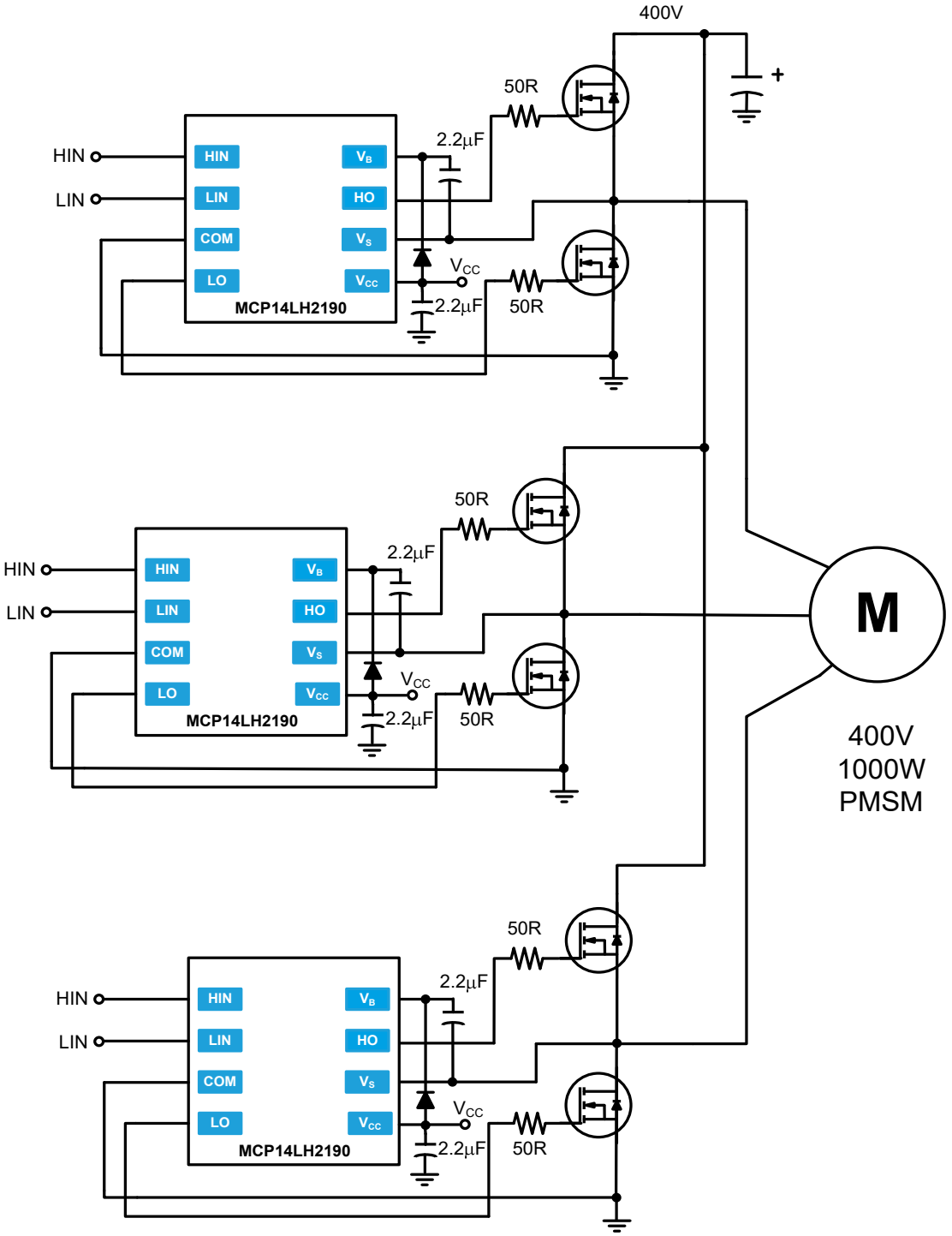
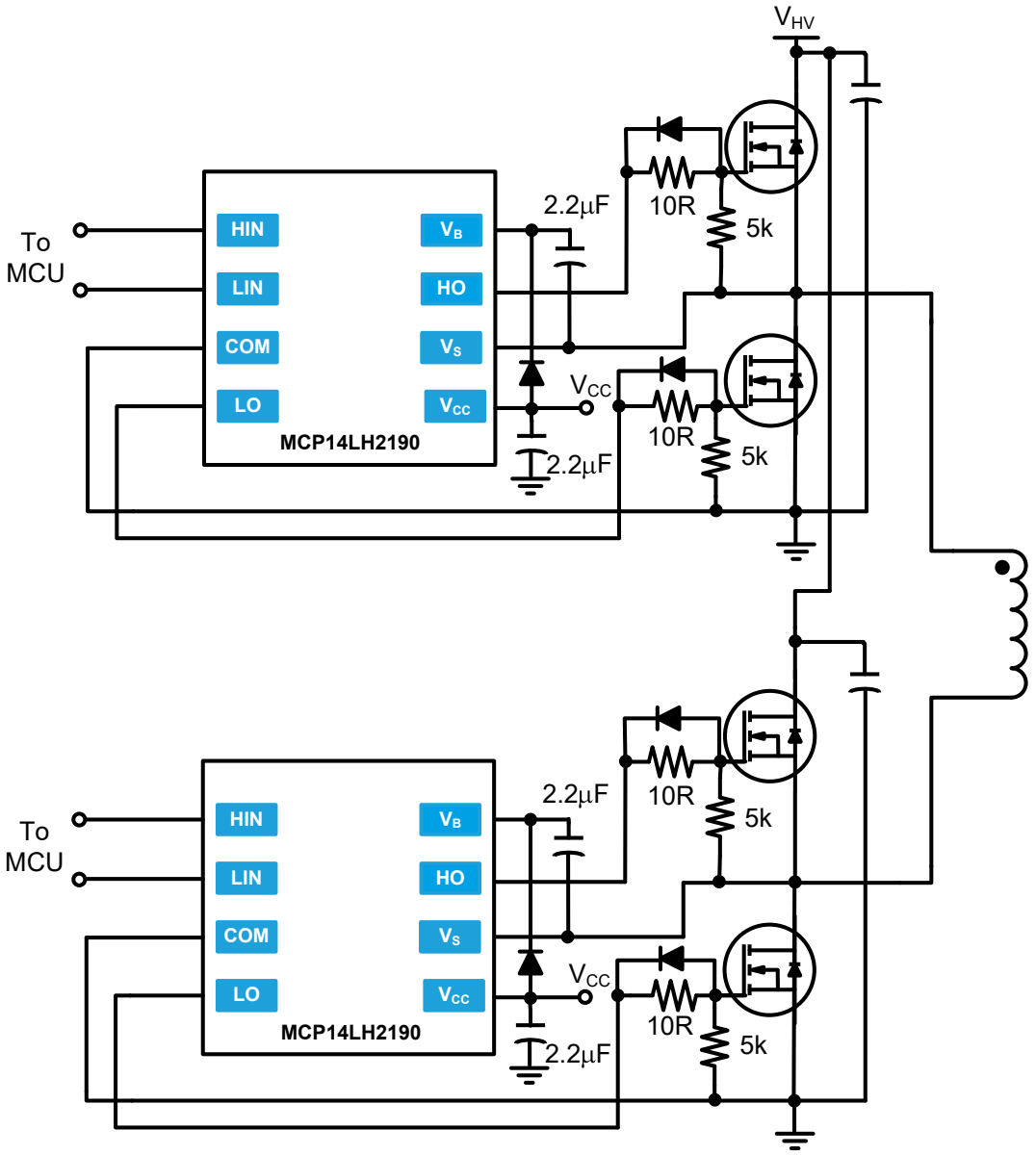


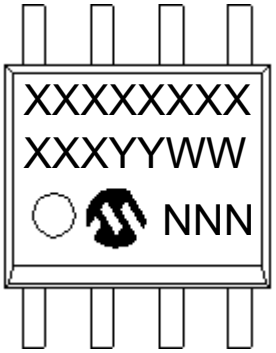
Figure 6-4. The MCP14LH2190 Full-Bridge Configuration for 1 kW - 3 kW Power Supply



7. Packaging Information

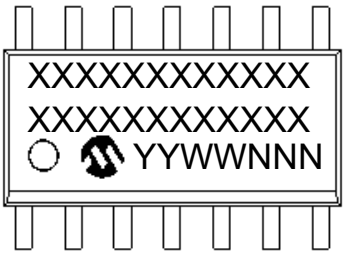
Package Marking Information

8-Pin SOIC (MCP14LH2190):

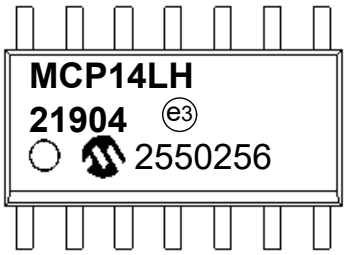


Example:

14-Pin SOIC (MCP14LH21904):



Example:



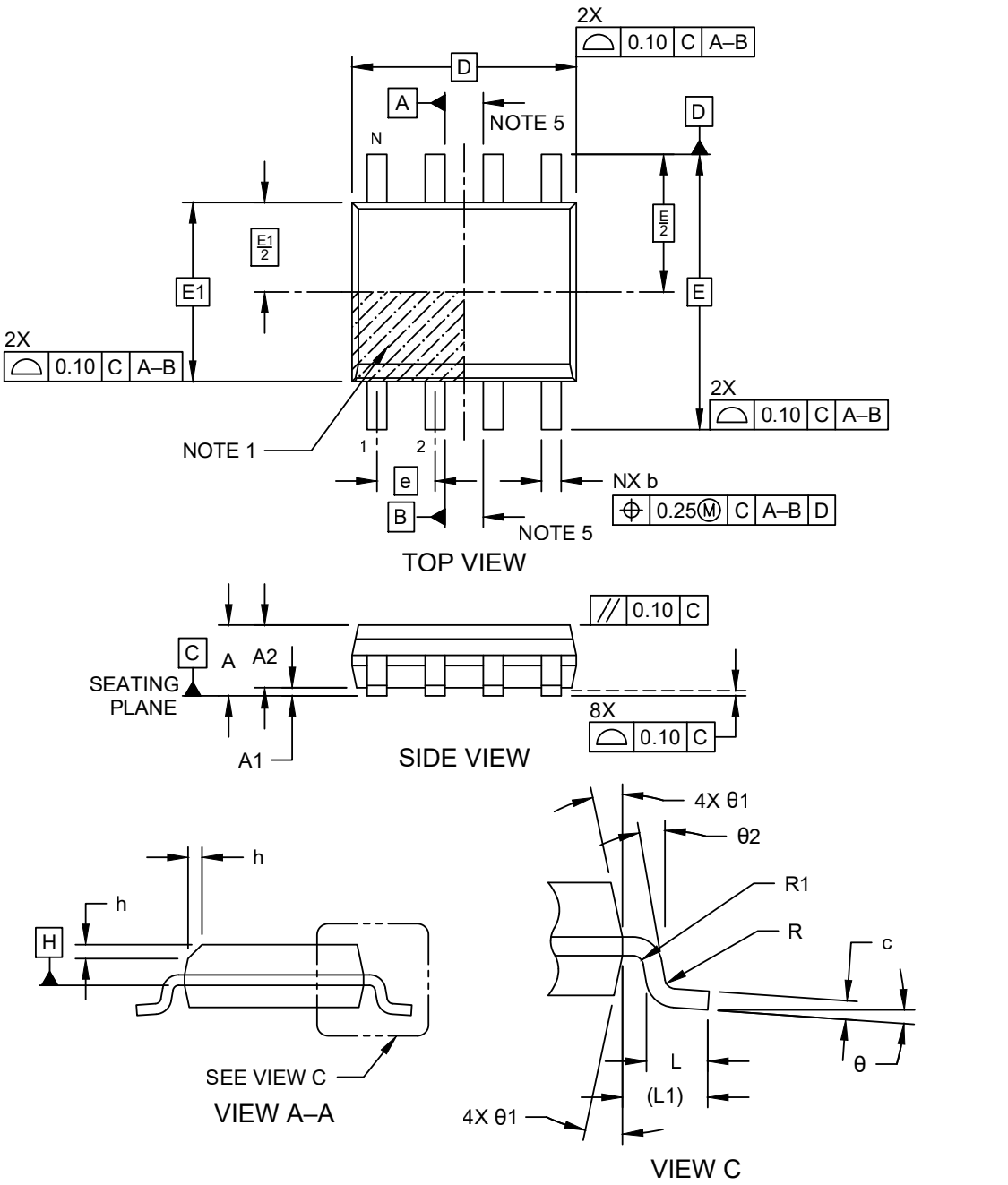
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

Package Outline Drawings

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

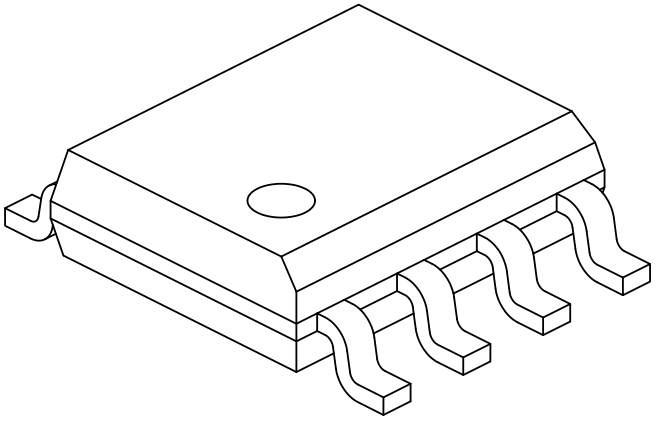
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

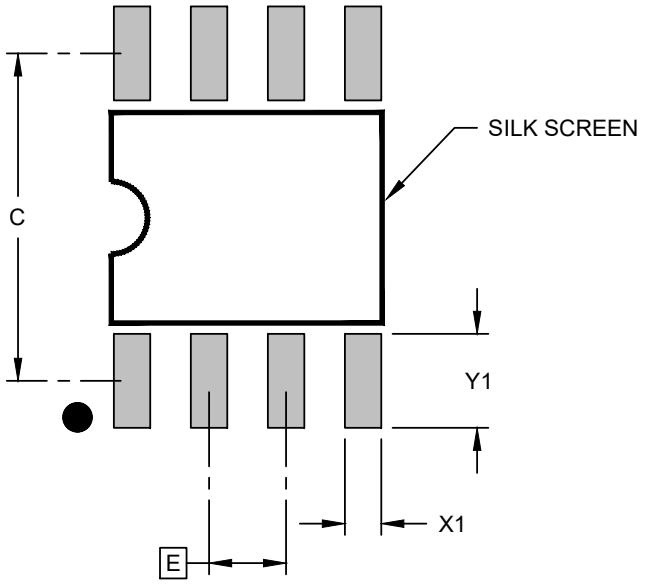
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

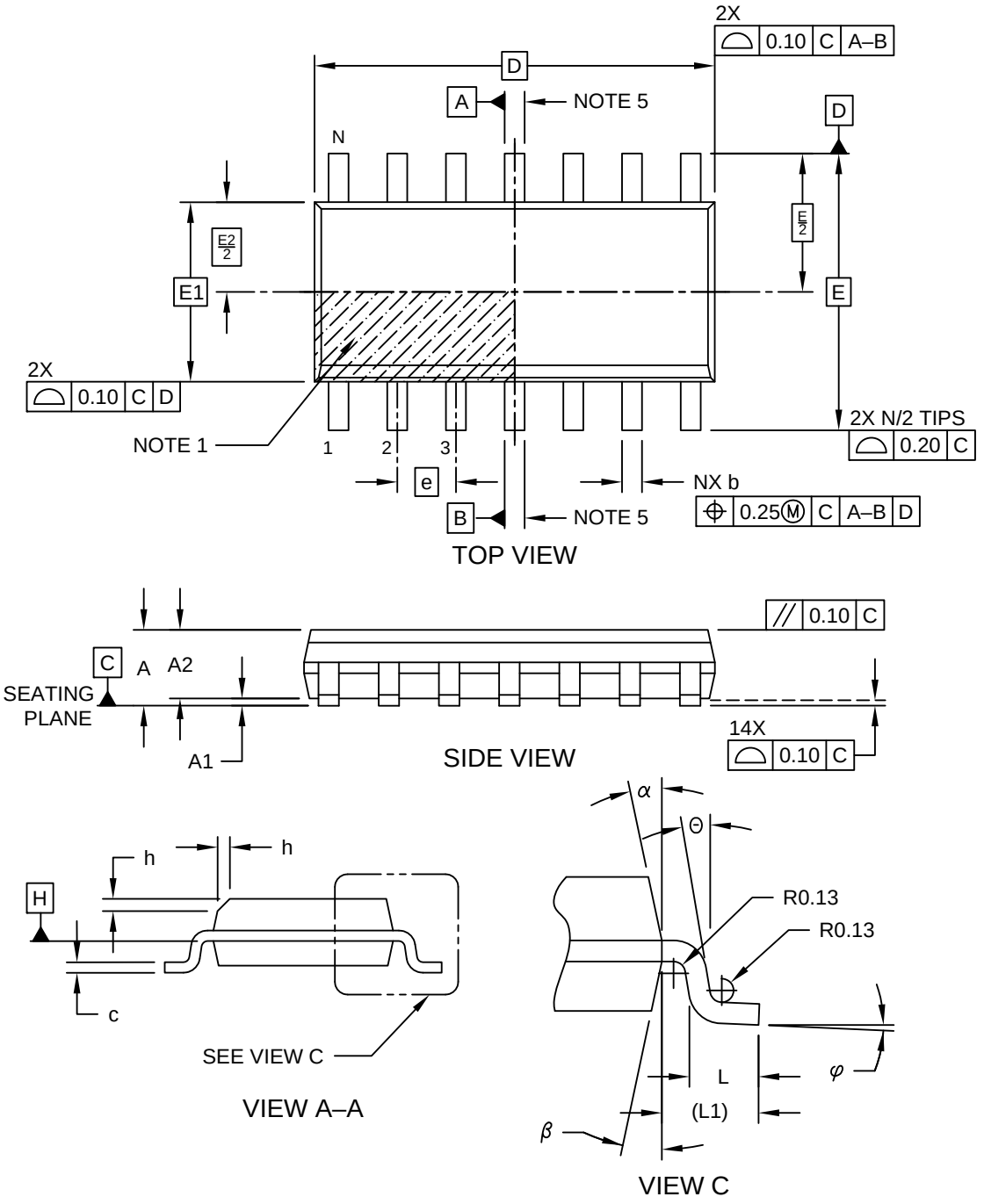
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-C2X Rev L

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

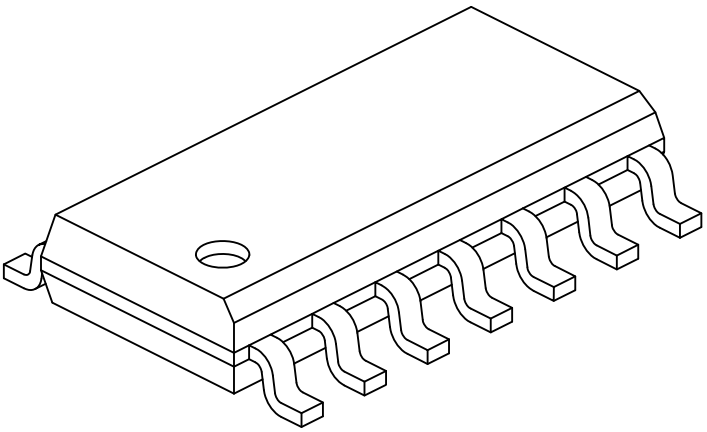
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

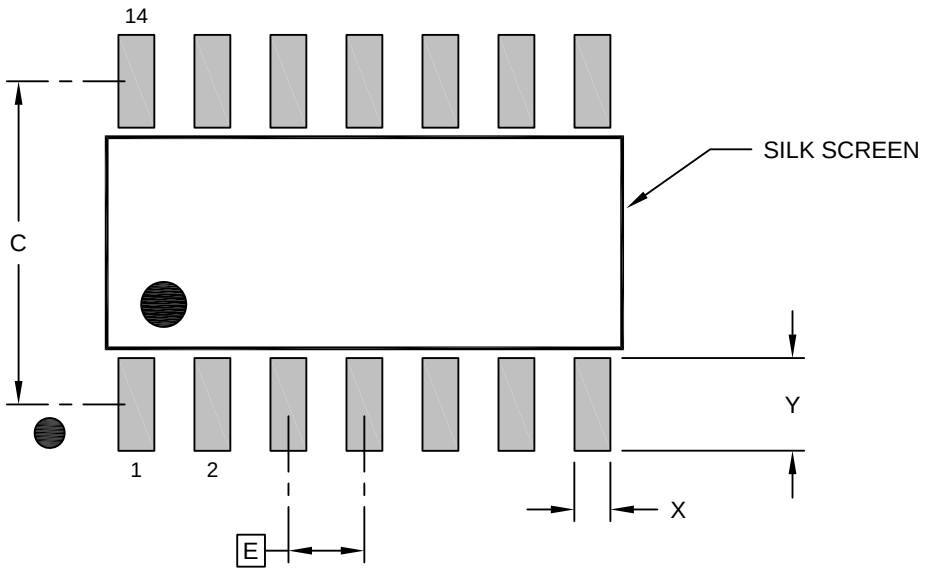
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

8. Revision History

Doc. Rev.	Date	Section	Comments
DS20007068A	November 2025	—	Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

Device:	MCP14LH2190(4): High-Side and Low-Side Gate Driver	
Tape and Reel Option(1):	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	SN	= Plastic Small Outline IC, 3.90 mm, SOIC, 8-Pin (Package Code: SN)
	SL	= Plastic Small Outline IC, 3.90 mm, SOIC, 14-Pin (Package Code: SL)

Examples:

- MCP14LH2190T-E/SN: Half-Bridge Gate Driver, Tape and Reel, Extended Temperature Range, SOIC-8 Package
- MCP14LH21904T-E/SL: Half-Bridge Gate Driver, Tape and Reel, Extended Temperature Range, SOIC-14 Package

Notes:

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2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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