NIV1161, NIS1161

ESD Protection with Automotive Short-to-Battery Blocking

Low Capacitance ESD Protection with short−to−battery blocking for Automotive High Speed Data Lines

The NIS/NIV1161 is designed to protect high speed data lines from ESD as well as short to vehicle battery situations. The ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines while the low $R_{DS(on)}$ FET limits distortion on the signal lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB and LVDS protocols.

Features

- Low Capacitance (0.65 pF Typical, I/O to GND)
- Diode Capacitance Matching Between I/O's: 1% Typical
- Optimized Layout for Excellent High Speed Signal Integrity
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Automotive High Speed Signal Pairs
- USB2.0/3.0
- LVDS
- HDMI
- APIX2

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_{J(max)}$	−55 to +150	°C
Storage Temperature Range	TSTG	−55 to +150	°C
Drain−to−Source Voltage	V_{DSS}	30	V
Gate−to−Source Voltage	V_{GS}	±10	V
Lead Temperature Soldering	T_{SLD}	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±8 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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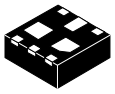
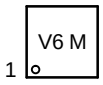
MARKING DIAGRAM

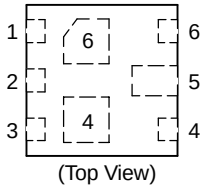


WDFN6
CASE 511CB

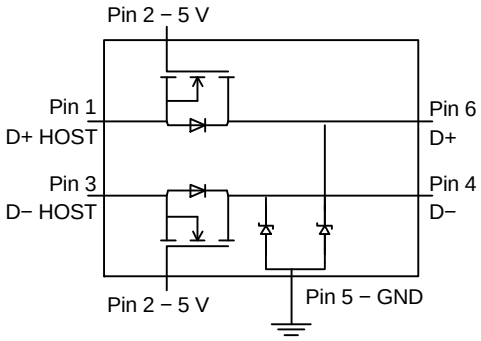


V6 = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATICS



(Top View)



ORDERING INFORMATION

Device	Package	Shipping†
NIV1161MTTAG	WDFN−6 (Pb−Free)	3000 / Tape & Reel
NIS1161MTTAG	WDFN−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND		5	16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	16.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1.0	μA
Clamping Voltage	V_C	I_{PP} = 1 A, I/O Pin to GND (8 x 20 μs pulse)			26	V
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 KV Contact	See Figures 1 & 2			
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		34 55 −5.2 −10		V V V V
Junction Capacitance Match	ΔC_J	V_R = 0 V, f = 1 MHz between I/O1 to GND and I/O2 to GND		1.0		%
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND (Pin 7 to GND, Pin 9 to GND)		0.65		pF
Drain−to−Source Breakdown Voltage	$V_{BR(DSS)}$	V_{GS} = 0 V, I_D = 100 μA	30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{BR(DSS)}/T_J$	Reference to 25°C, I_D = 100 μA		27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V			±1.0	μA
Gate Threshold Voltage (Note 3)	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 100 μA	0.1	1.0	1.5	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C, I_D = 100 μA		−2.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 125 mA		1.4	7.0	Ω
		V_{GS} = 2.5 V, I_D = 125 mA		2.3	7.5	
Forward Transconductance	g_{FS}	V_{DS} = 3.0 V, I_D = 125 mA		80		mS
Switching Turn−On Delay Time (Note 4)	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 24 V I_D = 125 mA, R_G = 10 VΩ		9		nS
Switching Turn−On Rise Time (Note 4)	t_r			41		nS
Switching Turn−Off Delay Time (Note 4)	$t_{d(OFF)}$			96		nS
Switching Turn−Off Fall Time (Note 4)	t_f			72		nS
Drain−to−Source Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 125 mA		0.79	0.9	V
3 dB Bandwidth	f_{BW}	R_L = 50 Ω		5		GHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 3 and 4 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.
3. Pulse test: pulse width ≤ 300 μS, duty cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperatures.

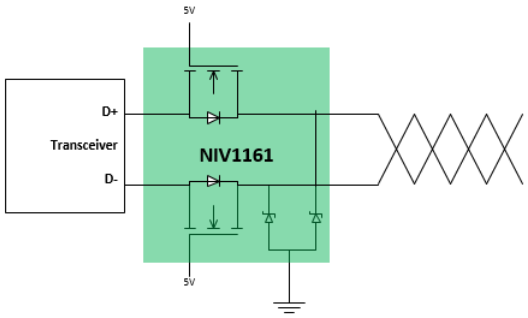
Figure 1. IEC61000−4−2 +8kV Contact ESD Clamping Voltage

Figure 2. IEC61000−4−2 −8kV Contact ESD Clamping Voltage

Application

Today's connected cars are using multiple high speed signal pair interfaces for various applications such as infotainment, connectivity and ADAS. The electrical hazards likely to be encountered in these automotive high speed signal interfaces include damaging ESD and transient events which occur during manufacturing and assembly, by vehicle occupants or other electrical circuits in the vehicle. The major documents discussing ESD and transient events as far as road vehicles are concerned are ISO 10605 (Road vehicles − Test methods for electrical disturbances from electrostatic discharge) which describes ESD test methods and ISO 7637 (Road vehicles − Electrical disturbances from conduction and coupling) for effects caused by other electronics in the vehicle. IS0 10605 is based on IEC 61000−4−2 Industry Standard, which specifies the various levels of ESD signal characteristics, but also includes additional vehicle−specific requirements. Further, OEM specific test requirements are usually also imposed. In addition, these high speed signal pairs require protection from short−to−battery (which goes up to 16 VDC) and short−to−ground faults.

A suitable protection solution must satisfy well known constraints, such as low capacitive loading of the signal lines to minimize signal attenuation, and also respond quickly to surges and transients with low clamping voltage. In addition, small package sizes help to minimize demand for board−space while providing the ability to route the trace signals with minimal bending to maintain signal integrity.



The NIV1161 provides a solution to these high speed signal interface protections from ESD as well as short−to−battery situations. The ESD−protection is designed to meet the IEC61000−4−2 level 4 with a low I/O−to−ground capacitance of 0.65 pF typical. Capacitances are closely matched to preserve signal integrity. Low dynamic resistance allows very low clamping voltages, and the breakdown voltage of 16.5 V allows the device to survive a short−to−battery condition, which ranges from 9 V to 16 V. The series FETs are designed with very low on−state resistance ($R_{DS(ON)}$), and feature an internal layout that allows flow−through design to maintain high−speed signal integrity. The threshold voltage of 1.0 V allows operation at low gate−drive voltages consistent with USB, LVDS and other low level signals.

TYPICAL MOSFET PERFORMANCE CURVES

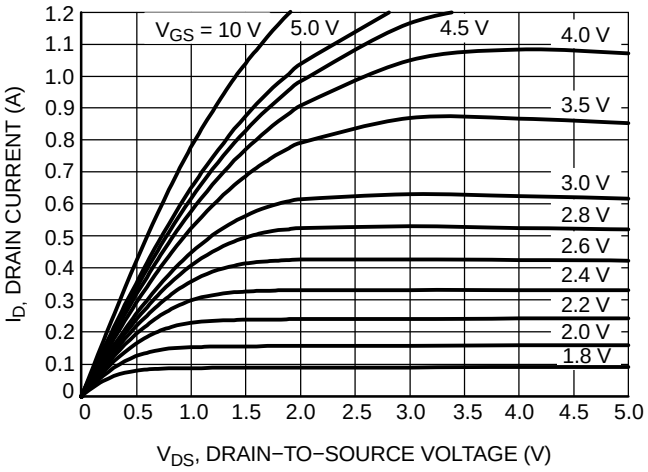


Figure 1. On−Region Characteristics

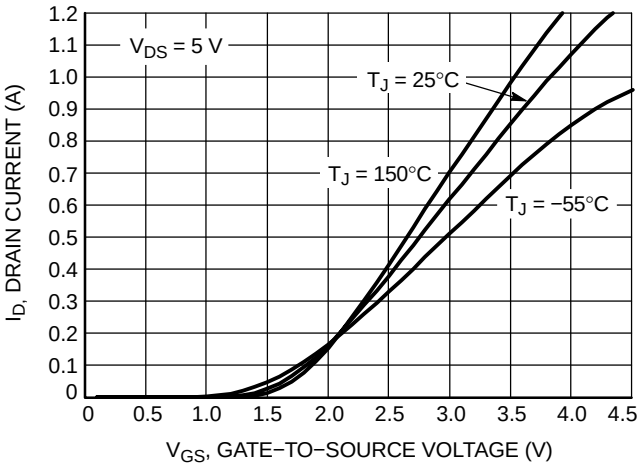


Figure 2. Transfer Characteristics

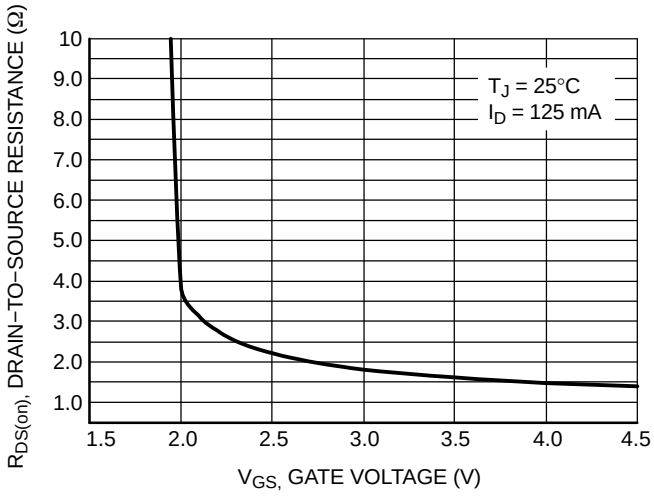


Figure 3. On−Resistance vs. Gate−to−Source Voltage

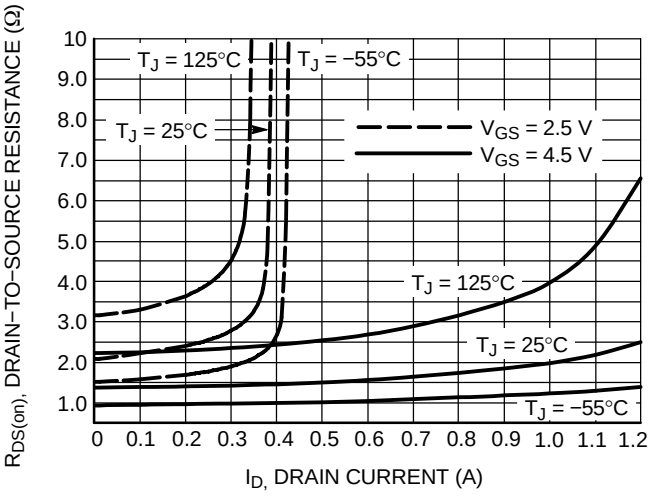


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

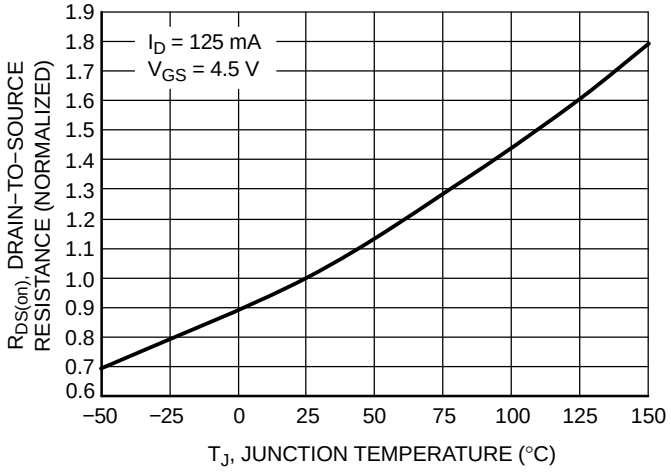


Figure 5. On−Resistance Variation with Temperature

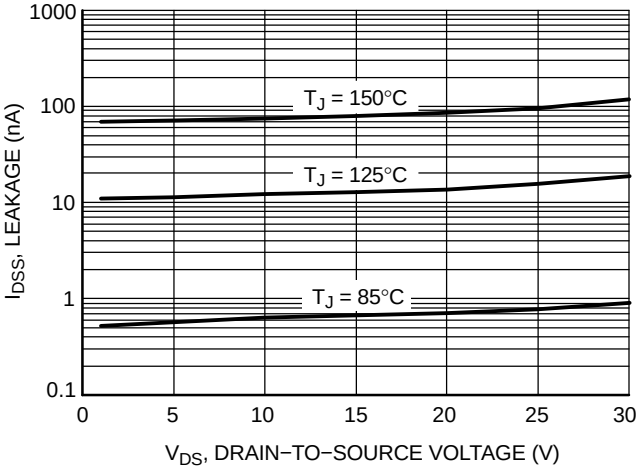
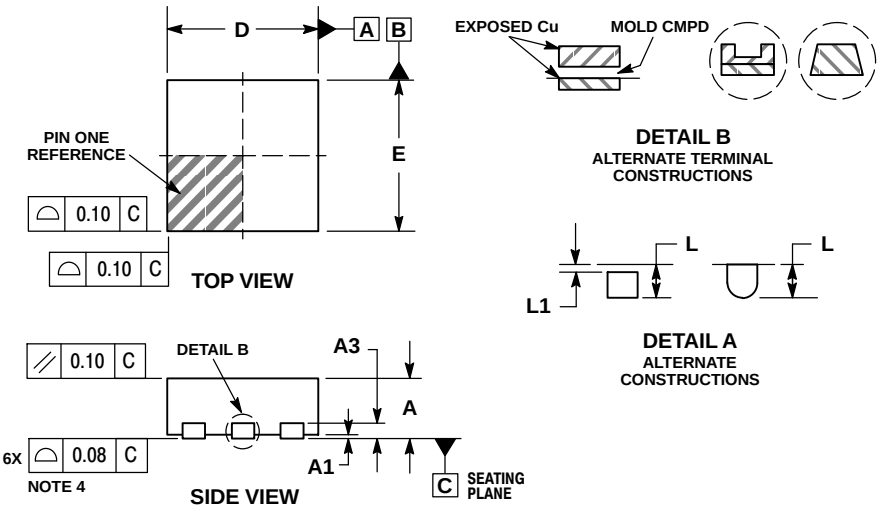


Figure 6. Drain−to−Source Leakage Current vs. Voltage

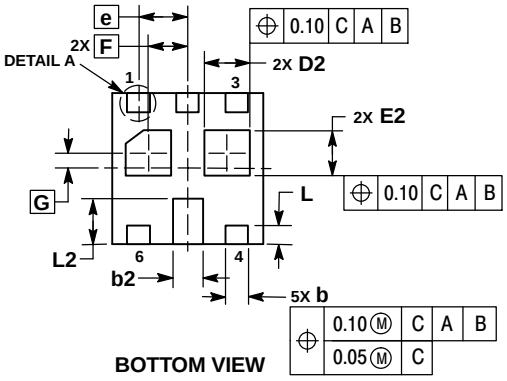
PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 511CB
ISSUE O

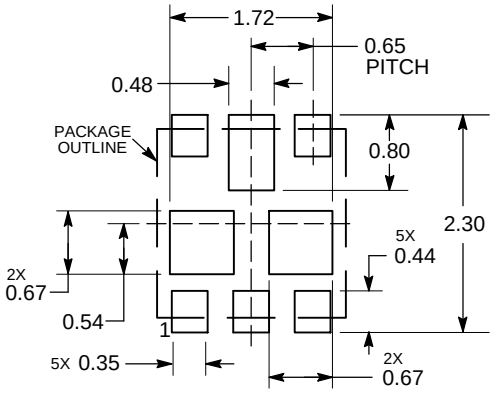


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b2	0.35	0.45
D	2.00 BSC	
D2	0.55	0.65
E	2.00 BSC	
E2	0.55	0.65
e	0.65 BSC	
F	0.52 BSC	
G	0.20 BSC	
L	0.20	0.30
L1	---	0.15
L2	0.55	0.65



RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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