

TC74ACT175P, TC74ACT175F, TC74ACT175FN

Quad D-Type Flip Flop with Clear

The TC74ACT175 is an advanced high speed CMOS QUAD D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

These four flip-flops are controlled by a clock input (CK) and a clear input (CLR).

The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and $\overline{Q}1$ thru $\overline{Q}4$) on the positive-going edge of the clock pulse.

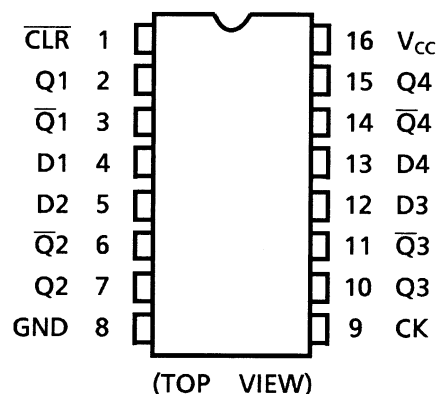
Reset function is accomplished when the clear input is taken low, and all Q outputs are kept in low level regardless of other input conditions.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

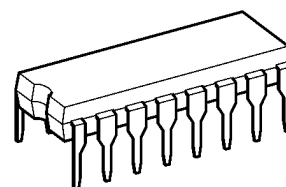
- High speed: $f_{max} = 160$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8$ μ A (max) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs: $V_{IL} = 0.8$ V (max)
 $V_{IH} = 2.0$ V (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F175

Pin Assignment



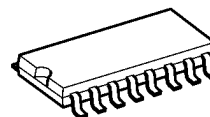
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74ACT175P



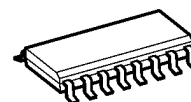
DIP16-P-300-2.54A

TC74ACT175F



SOP16-P-300-1.27A

TC74ACT175FN

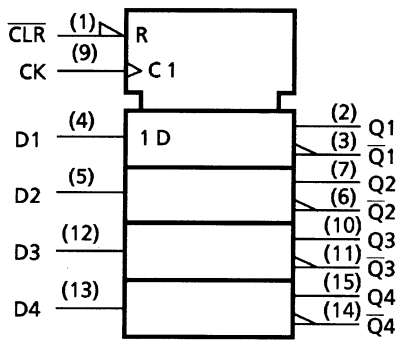


SOL16-P-150-1.27

Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

IEC Logic Symbol

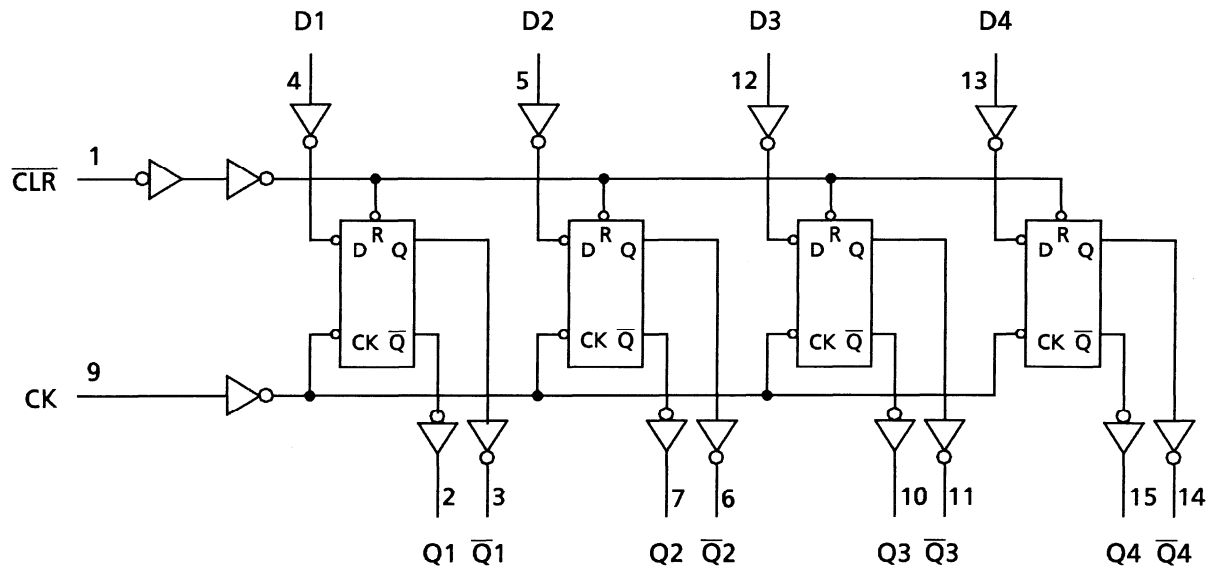


Truth Table

Inputs			Outputs		Function
CLR	D	CK	Q	$\overline{Q}$	
L	X	X	L	H	Clear
H	L	$\uparrow$	L	H	—
H	H	$\uparrow$	H	L	—
H	X	$\downarrow$	Q_n	$\overline{Q}_n$	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
					V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—			4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—			4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5	4.4	4.5	—	4.4	—	V	
			I _{OH} = -24 mA	4.5	3.94	—	—	3.80	—		
			I _{OH} = -75 mA (Note)	5.5	—	—	—	3.85	—		
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V	
			I _{OL} = 24 mA	4.5	—	—	0.36	—	0.44		
			I _{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65		
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND			5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND			5.5	—	—	8.0	—	80.0	μA
	I _C	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND			5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C	Ta = -40 to 85°C	Unit	
			VCC (V)	Limit		Limit
Minimum pulse width (CK)	tW (L) tW (H)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width (CLR)	tW (L)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time	tS	—	5.0 ± 0.5	4.0	4.0	ns
Minimum hold time	tH	—	5.0 ± 0.5	1.0	1.0	ns
Minimum removal time (CLR)	trem	—	5.0 ± 0.5	4.0	4.0	ns

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q, $\overline{Q}$)	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	6.9	11.0	1.0	12.5	ns
Propagation delay time ($\overline{\text{CLR}}$ -Q, $\overline{Q}$)	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	6.5	10.4	1.0	11.8	ns
Maximum clock frequency	f _{max}	—	5.0 ± 0.5	80	145	—	80	—	MHz
Input capacitance	C _{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C _{PD} (Note)	—		—	46	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per F/F)}$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD}(\text{total}) = 25 + 21 \cdot n$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

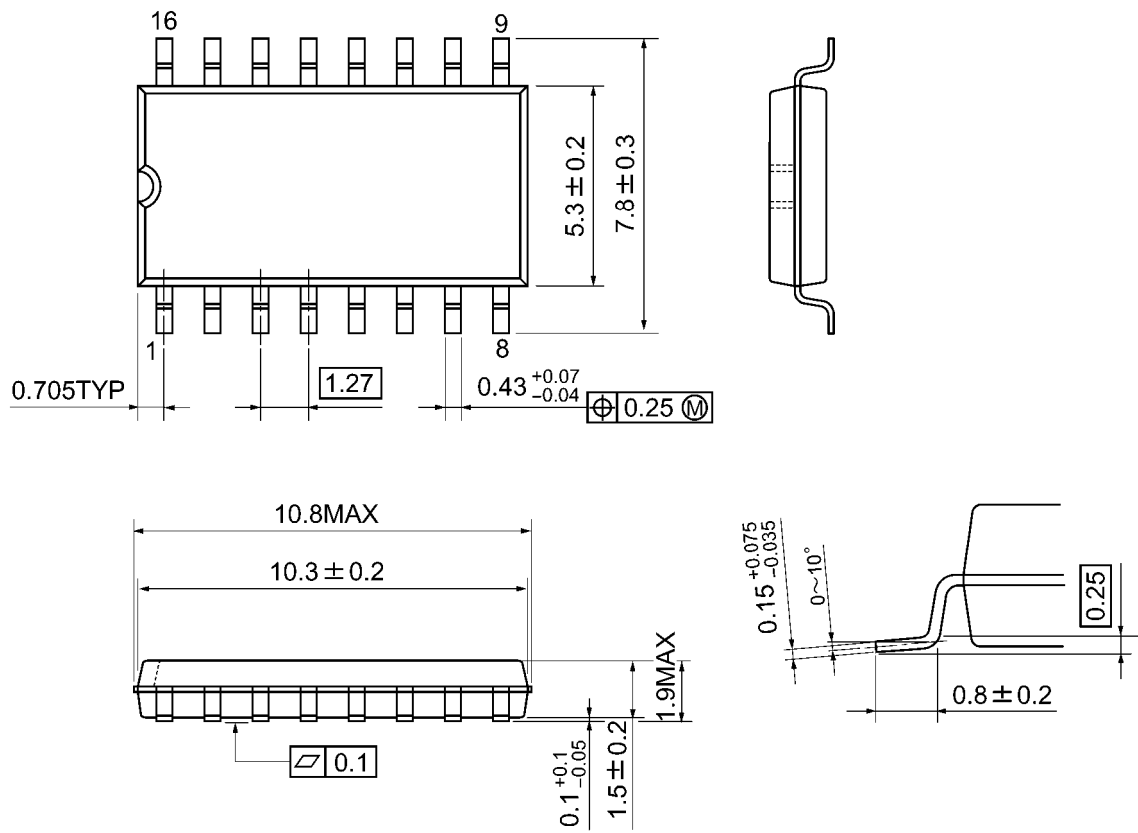


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

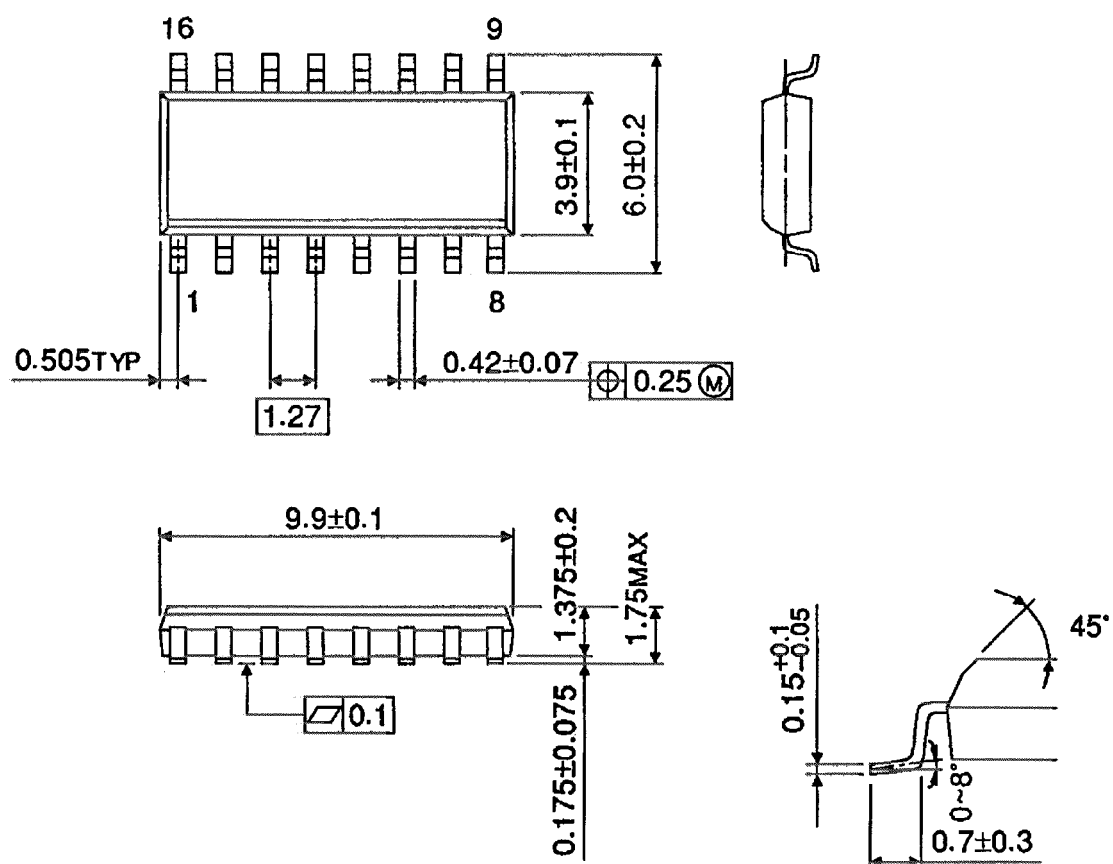


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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