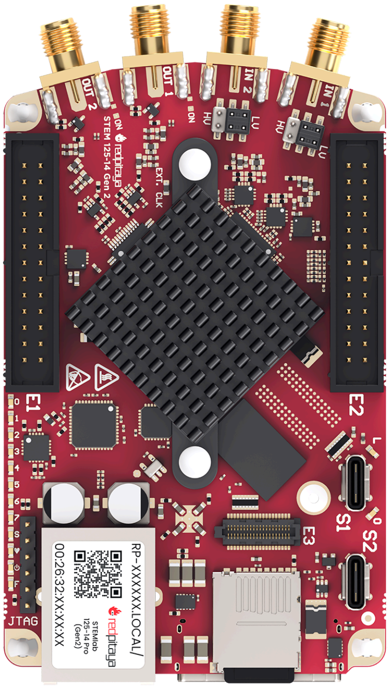
STEMlab 125-14 PRO Gen 2



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Overview

The STEMlab 125-14 PRO Gen 2 is a high-performance, versatile, and compact measurement and control platform designed for a wide range of applications in electronics, signal processing, and embedded systems development. It features a dual-core ARM Cortex-A9 processor, an FPGA AMD (Xilinx) Zynq 7010 SoC, and high-speed ADCs and DACs, making it suitable for tasks such as data acquisition, signal generation, and real-time processing.

Features

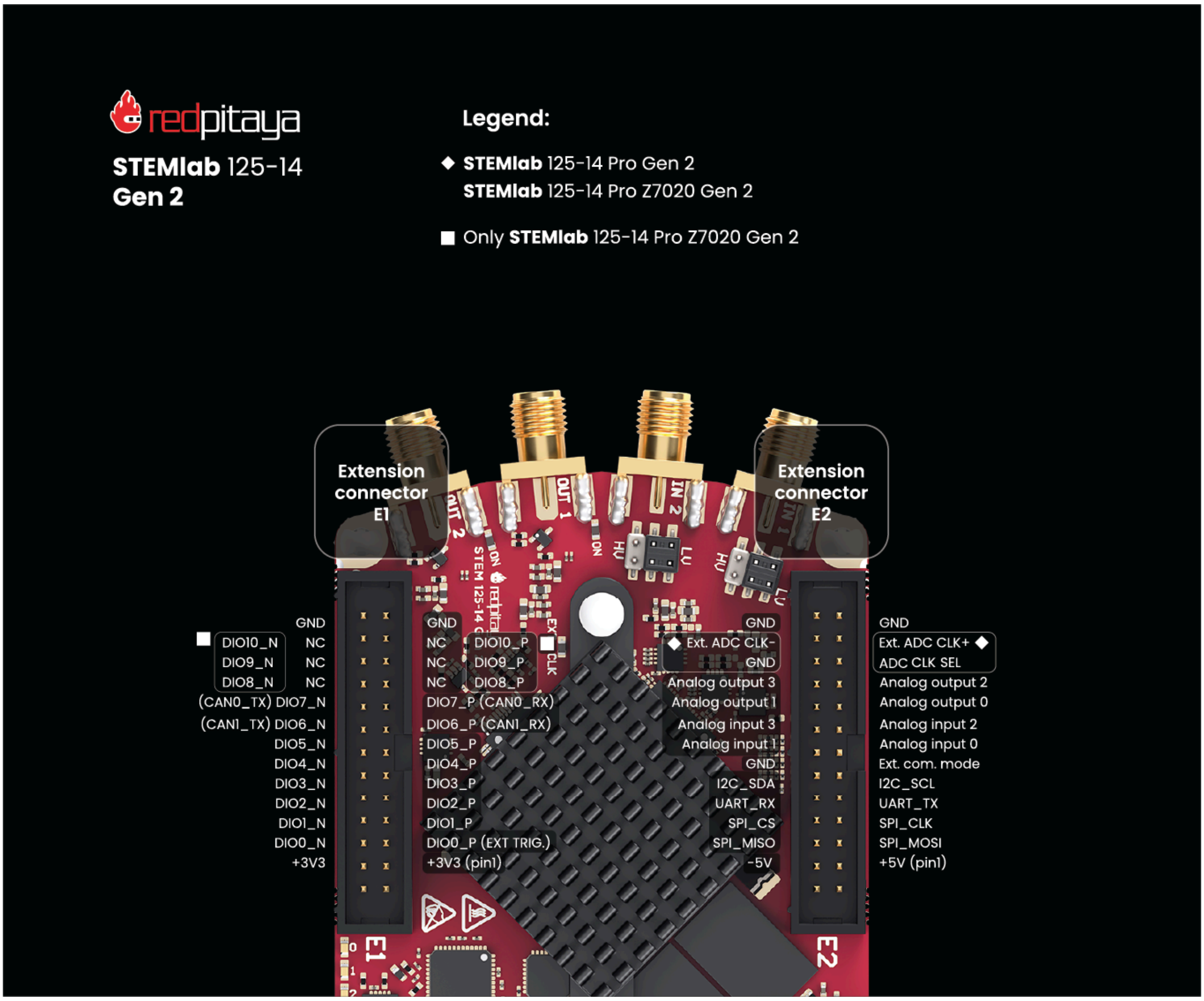
- Improved Gen 2 frontend architecture
- 14-bit, 125 MS/s ADC and DAC
- Dual-core ARM Cortex-A9 processor
- FPGA AMD (Xilinx) Zynq 7010 SoC
- 512 MB RAM
- 16 digital I/Os, 4 analog inputs, 4 analog outputs
- Multiple communication interfaces: I2C, SPI, UART, CAN
- USB-C connectivity for power and console
- External clock input support
- E3 connector for external QSPI/eMMC storage, power and watchdog control.

Quick Reference

Category	Key Specifications
ADC	2 channels, 14-bit, 125 MS/s, DC-50 MHz
DAC	2 channels, 14-bit, 125 MS/s, DC-50 MHz
Processor	Dual-core ARM Cortex-A9
FPGA	AMD Zynq 7010 SoC
RAM	512 MB
Digital I/O	16 GPIOs @ 3.3V

Category	Key Specifications
Analog I/O	4 inputs (12-bit), 4 outputs (8-bit)
Jitter Performance	20 ps RMS @ 40 MHz
Connectivity	Ethernet, USB-C, Extension connectors
Special Features	E3, External ADC clock

Board Layout & Pinout



The pinout diagram shows all external connectors including RF inputs/outputs (IN1, IN2, OUT1, OUT2) and extension connectors (E1, E2).

For other external connectors like S1 and S2 synchronisation coni
communication and ethernet ports please see the general Gen 2 p

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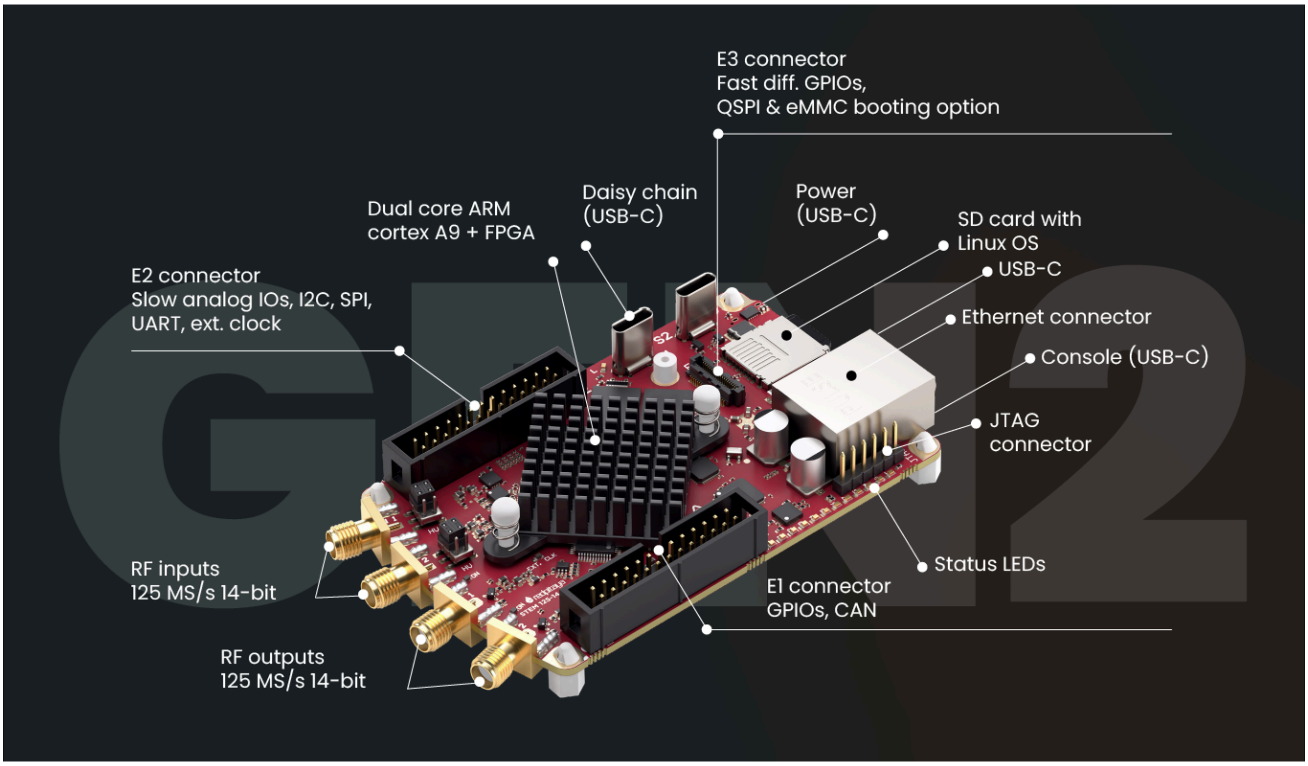

Technical Specifications

Parameter	Value
Basic	
Processor	Dual core ARM Cortex-A9
FPGA	FPGA AMD (Xilinx) Zynq 7010 SoC
RAM	512
Core clock frequency	125
System memory	Micro SD up to 32 GB
Serial console connector	USB-C
Power connector	USB-C
Power consumption	5 V, 3 A
Connectivity	
Ethernet	1
USB	USB-C 2.0
Wi-Fi	Requires Wi-Fi dongle

Parameter	Value
RF inputs	
RF input channels	2
Sampling rate	125
ADC resolution	14
Input impedance	1 MΩ / 10 pF
Full scale voltage range	±1 (LV) ±20 (HV)
Input coupling	DC
Absolute max. input voltage	±6 (LV) ±30 (HV)
Input ESD protection	1500
Overload protection	Protection diodes
Bandwidth	DC - 50
Connector type	SMA
RF outputs	
RF output channels	2
Sampling rate	125
DAC resolution	14
Load impedance	50 Ω / Hi-Z
Voltage range	±1 @ 50 Ω ±2 @ Hi-Z
Output coupling	DC
Short circuit protection	Yes
Output slew rate	2 V / 10 ns
RF output jitter @40 MHz	20
Bandwidth	DC - 50

Parameter	Value
Connector type	SMA
Extension connectors	
Digital GPIOs	16
Digital voltage levels	3.3
High-speed diff. pairs (E3)	N/A
High-speed diff. pair voltage levels (E3)	N/A
Analog inputs	4
Analog input voltage range	0 - 3.5
Analog input resolution	12
Analog input sampling rate	100
Analog outputs	4
Analog output voltage range	0 - 1.8
Analog output resolution	8
Analog output sampling rate	≲ 3.2
Analog output bandwidth	≈ 120
Communication interfaces	I2C, SPI, UART, CAN
Available voltages	±5, +3.3
External ADC clock	Yes
E3 connector	Yes
Synchronisation	
External trigger input	DIO0_P
External trigger input impedance	Hi-Z
Trigger output	DIO0_N
Daisy chain connectors (S1 & S2)	Yes
Daisy chain connectors speed	up to 500
Daisy chain connectors type	USB-C
Ref. clock input	N/A
Ref. clock frequency	N/A

Parameter	Value
Ref. clock connector type	N/A
Boot options	
SD card	Yes
QSPI	E3 add-on module
eMMC	E3 add-on module
Environmental Specifications	
Operating Temperature Range	0 to 55
Operating Humidity Range	< 90%
Automatic Shutdown Temperature	85
Dimensions	
Size (L x W x H)	106.8 x 60.0 x 17.9

See also

For more detailed information, please refer to the Gen 2 board comparison table.

Warning

Maximum Input Voltage

- **LV mode:** ±6 V absolute maximum
- **HV mode:** ±30 V absolute maximum

Exceeding these values may damage the board permanently.

Performance & Measurements

You can find the measurements of the fast analog frontend here:

- Gen 2 - STEMlab 125-14 Gen 2.

Schematics & 3D Models

Schematics

- Schematics_STEM_125-14_PRO_Gen2_V2r0_RevA.pdf.

Note

Full hardware schematics for the Red Pitaya board are not available. Red Pitaya has open-source code but not open hardware schematics. Nonetheless, development schematics are available. This schematic will give you information about hardware configuration, FPGA pin connections, and similar.

Mechanical Specifications & 3D Models

- STEP 3D_STEM_125-14-Pro-Gen2.zip.

Hardware Details

Components

The STEMlab 125-14 PRO Gen 2 uses high-performance analog components from Linear Technology (now Analog Devices) for the signal chain.

ADC: Analog Devices LTC2145-14

- Dual 14-bit, 125 MS/s ADC
- Low power consumption
- High dynamic range

DAC: Analog Devices AD9767

- Dual 14-bit, 125 MS/s DAC
- High SFDR performance
- Low power operation

FPGA: AMD (Xilinx) Zynq 7010

- Dual-core ARM Cortex-A9 @ 667 MHz
- Programmable logic fabric
- Integrated peripherals and memory controllers

Oscillator: SG3225VAN

- High-precision 125 MHz reference oscillator
- Low jitter performance

Extension Connectors & Interfaces

Overview

The STEMlab 125-14 PRO Gen 2 board features the following connectors and interfaces:

- **E1 and E2 connectors:** Primary expansion connectors with digital I/O, analog I/O, and communication interfaces. These connectors allow users to interface with additional hardware, sensors, or peripherals, enhancing the board's capabilities.
- **E3 connector:** Secondary expansion connector designed for high-speed differential pairs, QSPI/eMMC storage, power management, and watchdog control. This connector is ideal for advanced applications requiring additional storage or specialized interfaces.
- **S1 and S2 connectors:** Daisy-chain connectors for synchronizing multiple Red Pitaya boards. These connectors enable clock and trigger synchronization between boards.

Connector Physical Specifications

E1 and E2 Extension Connectors:

- Connector type: 2 x 13 pins IDC 2.54 mm pitch
- Pin count: 26 pins each (2x13 configuration)
- Pitch: 2.54 mm (0.1")

E3 Extension Connector:

- Connector type: 2 x 20 pins Micro Blade & Beam 0.50 mm pitch.
- Pin count: 40 pins (2x20 configuration)
- Pitch: 0.50 mm

Mating Connectors:

Note

When looking for mating connectors for custom Red Pitaya shields, double height elevated sockets are needed to clear the heatsink and ethernet connector on the board. Any connectors with *insulation height* of 0.635” (16.13 mm) or greater will work. This clearance requirement is based on the tallest components on the Red Pitaya board (heatsink and ethernet connector).

Note

To prevent damage to the board or the shield, when connecting shields to the E1 and E2 connectors, please ensure:

- **Proper alignment of connectors** - ensure the connectors are correctly aligned. The connectors on the Red Pitaya board have additional space in the socket housing, making it possible to misalign the shields by ±1 pin while still appearing physically connected. This can cause damage to the board and/or the shield, so please double-check the alignment before powering on the board.
- **Tight-fitting counterparts** - use connectors that fit securely to prevent accidental disconnections or damage.

E1 Connector - Digital I/O & CAN

The E1 extension connector provides digital I/O and CAN bus interfaces for control and communication applications.

Features:

- Two +3V3 power sources (max 0.5 A of current)
- 16 single-ended or 8 differential digital I/Os with 3.3 V logic level
- Two CAN buses (configurable via software)

Electrical Specifications:

All DIOx_y pins are LVCMOS33, with the following absolute maximum ratings:

- Min. voltage: -0.40 V
- Max. voltage: 3.3 V + 0.55 V
- Drive strength: < 8 mA

E1 Pinout:

Pin	Description	FPGA pin number	FPGA pin description
1	3V3		
2	3V3		
3	DIO0_P / EXT TRIG	G17	IO_L16P_T2_35
4	DIO0_N / TRIG OUT	G18	IO_L16N_T2_35
5	DIO1_P	H16	IO_L13P_T2_MRCC_35
6	DIO1_N	H17	IO_L13N_T2_MRCC_35
7	DIO2_P	J18	IO_L14P_T2_AD4P_SRCC_3
8	DIO2_N	H18	IO_L14N_T2_AD4N_SRCC_
9	DIO3_P	K17	IO_L12P_T1_MRCC_35
10	DIO3_N	K18	IO_L12N_T1_MRCC_35
11	DIO4_P	L14	IO_L22P_T3_AD7P_35
12	DIO4_N	L15	IO_L22N_T3_AD7N_35
13	DIO5_P	L16	IO_L11P_T1_SRCC_35
14	DIO5_N	L17	IO_L11N_T1_SRCC_35
15	DIO6_P / CAN1_RX	K16	IO_L24P_T3_AD15P_35
16	DIO6_N / CAN1_TX	J16	IO_L24N_T3_AD15N_35
17	DIO7_P / CAN0_RX	M14	IO_L23P_T3_35
18	DIO7_N / CAN0_TX	M15	IO_L23N_T3_35
19	NC		
20	NC		
21	NC		

Pin	Description	FPGA pin number	FPGA pin description
22	NC		
23	NC		
24	NC		
25	GND		
26	GND		

Note

To change the functionality of DIO6_P, DIO6_N, DIO7_P and DIO7_N from GPIO to CAN, please modify the **housekeeping** register value at **address 0x34**. For further details, please refer to the FPGA register section.

The change can also be performed with the appropriate SCPI or API command. Please refer to the CAN commands section for further details.

E2 Connector - Analog & Communication

The E2 extension connector provides analog I/O and communication interfaces for sensor integration and data acquisition.

Features:

- ±5 V power sources (max 0.5 A for +5 V, max 0.1 A for -5 V)
- SPI, UART, I2C communication interfaces
- 4 slow ADCs (12-bit, 100 kS/s)
- 4 slow DACs (8-bit PWM, ≲ 3.2 MS/s)
- External clock input capability

E2 Pinout:

Pin	Description	FPGA pin number	FPGA pin description
1	+5V		

Pin	Description	FPGA pin number	FPGA pin description
2	-5V		
3	SPI (MOSI)	E9	PS_MIO10_500
4	SPI (MISO)	C6	PS_MIO11_500
5	SPI (SCK)	D9	PS_MIO12_500
6	SPI (CS)	E8	PS_MIO13_500
7	UART (TX)	D5	PS_MIO8_500
8	UART (RX)	B5	PS_MIO9_500
9	I2C (SCL)	B13	PS_MIO50_501
10	I2C (SDA)	B9	PS_MIO51_501
11	Ext com. mode (AIN)		
12	GND		
13	Analog Input 0	B19, A20	IO_L2P_T0_AD8P_35, IO_I
14	Analog Input 1	C20, B20	IO_L1P_T0_AD0P_35, IO_L
15	Analog Input 2	E17, D18	IO_L3P_T0_DQS_AD1P_35
16	Analog Input 3	E18, E19	IO_L5P_T0_AD9P_35, IO_I
17	Analog Output 0	T10	IO_L1N_T0_34
18	Analog Output 1	T11	IO_L1P_T0_34
19	Analog Output 2	P15	IO_L24P_T3_34
20	Analog Output 3	U13	IO_L3P_T0_DQS_PUDC_B
21	ADC CLK Sel.		
22	GND		
23	Ext. ADC Clk+ [4]	U18	IO_L12P_T1_MRCC_34
24	Ext. ADC Clk- [4]	U19	IO_L12P_T1_MRCC_34
25	GND		
26	GND		

E3 Connector - QSPI/eMMC & Power Control

The E3 extension connector provides external boot storage interfaces (QSPI/eMMC), power management, and watchdog control for mission-critical applications.

Features:

- QSPI Flash interface (6 pins) for external boot
- eMMC interface (6 pins) for external boot
- I2C communication (SCL, SDA)
- Power control signals (shutdown, watchdog kick)
- Boot mode selection (SDIO_SEL)
- 5V power supply pins

Electrical Specifications:

All E3 pins are LVCMOS33 (3.3V), with the following absolute maximum ratings:

- Abs. Min. voltage: -0.40 V
- Abs. Max. voltage: 3.3 V + 0.55 V
- Voltage levels: 3.3 V

E3 Pinout:

Pin	Description	FPGA pin number	FPGA pin description	Voltage l
1	I2C0_SCL			3V3
3	PS_POR#	C7	PS_POR_B_500	3V3
5	PWR_ON			3V3
7	NC			
9	NC			
11	NC			
13	NC			
15	NC			
17	NC			
19	NC			

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Pin	Description	FPGA pin number	FPGA pin description	Voltage l
21	NC			
23	NC			
25	NC			
27	NC			
29	NC			
31	NC			
33	NC			
35	NC			
37	NC			
39	+5V			

Note

Boot Mode Selection:

The **SDIO_SEL** pin (pin 6) controls the boot source:

- **Low (GND):** Boot from SD card (default)
- **High (3.3V):** Boot from external QSPI or eMMC

The boot mode must be set before powering on the board.

Important

E3 Add-on Module Required:

External boot storage (QSPI/eMMC) requires an E3 add-on module with the appropriate storage chips. See E3 Add-on board for details.

Auxiliary Analog Inputs & Outputs

Auxiliary Analog Input Channels

The E2 connector provides 4 auxiliary analog inputs for slow-speed measurements and sensor interfacing.

Parameter	Value	Units	Notes
Number of channels	4	-	
ADC resolution	12	bit	
Sampling rate	100	kS/s	[7]
Input filter bandwidth	120	kHz	
Input voltage range	0 - 3.5	V	
Input coupling	DC	-	
Connector	Extension connector E2 connector	-	Pins 13,

Auxiliary Analog Output Channels

The E2 connector provides 4 auxiliary analog outputs using PWM with low-pass filtering.

Parameter	Value	Units	Note
Number of channels	4	-	
Output resolution	8	bit	
Sampling rate	≲ 3.2	MS/s	
Output filter bandwidth	200	kHz	
Output voltage range	0 - 1.8	V	
Output coupling	DC	-	
Output type	Low pass filtered PWM	-	[8]
PWM time resolution	8 ns	ns	(1/125
Connector	Extension connector E2 connector	-	Pins 1

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General Purpose Digital I/O Channels

Parameter	Value	Units	Notes
Number of GPIOs	16	-	
Digital voltage level	3.3	V	
Abs. min. voltage	-0.40	V	
Abs. max. voltage	3.3 + 0.55	V	
Current limitation	< 8	mA	Drive stre
Direction	Configurable	-	
Time resolution	8 ns	ns	(1/125 MH
Connector location	Extension connector E1 connector	-	

Synchronisation Connectors (S1 & S2)

The USB-C S1 and S2 connectors enable daisy chaining of multiple Red Pitaya boards for synchronized multi-channel applications.

S1 Connector (Transmit): Used exclusively for transmitting clock and trigger signals from the current board to the next board in the chain.

S2 Connector (Receive): Used exclusively for receiving clock and trigger signals from the previous board in the chain.

Important

S1 and S2 are NOT standard USB-C ports!

The connectors S1 and S2 are used **only for interconnection between Red Pitaya modules**. The connection is not compliant with USB-C specification.

Do not connect S1 or S2 to any other USB-C ports except Red Pit connectors (USB ports are DC coupled).

S1 Connector (Transmit)

Pin	USB-C Signal	Description	FPGA pin number	FPGA pin descri
A1	GND			
A2	TX1+	Daisy_IO0_P	T12	IO_L2P_T0_34
A3	TX1-	Daisy_IO0_N	U12	IO_L2N_T0_34
A4	VBUS	[9]		
A5	CC1	S1_Orient [10]	W6	IO_L22N_T3_13
A6	D1+	D2+		
A7	D1-	D2-		
A8	SBU1	NC		
A9	VBUS	[9]		
A10	RX2-	NC		
A11	RX2+	NC		
A12	GND			

S2 Connector (Receive)

Pin	USB-C Signal	Description	FPGA pin number	FPGA pin descri
A1	GND			
A2	TX1+	NC		
A3	TX1-	NC		
A4	VBUS	[9]		
A5	CC1	[11]		
A6	D1+	D2+		
A7	D1-	D2-		

Pin	USB-C Signal	Description	FPGA pin number	FPGA pin descri
A8	SBU1	NC		
A9	VBUS	[9]		
A10	RX2-	Daisy_IO3_N		
A11	RX2+	Daisy_IO3_P		
A12	GND			

Advanced Features

Power Supply

Red Pitaya Gen 2 boards support two physical power inputs:

1. **USB-C connector**
2. **+5V pin (pin 1) and GND pin (pin 25,26) on the |E2| connector**

The sections below describe the supported powering scenarios and their implications.

External Power Specifications:

Parameter	Specification
Power supply voltage	5 V
Maximum current draw	3.0 A
Power supply type	DC
Abs. max. voltage	5.5 V
Abs. min. voltage	4.5 V

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Note

The board’s maximum current draw is 3.0 A. The power supply may have a higher current rating — this will not cause any issues.

Note

Why is power protection implemented? The USB-C protection circuit was introduced because boards were being powered from computer USB ports, which typically provide 0.5–0.9 A — insufficient for reliable operation and likely to cause reboots and network disconnections.

Powering scenario 1 — Recommended: USB-C with a standard USB-C power supply

Connect a USB-C power supply (5 V, 3 A) with functional CC lines to the USB-C connector. Leave jumper **JP5 unbridged** (default).

- The USB-C protection circuit detects the CC lines and confirms the supply is USB-C compliant.
- The **Power Error LED remains off**, indicating normal operation.
- Full overcurrent protection (3.0 A PTC resettable fuse) is active.

Note

A USB-C power supply without CC lines (e.g. a simple 2-wire USB-C cable with a generic 5 V adapter) will **not** satisfy the protection circuit and will cause the Power Error LED to light up, as described in scenario 2b below.

Powering scenario 2 — Alternative: 2-pin (non-USB-C) power supply

If a 2-wire 5 V power supply is used (no CC lines), there are two connection options:

2a — Via the E2 connector (+5V pin)

Connect the supply directly to pin 1 (+5V) and pin 25/26 (GND) on the E2 connector connector. The JP5 jumper state does not matter in this case.

- The USB-C protection logic is entirely bypassed — the protection circuit is not in the power path.

- The 3.0 A PTC resettable fuse on the E2 connector +5V pin remains active for overcurrent protection.
- The **Power Error LED will be on**, because the USB-C protection circuit receives board power but no CC line signal.

2b — Via the USB-C connector

Connect the 2-wire supply through the USB-C connector. **JP5 must be bridged** to allow power flow in this configuration.

- The USB-C protection circuit is in the power path and receives power, but receives no CC line signal.
- The **Power Error LED will be on** — this is expected behaviour, not a fault.
- It is the user's responsibility to verify that the supply provides a stable 5 V at up to 3 A.

Warning

When using scenario 2 (either sub-option), the **Power Error LED being on is expected and does not indicate a hardware fault**. It indicates that the USB-C protection circuit cannot verify the connected supply's compliance. The user must ensure the supply meets the 5 V / 3 A specification independently.

Available Power Rails on Extension Connectors:

The E1 connector and E2 connector connector expose several power rails that can be used to supply power to **external devices or circuits connected to the board**. The current limits below are the maximum currents that Red Pitaya can source from each rail to external loads — they are not related to the board's own power consumption.

Voltage Rail	Max. Sourceable Current
+5 V	0.5 A [12]
-5 V	0.1 A
+3V3	0.5 A [12]

Note

Exceeding these limits may cause voltage rail instability or trigger the board's protection circuitry, which can result in a board reset or shutdown.

The +5V pin on E2 connector (pin 1) also serves as a power input when using powering scenario 2a. In that role it is protected by a 3.0 A PTC resettable fuse located on the PCB near the E2 connector connector.

External ADC Clock

The main ADC, DAC, and FPGA CLK signal can be supplied from an external source through the **Ext. ADC Clk±** ports on the E2 connector connector.

Clock Selection

Both the internal oscillator clock and the external clock signal are connected to the NB6L72 Differential Crosspoint Switch. The **CLK_SEL** pin (pin 21 on E2 connector) is used to select the clock source:

- **3V3 (logic high) or unconnected:** Internal clock (default), supplied from the onboard oscillator.
- **GND (logic low):** External clock, supplied through the Ext. ADC Clk± ports.

Signal Path

The clock signal travels from the output of the NB6L72 through the ADC to the FPGA and DAC, ensuring consistent timing across the signal acquisition path.

External Clock Specifications

The external ADC clock should comply with NB6L72 input specifications:

Parameter		Description
	Clock input pins	23 (Clk+) and 24 (Clk-) on E2 connec
	Input standards	LVPECL, CML, LVDS, LVCMOS, LVTTL
	Input clock coupling	AC (on-board capacitors)
f_{CLK}	Input frequency range	
$V_{ID,DIFF,PP}$	Input voltage swing	Differential peak-to-peak

Parameter	Description	
IDC	Input clock duty cycle	

Note

The typical operating frequency depends on the board variant:

- **STEMlab 125-14 Gen 2 boards:** 125 MHz

Operating outside the board's specified frequency is possible but voids all performance guarantees. See the warning below.

Note

The board includes AC coupling capacitors on the external clock inputs, so the input signal must have sufficient amplitude and slew rate to meet the NB6L72 input specifications after AC coupling.

For further information on voltage levels and timing requirements, please refer to the NB6L72 datasheet.

Warning

Not a reference clock input: The Ext. ADC Clk± ports are not a reference clock input for a PLL or any other timing circuit. They directly drive the main sampling clock for the ADC, DAC, and FPGA. Connecting a reference clock signal intended for a PLL will not function as expected.

Warning

Changing the external clock frequency during operation is not supported.

The Zynq 7010/7020 PL uses Mixed-Mode Clock Managers (MMCMs) and PLLs to derive internal fabric clocks from the input clock. Changing the external clock frequency during operation will cause the MMCM/PLL to lose lock, resulting in undefined output clocks and acquisition/generation errors. A full FPGA reset or reconfiguration is required after any clock frequency change.

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Note

Operating at non-standard clock frequencies:

The Red Pitaya FPGA is designed, tested, and guaranteed to operate correctly at the board's specified core clock frequency (125 MHz for STEMlab 125-14, 122.88 MHz for SDRlab 122-16, etc).

While it is possible to run the board at different clock frequencies, please be aware that:

1. **FPGA functionality:** The official FPGA configuration may not function as intended at non-standard frequencies and requires thorough testing
2. **Sampling rates:** The ADC and DAC sampling rates will change proportionally with the clock frequency
3. **Analog bandwidth:** The analog bandwidth of the board will change with the clock frequency
4. **Absence of external clock:**

   - **OS 2.07-48 or higher:** If no valid external clock is present, the PS side will boot using an internal 33 MHz oscillator, but the FPGA will not operate (no signal acquisition/generation functionality)
   - **OS versions prior to 2.07-48:** The board will fail to boot (stuck in reboot cycle) if no valid external clock is detected

Note

Advanced: Dynamic clock reconfiguration

The standard Red Pitaya FPGA bitstream does not implement the Dynamic Reconfiguration Port (DRP) interface that AMD (Xilinx) provides for runtime MMCM/PLL reconfiguration. A custom FPGA design using DRP-based MMCM reconfiguration with active lock monitoring could theoretically support runtime clock frequency changes, but this requires extensive FPGA development and verification. The PS side (ARM/Linux) is not affected by clock changes, as it runs from its own independent 33 MHz crystal-derived PLL.

Note

When synchronising multiple Red Pitaya boards, please keep in mind that:

- X-channel 2.0 synchronisation (Click Shields) works out-of-the-box
- X-channel synchronisation requires a hardware modification as secondary boards differ from the primary board

External Booting Options

The E3 connector on the STEMlab 125-14 PRO Gen 2 and STEMlab 125-14 PRO Z7020 Gen 2 provides pins for connecting **external QSPI** (SFSPI pins) or **eMMC** (EMMC pins) storage devices.

These storage chips should be located on an external module (for example, the E3 Add-on board).

For information on how to configure the boot mode, please refer to the External Booting Options section.

Boot Mode Selection

Note

More information regarding booting the Red Pitaya board from external storage will be provided in future documentation updates.

E3 Boot Interface Pins

QSPI Flash Pins (SFSPI):

Pin	Signal	FPGA Pin	Description
28	SFSPI_IO3	A6 (PS_MIO5_500)	Data line 3
30	SFSPI_IO2	B7 (PS_MIO4_500)	Data line 2
32	SFSPI_IO1	D6 (PS_MIO3_500)	Data line 1
34	SFSPI_IO0	B8 (PS_MIO2_500)	Data line 0
36	SFSPI_CS#	A7 (PS_MIO1_500)	Chip select
38	SFSPI_SCK	A5 (PS_MIO6_500)	Clock

eMMC Pins:

Pin	Signal	FPGA Pin	Description
10	EMMC_CMD	C17 (PS_MIO41_501)	Command line
12	EMMC_DAT3	B15 (PS_MIO45_501)	Data line 3
14	EMMC_DAT2	F13 (PS_MIO44_501)	Data line 2
18	EMMC_DAT1	A9 (PS_MIO43_501)	Data line 1
20	EMMC_DAT0	E12 (PS_MIO42_501)	Data line 0
24	EMMC_CLK	D14 (PS_MIO40_501)	Clock

Control & Power Pins:

Pin	Signal	FPGA Pin	Description
2	E3_SHDN	E6 (PS_MIO0_500)	Module shutdown
4	E3_WDT_KICK	D8 (PS_MIO7_500)	Watchdog kick
6	SDIO_SEL [4]	D16 (PS_MIO46_501)	Boot mode select
39, 40	+5V	-	Power supply

Note

More information regarding booting the Red Pitaya board from external storage will be provided in future documentation updates.

Calibration

Red Pitaya Gen 2 boards are factory-calibrated. Recalibration may be required after extended use, environmental changes, or when measurement accuracy degrades.

There are three ways to calibrate the board:

- Calibration application — graphical interface accessible from the *System Tools* menu. Recommended for most users.
- Calibration command line utility (calib) — command line tool for scripted or advanced calibration workflows.
- C++ or Python API commands — programmatic access to calibration parameters.

For a full description of the calibration procedure, required equipment, and technical reference, please refer to the Calibration documentation.

> **Note**
>
> Gen 2 boards do not require 50 Ω terminators during calibration, unlike the original generation boards. The improved analog front-end circuitry eliminates this requirement.

Additional Resources

For additional specifications and measurements, please refer to:

- Gen 2 hardware specifications - Common Gen 2 specifications
- Gen 2 board comparison table - Comparison across all Red Pitaya Gen 2 models
- E3 module specifications - Detailed E3 module specifications

Legal & Disclaimers

> **Note**
>
> The information provided by Red Pitaya d.o.o. is believed to be accurate and reliable. However, no liability is accepted for its use. Please note that the contents may be subject to change without prior notice.

Footnotes

[1]

The absolute maximum input voltage values are for frequencies below 1 kHz. For higher frequencies, please use the input voltage range specifications as **Absolute maximum**.

[2]
See the X-channel 2.0 (Click Shield) synchronisation and X-channel 2.0 (Click Shield) synchronisation examples for trigger output configuration.

[3]
Not compatible with USB-C standard (DC-coupled). Use only for daisy-chaining multiple Red Pitaya boards.

[4] (1,2,3)
The external ADC clock goes first to the NB6L72 clock selector chip, then passes through the ADC to finally reach the FPGA pins.

[5] (1,2,3)
For exact voltage levels, please refer to the NB6L72 datasheet.

[6]
Negative logic in the FPGA.

[7]
The default software enables sampling at a CPU-dependent speed. To acquire data at a 100 kS/s rate, additional FPGA processing must be implemented.

[8]
The output is passed through a first-order low-pass filter. Should additional filtering be required, this can be applied externally in line with the specific requirements of the application.

[9] (1,2,3,4,5,6,7,8)
VBUS connectors are connected together on the board. They are not connected to the board power supply.

[10] (1,2)
On the S1 connector, the CC1 pin is connected to the Orient LED and to the S1_ORIENT FPGA pin (via resistor divider to reduce the voltage levels to 2V5). CC1 and CC2 pins are connected to an XOR gate which determines the state of the **Link LED**. The output of the XOR gate is also connected to the S1_LINK FPGA pin (via resistor divider to reduce the voltage levels to 2V5).

[11]

On the S2 connector, the CC1 pin is protected with a Zener diode to 3V3, but is not connected to the FPGA. CC2 pin is not connected.

[12] (1,2)
Application specific. The output current is shared between the extension connectors and the connected USB devices, and can be higher if other peripheral units are not in use.