Si53159-EVB

Si53159 Evaluation Board User's Guide

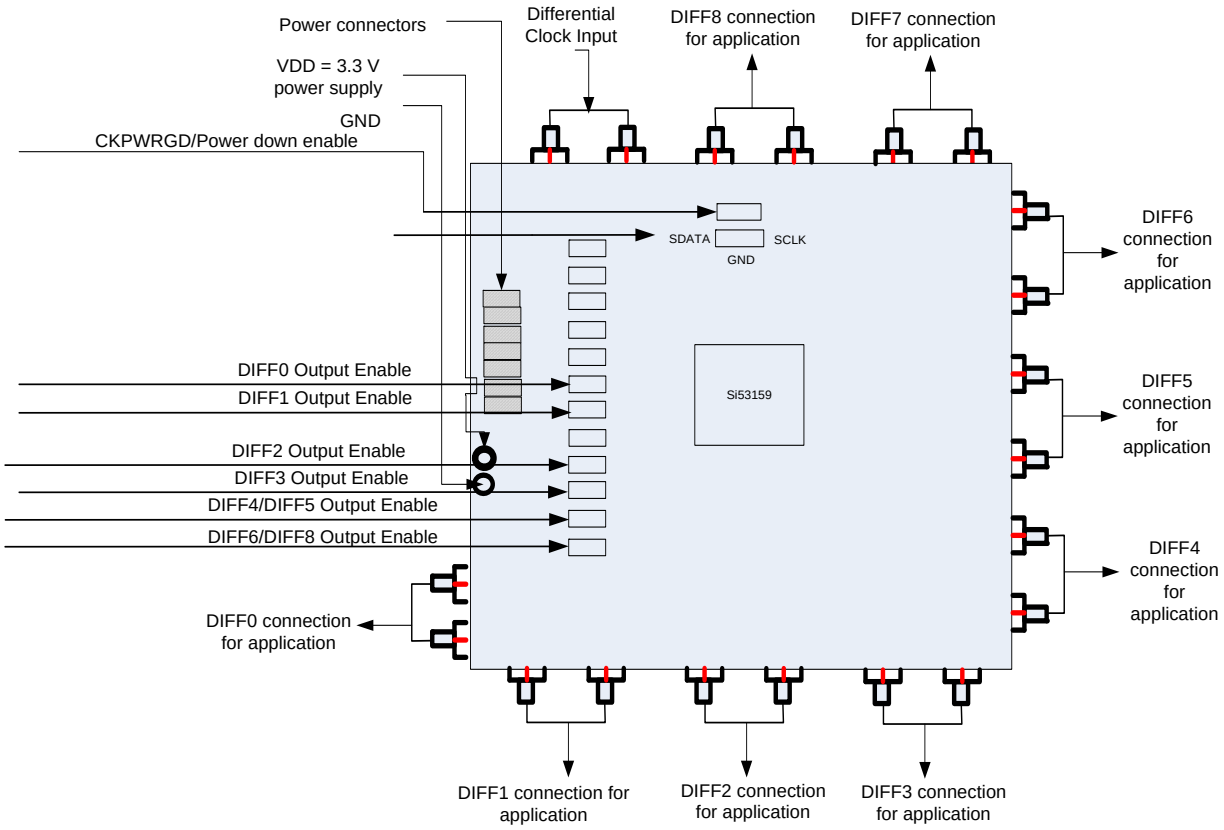
Description

The Si53159 is a nine port PCIe clock buffer compliant to the PCIe Gen1, Gen2 and Gen3 standards. The Si53159 is a 48-pin QFN device that operates on a 3.3 V power supply and can be controlled using SMBus signals along with hardware control input pins. The device is spread aware and accepts frequency spread differential clock frequency range from 100 to 210 MHz. The connections are described in this document.

EVB Features

This document is intended to be used in conjunction with the Si53159 device and data sheet for the following tests:

- PCIe Gen1, Gen2, Gen3 compliancy
- Power consumption test
- Jitter performance
- Testing out I^2C code for signal tuning
- In-system validation where SMA connectors are present



1. Front Panel

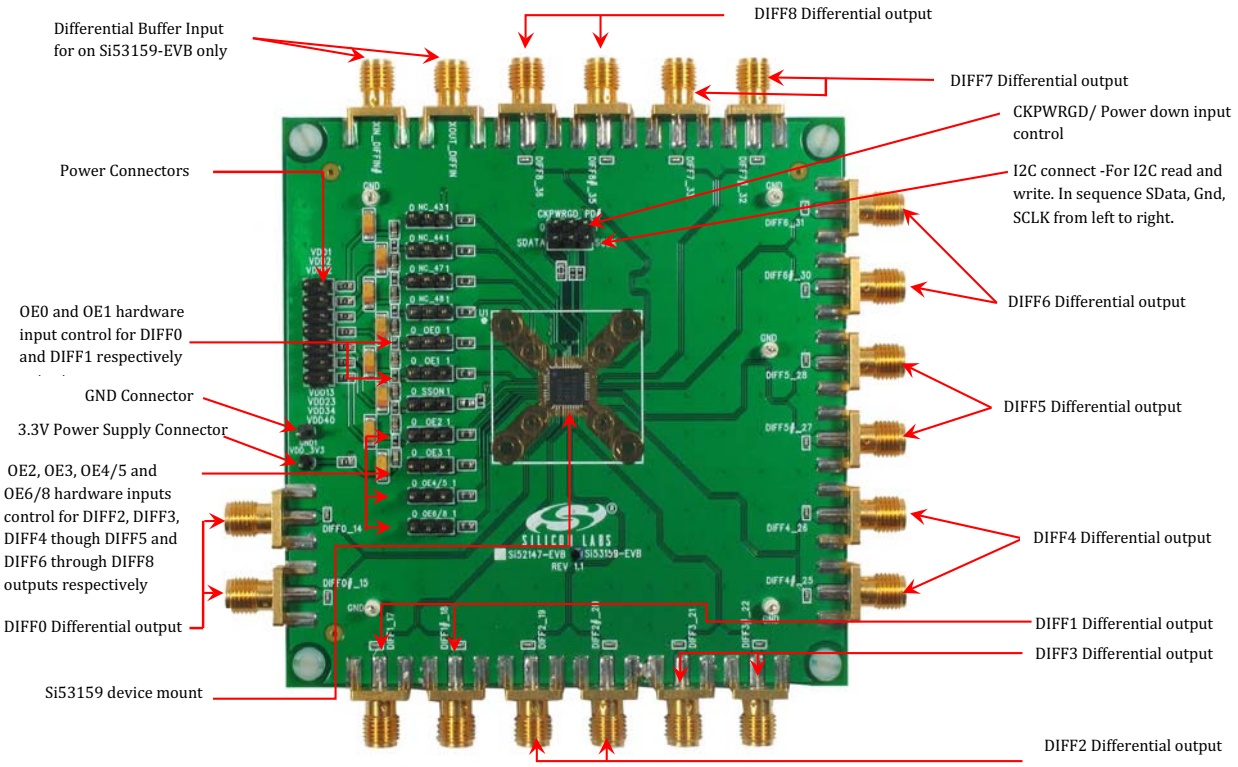


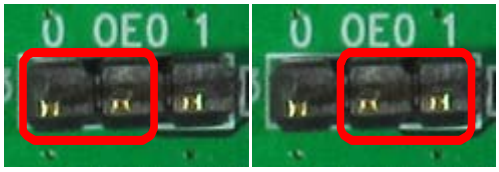
Figure 1. Evaluation Module Front Panel

Table 1. Input Jumper Settings

Jumper Label	Type	Description
OE0	I	**OE0, 3.3 V Input for Enabling DIFF0 Clock Output**. 1 = DIFF0 enabled, 0 = DIFF0 disabled.
OE1	I	**OE1, 3.3 V Input for Enabling DIFF1 Clock Output**. 1 = DIFF1 enabled, 0 = DIFF1 disabled.
OE2	I	**OE2, 3.3 V Input for Enabling DIFF2 Clock Output**. 1 = DIFF2 enabled, 0 = DIFF2 disabled.
OE3	I	**OE3, 3.3 V Input for Enabling DIFF3 Clock Output**. 1 = DIFF3 enabled, 0 = DIFF3 disabled.
OE4/5	I	**OE4/5, 3.3 V Input for Enabling DIFF4 and DIFF5 Clock Outputs.** 1 = DIFF4 & DIFF5 enabled, 0 = DIFF4 & DIFF5 disabled.
OE6/8	I	**OE6/8, 3.3 V Input for Enabling DIFF6, DIFF7 and DIFF8 Clock Outputs.** 1 = DIFF6, DIFF7 & DIFF8 enabled, 0 = DIFF6, DIFF7 & DIFF8 disabled.
CLKPWGD/$\overline{PD}$	I	**3.3 V LVTTL Input.** After CLKPWGD (active high) assertion, this pin becomes a real-time input for asserting power down (active low).
SDATA	I/O	**SMBus-Compatible SDATA**.
SCLK	I	**SMBus-Compatible SCLOCK**.

1.1. Generating DIFF Outputs from the Si53159

Upon power-on of the device if the differential input is applied and input pins are left floating, by default all DIFF outputs DIFF[0:8] are ON. The input pin headers have clear indication of jumper settings for setting logic low (0) and high (1) as shown in the figure below, the jumper placed on the middle and left pin will set input OE0 to low; and jumper placed on the middle and right pin will set input OE0 to high.



The output enable pins can be changed on the fly to observe outputs stopped cleanly. Input functionality is explained in detail below.

1.1.1. OE [0:8] Inputs

The output enable pins can change on the fly when the device is on. Deasserting (valid low) results in corresponding DIFF output to be stopped after their next transition with final state low/low. Asserting (valid high) results in corresponding output that was stopped are to resume normal operation in a glitch-free manner.

Each of the hardware OE [0:8] pins are mapped via I^2C to control bit in Control register. The hardware pin and the Register Control Bit both need to be high to enable the output. Both of these form an “AND” function to disable or enable the DIFF output. The DIFF outputs and their corresponding I^2C control bits and hardware pins are listed in Table 2.

Table 2. Output Enable Control

I^2C Control Bit	Output	Hardware Control Input
Byte1 [bit 4]	DIFF0	OE0
Byte1 [bit 2]	DIFF1	OE1
Byte2 [bit 1]	DIFF2	OE2
Byte2 [bit 0]	DIFF3	OE3
Byte1 [bit 7]	DIFF4	OE4/5
Byte1 [bit 6]	DIFF5	OE4/5
Byte2 [bit 5]	DIFF6	OE6/8
Byte2 [bit 4]	DIFF7	OE6/8
Byte2 [bit 3]	DIFF8	OE6/8

2. Schematics

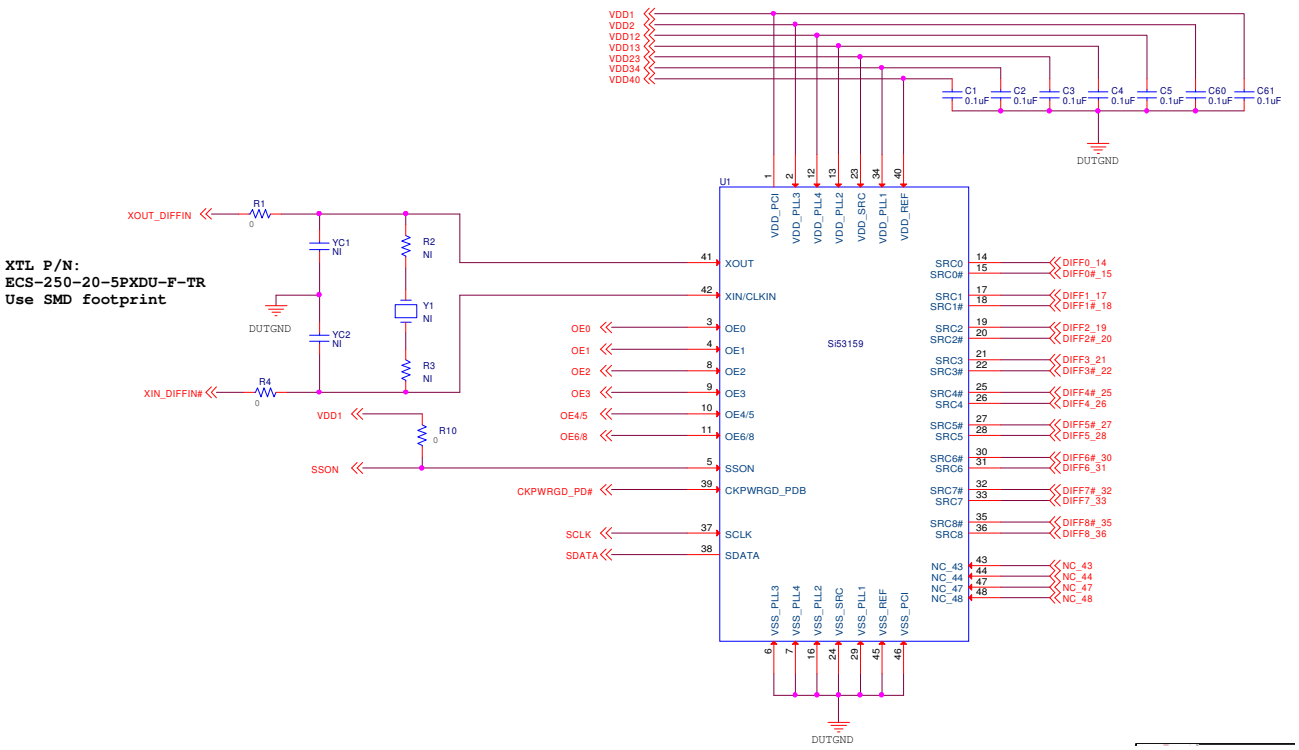


Figure 2. QFN-48 Device Connection

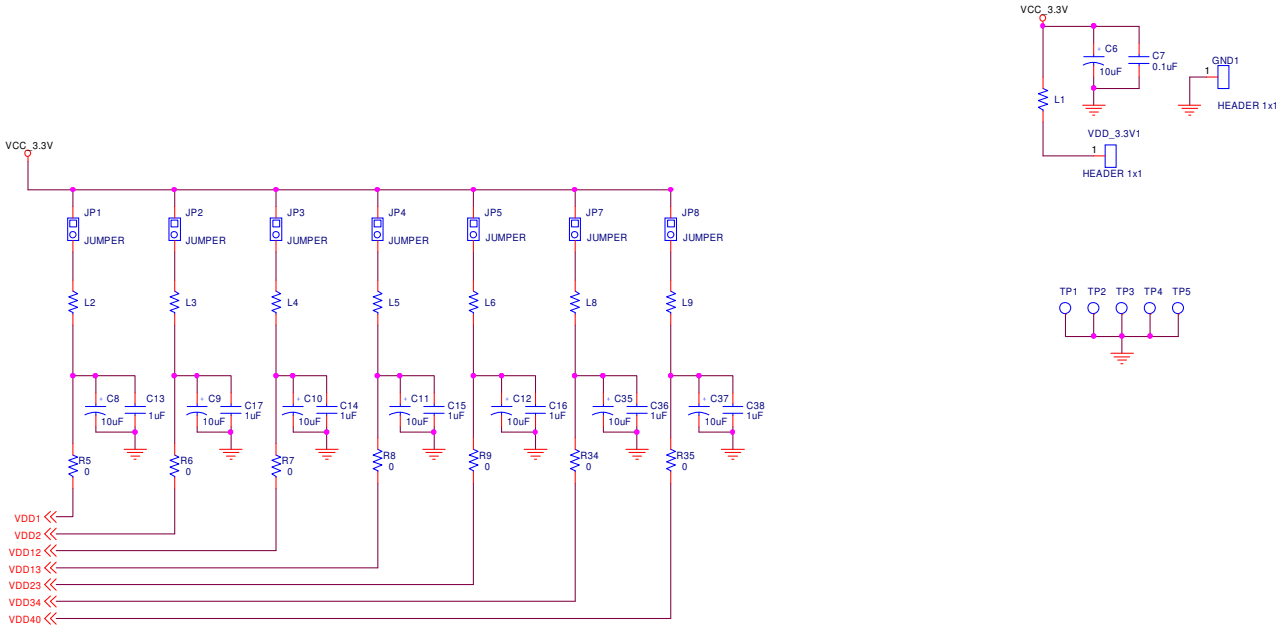


Figure 3. Device Power Supply

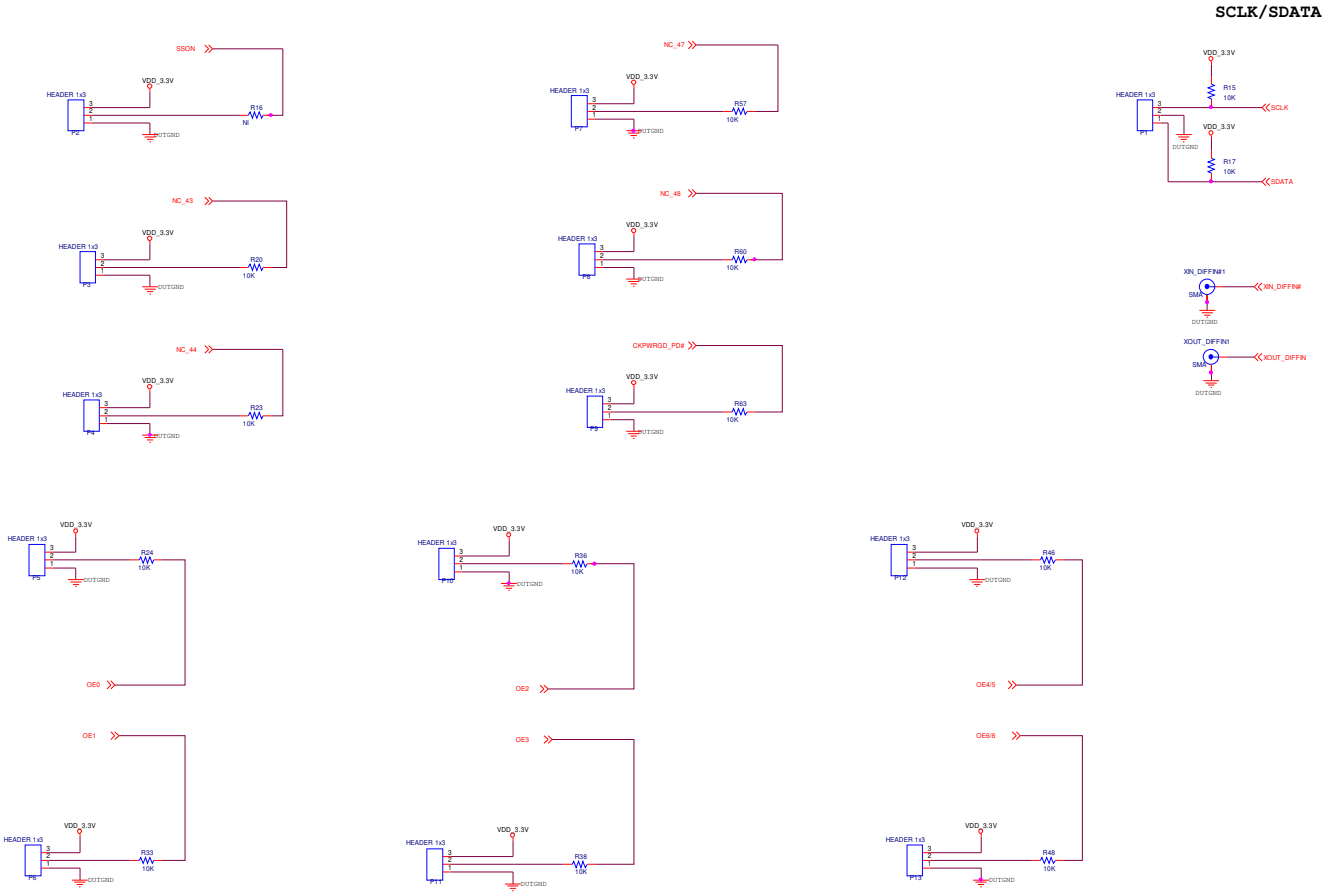


Figure 4. Clock and Control Signals

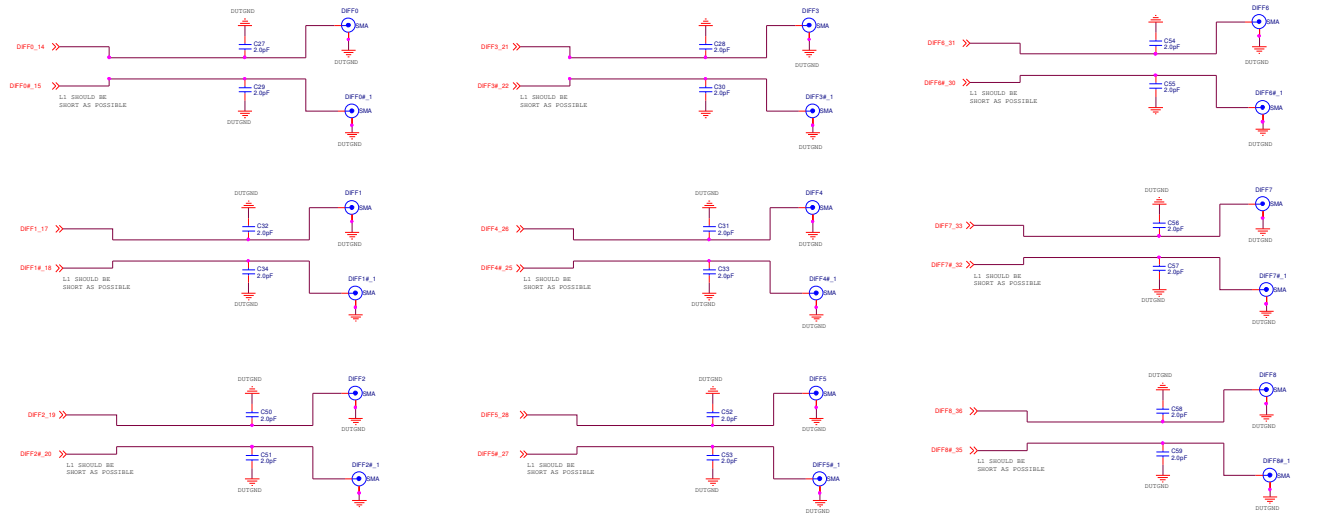


Figure 5. Differential Clock Signals

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