SP Industrial
Reliable Embedded Partner

Datasheet

Industrial DRAM

DDR4 SODIMM Series

Specifications Overview

- **Capacity**
  - 2GB, 4GB, 8GB, 16GB, 32GB
- **Form Factor**
  - DDR4 SODIMM
- **Performance**
  - 2400 = 19.2GB/s
  - 2666 = 21.3 GB/s
  - 3200 = 25.6 GB/s
- **Temperature Range**
  - Operation temperature:
    Normal temperature: -20°C ~ 95°C
    Wide temperature: -40° ~ 105°C
- **Power Consumption**
  - Supply Voltage: DC +1.2V ± 5%
- **Compliant Specifications**
  - RoHS
- **Feature Support**
  - Anti-Sulfur Resistant (Optional)

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Revision	Date	Description
1.0	2017/12	First Release
1.1	2018/3	Add 512Mx16 Solution
1.2	2018/7	Add Wide Temp Series
1.3	2019/6	Add 256Mx16, DDR4-2666 Products
1.3a	2019/9	Modify Part Number
1.4	2019/11	Add 8GB 512Mx8 Solution
1.5	2020/03	Change Industrial Cover Page Add New Part Number And Thermal Sensor Description
1.6	2020/06	Add 32GB 2Gx8 Solution
1.7	2020/09	Add 4GB, DDR4-2666 Solution; DDR4-3200_1Gx8 Solution
1.8	2021/08	Update Data Transfer Rates Add IDD/ IPP Info
1.9	2022/02	Add New PN Of 32GB 2Gx8 Solution Remove SP004GISF*240CS0, SP016GISF*240BS0
2.0	2022/05	Optimize Temperature Description
2.1	2022/09	Update Reliability MTBF Specification
2.2	2023/01	Remove SFV/ SFF section Remove P/N: SP004GISFU240NH0, SP008GISFU240NH0, SP008GISFU266BS0 SP016GISFU266BS0, SP016GISFU266BH0, SP032GISFU266FS0 Add P/N: SP004GISFU266NM0 (TBD), SP004GISFU320NM0 (TBD) Remove P/N: SP004GISFE240NH0, SP004GISFE266NH0, SP004GISFE266NS0 SP008GISFE266BS0, SP008GISFE266BH0, SP016GISFE266BS0 SP016GISFE266BH0, SP032GISFE266FS0
2.3	2023/05	Add 4GB IDD/ IPP Specification
2.4	2023/05	Add P/N SP004GISFU240NH0
2.5	2023/11	Update Temperature
2.6	2023/12	Update Temperature
2.7	2024/07	Add P/N SP008GISFU240BH0; SP016GISFU266FH0
2.8	2024/09	Adjust Format & Add E-DIE Order Info
2.8a	2024/12	Update Temperature Information
2.9	2025/1	Revise 1.2 Features Update Order Information
3.0	2025/8	Update Order Information
3.1	2025/8	Update Order Information
3.2	2025/11/26	Update Datasheet Format
3.3	2025/12/11	Update Order Information
3.4	2026/04/24	Add Samsung Solution Remove P/N: SP016GISFU320BN0, SP016GISFV320BN0 Update Specifications Overview

		Update Order Information

1. Product Description

1.1 Overview

Silicon Power Computer & Communications industrial DRAM products are JEDEC standard 260-Pin low power Double Data Rate 4 (DDR4) Synchronous DRAM Small Outline Dual In-Line Memory Module (SODIMM). DDR4 SODIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint. It is commonly used as the main memory in computers and other devices due to its cost-effectiveness and relatively high speed.

1.2 Features

- Fast data transfer rates:

Module Transfer Rates	Supported Transfer Rates			
	DDR4-2133(CL15)	DDR4-2400(CL17)	DDR4-2666(CL19)	DDR4-3200(CL22)
DDR4-2400	V	V		
DDR4-2666	V	V	V	
DDR4-3200	V	V	V	V

- Single or Dual rank
- $V_{DD} = V_{DDQ} = 1.2V \pm 0.06V$
- Fly-by topology
- Terminated control, command, and address bus
- Halogen-free
- Data bus inversion (DBI) for data bus
- Integrated serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Anti-Sulfur Resistant (Optional)

2. Specification

1.1 Physical Dimension

2.1.1 Dimension

Table 1: Physical Dimension

Parameter	Dimension
Length	69.60 ± 0.1mm
Width	30.0 ± 0.1mm
Thickness (connector)	1.2mm ± 0.1mm

2.1.2 Weight

- 9.5g ± 10%

1.2 Performance

- DDR4-2400
- DDR4-2666
- DDR4-3200

1.3 Environmental Conditions

Table 2: Environmental Conditions

Feature	Operating	Storage
Temperature (Normal Grade)	-20°C ~ 95°C	-55°C ~ 110°C
Temperature (Wide Grade)	-40°C ~ 105°C	-55°C ~ 110°C
Humidity	10% ~ 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

1.4 Compliance Specifications

- RoHS

3. Functional Description

3.1 Pin Assignment

Table 3: Pin Assignment

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	VSS	68	VSS	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	VSS	135	VDD	201	VSS	4	DQ4	70	DQ24	136	VDD	202	VSS
5	VSS	71	DQ25	137	CK0_t	203	DQ46	6	VSS	72	VSS	138	CK1_t/NF	204	DQ47
7	DQ1	73	VSS	139	CK0_c	205	VSS	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	VSS
9	VSS	75	DM3_n/ DBI3_n	141	VDD	207	DQ42	10	VSS	76	DQS3_t	142	VDD	208	DQ43
11	DQS0_c	77	VSS	143	PARITY	209	VSS	12	DM0_n/ DBI0_n	78	VSS	144	A0	210	VSS
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	VSS	80	DQ31	146	A10/AP	212	DQ53
15	VSS	81	VSS	147	VDD	213	VSS	16	DQ6	82	VSS	148	VDD	214	VSS
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	VSS	84	DQ27	150	BA0	216	DQ48
19	VSS	85	VSS	151	WE_n/ A14	217	VSS	20	DQ2	86	VSS	152	RAS_n/ A16	218	VSS
21	DQ3	87	CB5/NC	153	VDD	219	DQS6_c	22	VSS	88	CB4/NC	154	VDD	220	DM6_n/ DBI6_n
23	VSS	89	VSS	155	ODT0	221	DQS6_t	24	DQ12	90	VSS	156	CAS_n/ A15	222	VSS
25	DQ13	91	CB1/NC	157	CS1_n/ NC	223	VSS	26	VSS	92	CB0/NC	158	A13	224	DQ54
27	VSS	93	VSS	159	VDD	225	DQ55	28	DQ8	94	VSS	160	VDD	226	VSS
29	DQ9	95	DQS8_c	161	ODT1/ NC	227	VSS	30	VSS	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	VSS	97	DQS8_t	163	VDD	229	DQ51	32	DQS1_c	98	VSS	164	VREFCA	230	VSS
33	DM1_n/ DBI_n	99	VSS	165	C1, CS3_n, NC	231	VSS	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	VSS	101	CB2/NC	167	VSS	233	DQ61	36	VSS	102	VSS	168	VSS	234	VSS
37	DQ15	103	VSS	169	DQ37	235	VSS	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	VSS	105	CB3/NC	171	VSS	237	DQ56	40	VSS	106	VSS	172	VSS	238	VSS
41	DQ10	107	VSS	173	DQ33	239	VSS	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	VSS	109	CKE0	175	VSS	241	DM7_n/ DBI7_n	44	VSS	110	CKE1/ NC	176	VSS	242	DQS7_t
45	DQ21	111	VDD	177	DQS4_c	243	VSS	46	DQ20	112	VDD	178	DM4_n/ DBI4_n	244	VSS
47	VSS	113	BG1	179	DQS4_t	245	DQ62	48	VSS	114	ACT_n	180	VSS	246	DQ63
49	DQ17	115	BG0	181	VSS	247	VSS	50	DQ16	116	ALERT_n	182	DQ39	248	VSS
51	VSS	117	VDD	183	DQ38	249	DQ58	52	VSS	118	VDD	184	VSS	250	DQ59
53	DQS2_c	119	A12	185	VSS	251	VSS	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	VSS
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	VSS	122	A7	188	VSS	254	SDA
57	VSS	123	VDD	189	VSS	255	VDDSPD	58	DQ22	124	VDD	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	VPP	60	VSS	126	A5	192	VSS	258	VTT
61	VSS	127	A6	193	VSS	259	VPP	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	VDD	195	DQ40	–	–	64	VSS	130	VDD	196	VSS	–	–
65	VSS	131	A3	197	VSS	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

3.2 Pin Description

Table 4: Pin Description

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM. A0–A14 (512Mx8).
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst- chopped.) See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs.)
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, RTT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable RTT.

Symbol	Type	I/O Level	Description
DM0_A_n-DM3_A_, DM0_B_n-DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. .
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin mVst be bounded to VDDQ on board.
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n mVst be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input/ Output	1.0V	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1V max	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
RFV			Reserved for Future use. No on DIMM electrical connection is present.

Symbol	Type	Description
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/ A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.

Symbol	Type	Description
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal VREF level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a singleended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to VDD on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/ TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet. (TDQS_t and TDQS_c are not valid for UDIMMs.)
VDD	Supply	**Module power supply:** 1.21V (TYP).
VPP	Supply	**DRAM activating power supply:** 2.5V –0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground.
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD.
RFU	-	Reserved for future use.
NC	-	**No connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.

3.3 Absolute Maximum DC Ratings

Table 5: Absolute Maximum DC Ratings

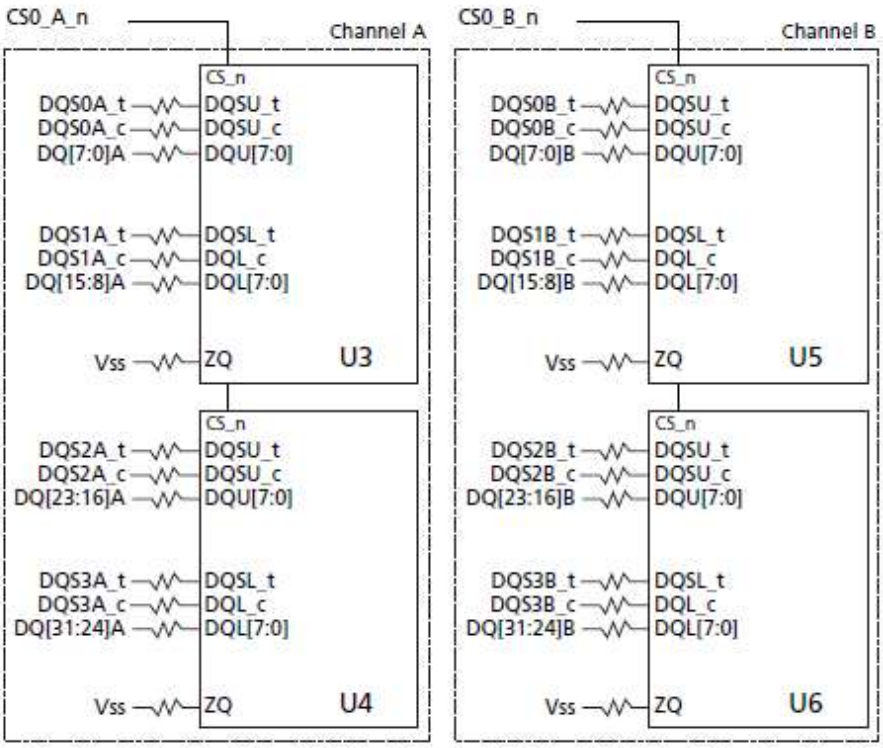
Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pins relative to VSS	-0.3 V ~ 1.5 V	V	1
VDDQ	Voltage on VDDQ pins relative to VSS	-0.3 V ~ 1.5 V	V	1
VPP	Voltage on VPP pin relative to VSS	-0.3 V ~ 3.0 V	V	2
VIN, VOUT	Voltage on any pin relative to VSS	-0.3 V ~ 1.5 V	V	

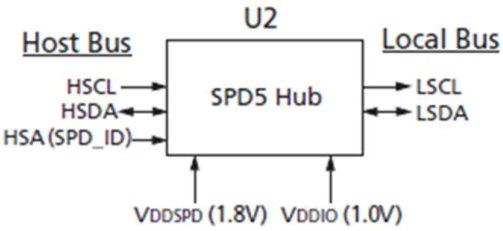
Notes:

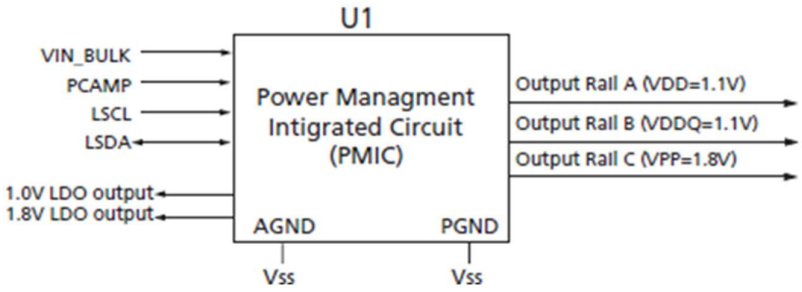
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV.

4. Block Diagram & Simplified Mechanical Drawing

4.1 Block Diagram (x16 1 Rank without ECC)





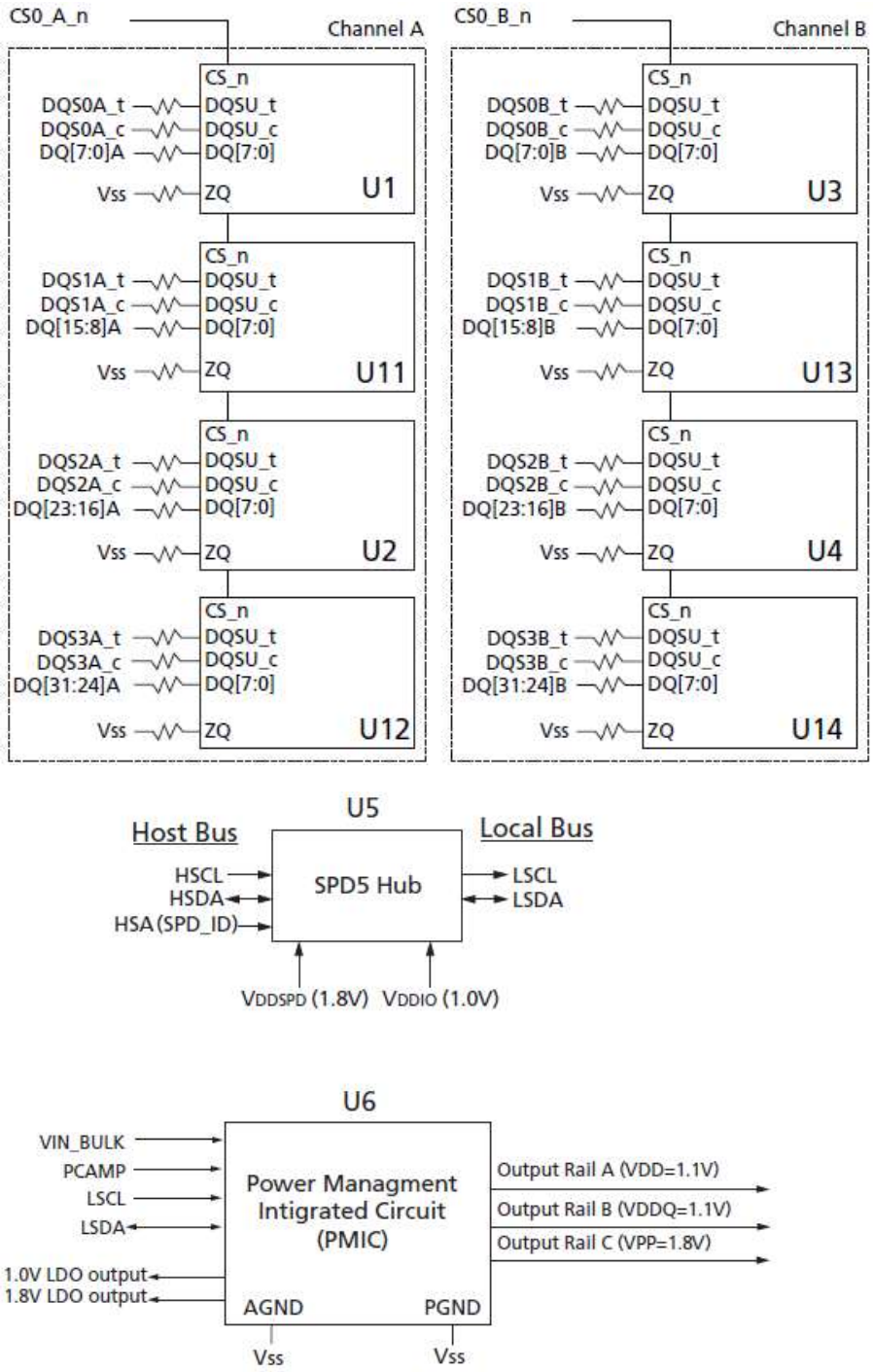


Notes:

1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2.Functional block diagram is for reference only.

4.2 Block Diagram (x8 1 Rank without ECC)

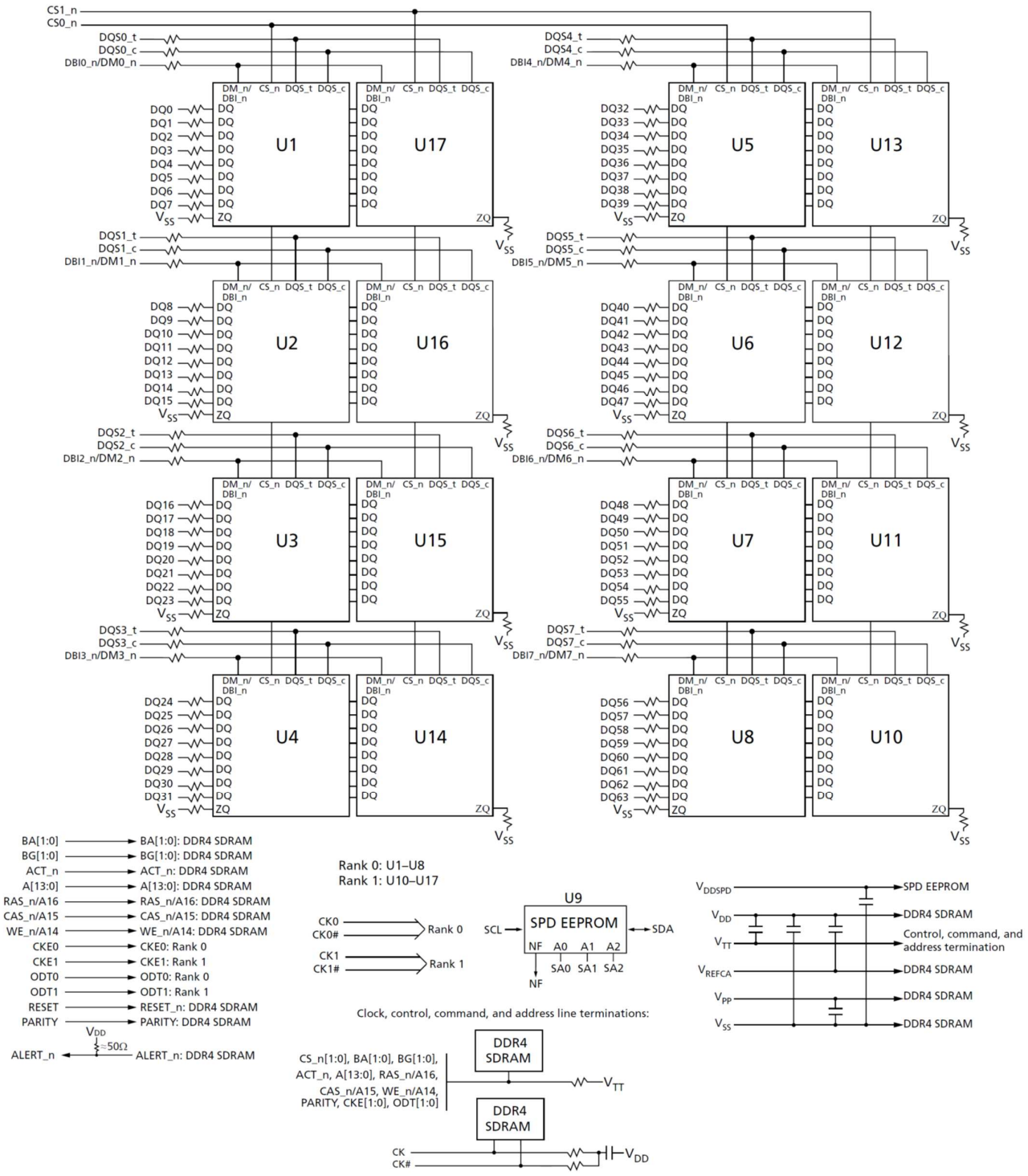


Notes:

1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

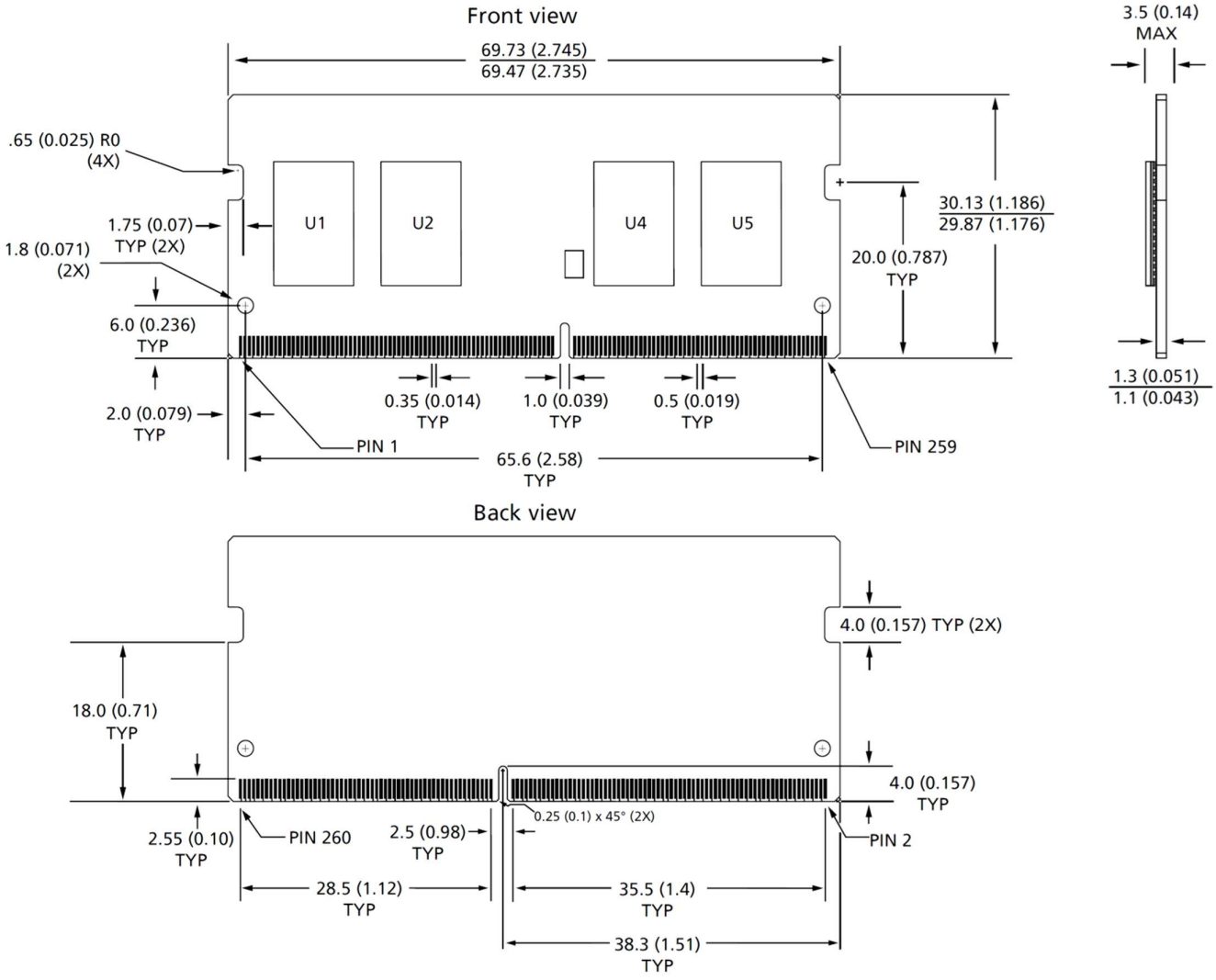
4.3 Block Diagram (x8 2 Ranks without ECC)



Notes:

1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

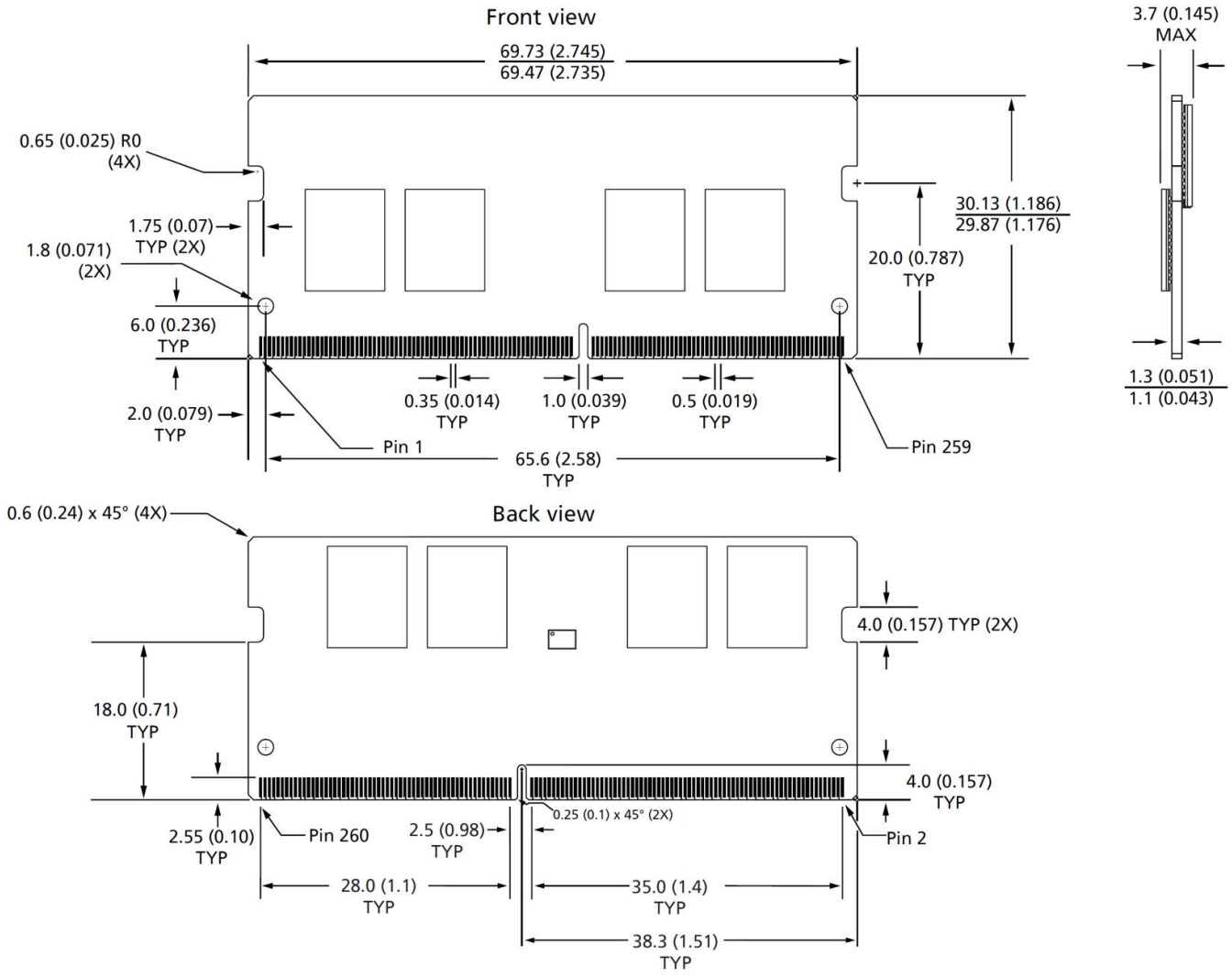
4.4 Simplified Mechanical Drawing (64bits SODIMM x16 1 Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

4.5 Simplified Mechanical Drawing (64bits SODIMM x8 1 Rank)

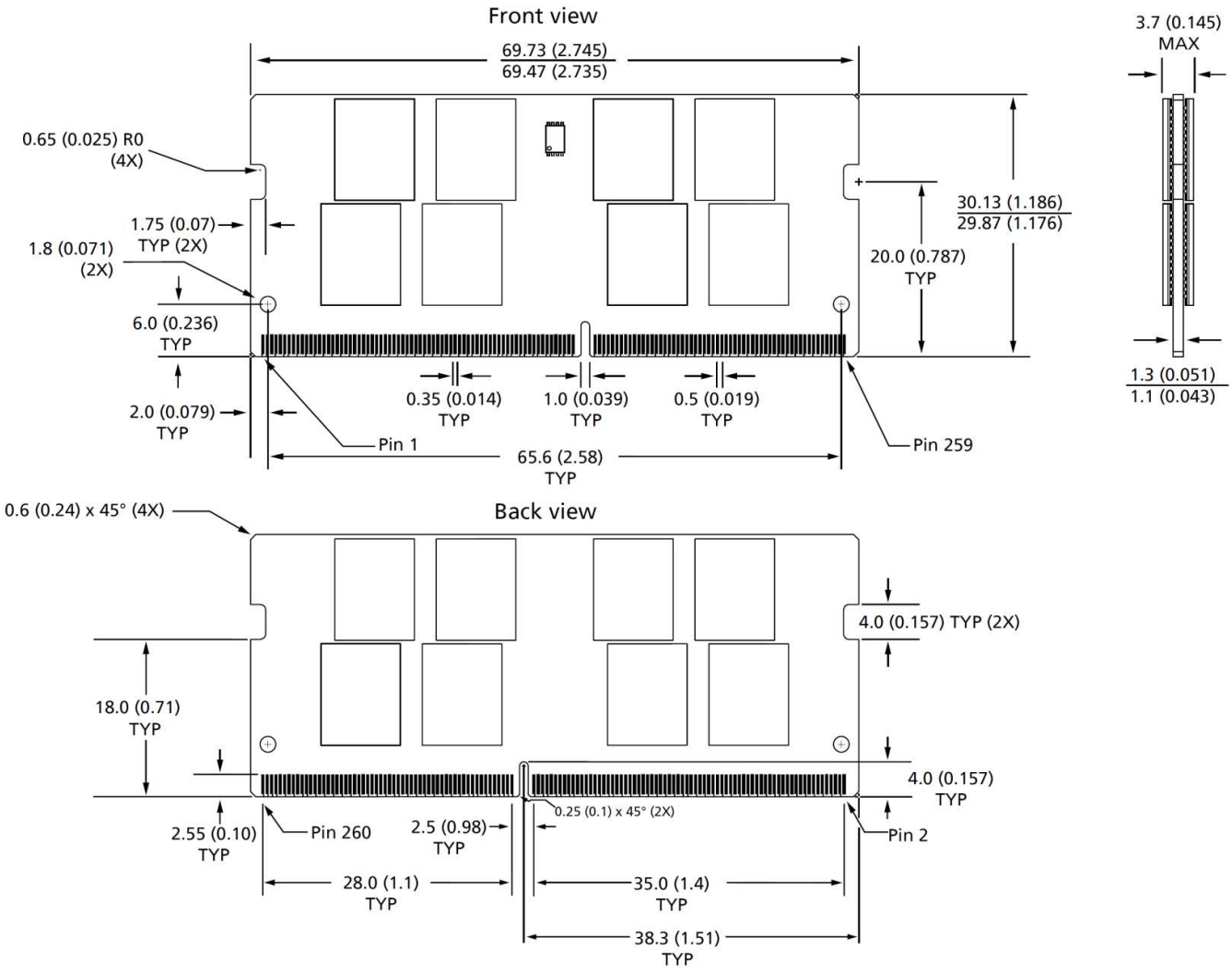


Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

4.6 Simplified Mechanical Drawing (64bits SODIMM x8 2 Ranks)



Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

5. Ordering Information

5.1 Part Number Definition

Table 6: Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	3	2	G	I	S	F	U	3	2	0	F	H	0

Code 1-2: Brand	SP: Silicon Power
Code 3-6: Capacity	002G: 2GB; 004G: 4GB; 008G: 8GB; 016G: 16GB; 032G: 32GB
Code 7: Product	I: Industrial Product Line
Code 8-9: Type & Form Factor	S: SODIMM; F: DDR4
Code 10: Operation Temperature	U: Normal Temperature -20°C ~ 95°C V: Wide Temperature: -40°C ~ 105°C
Code 11-13: Model Series	240:2400; 266:2666; 320: 3200
Code 14: Chip Specification	W: 256Mx16 N: 512Mx8 C: 512Mx16 B: 1Gx8 F: 2Gx8
Code 15: Chip Brand	H: Hynix; N: Nanya; S: Samsung
Code 16: Reserved	0: Standard; S: Anti-Sulfur Resistant
Code 17-18 (Option)	For Customization

5.2 Ordering Information Table

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
Normal Temperature (-20°C ~ 95°C)					
2GB	SP002GISFU266WN0	2GB (256Mx64) 256Mx16 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP002GISFU320WN0	2GB (256Mx64) 256Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
4GB	SP004GISFU240NH0	4GB (512Mx64) 512Mx8 1Rank	19.2GB/s	DDR4-2400	17-17-17
	SP004GISFU266CH0	4GB (512Mx64) 512Mx16 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP004GISFU266NN0	4GB (512Mx64) 512Mx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP004GISFU266NH0	4GB (512Mx64) 512Mx8 1Rank	21.3GB/s	DDR4-2666	19-19-19

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
	SP004GISFU320CH0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFU320CN0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFU320CS0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFU320NN0	4GB (512Mx64) 512Mx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
8GB	SP008GISFU240BH0	8GB (1Gx64) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17
	SP008GISFU266BH0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP008GISFU266BN0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP008GISFU320BH0	8GB (1Gx64) 1Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP008GISFU320BN0	8GB (1Gx64) 1Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
16GB	SP016GISFU266BH0	16GB (2Gx64) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19
	SP016GISFU266FH0	16GB (2Gx64) 2Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP016GISFU320BH0	16GB (2Gx64) 1Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP016GISFU320BS0	16GB (2Gx64) 1Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP016GISFU320FH0	16GB (2Gx64) 2Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
32GB	SP032GISFU320FH0	32GB (4Gx64) 2Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP032GISFU320FS0	32GB (4Gx64) 2Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
Wide Temperature (-40°C ~ 105°C)					
4GB	SP004GISFV266CH0	4GB (512Mx64) 512Mx16 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP004GISFV266NH0	4GB (512Mx64) 512Mx8 1Rank	21.3GB/s	DDR4-2666	19-19-19

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
	SP004GISFV266NN0	4GB (512Mx64) 512Mx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP004GISFV320CH0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFV320CN0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFV320CS0	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFV320CSS	4GB (512Mx64) 512Mx16 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP004GISFV320NN0	4GB (512Mx64) 512Mx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
8GB	SP008GISFV266BH0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP008GISFV266BN0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19
	SP008GISFV320BH0	8GB (1Gx64) 1Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
	SP008GISFV320BN0	8GB (1Gx64) 1Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
16GB	SP016GISFV266BH0	16GB (2Gx64) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19
	SP016GISFV320BH0	16GB (2Gx64) 1Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP016GISFV320BS0	16GB (2Gx64) 1Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP016GISFV320FH0	16GB (2Gx64) 2Gx8 1Rank	25.6GB/s	DDR4-3200	22-22-22
32GB	SP032GISFV320FH0	32GB (4Gx64) 2Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22
	SP032GISFV320FS0	32GB (4Gx64) 2Gx8 2Ranks	25.6GB/s	DDR4-3200	22-22-22

6. Appendix

Table 7: Abbreviation

Item	Abbreviation	Description
1	MTBF	Mean Time Between Failures
2	ECC	Error Correction Code
3	TCG	Trusted Computing Group
4	AES	Advanced Encryption Standard
5	OP	Over Provisioning
6	PS	Power Shield
7	DC	Direct Current
8	DRAM	Dynamic Random Access Memory
9	WAF	Write Amplification Factor
10	WLE	Wear Leveling Efficiency
11	Ta	Ambient Temperature
12	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.