AT93C56B and AT93C66B

3-wire Serial EEPROM

2K (256 x 8 or 128 x 16) and 4K (512 x 8 or 256 x 16)

DATASHEET

Features

- Low-voltage operation
  - V_{CC} = 1.7V to 5.5V
- User-selectable internal organization
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- 3-wire serial interface
- Sequential Read operation
- 2MHz clock rate (5V)
- Self-timed write cycle (5ms max)
- High reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-pad XDFN, and 8-ball VFBGA packages

Description

The Atmel® AT93C56B/66B provides 2,048/4,096 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 128/256 words of 16 bits each (when the ORG pin is connected to V_{CC}) and 256/512 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C56B/66B is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-pad XDFN, and 8-ball VFBGA packages.

The AT93C56B/66B is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before Write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

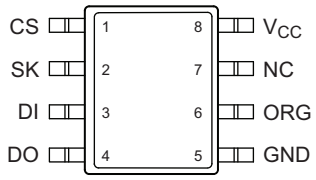
The AT93C56B/66B operates from 1.7V to 5.5V.

1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

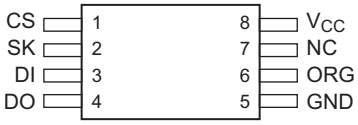
Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
NC	No Connect

8-lead SOIC



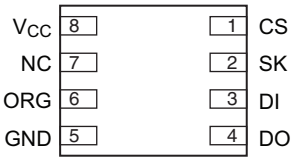
Top View

8-lead TSSOP



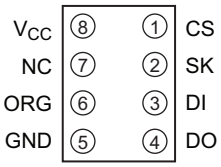
Top View

8-pad UDFN/XDFN



Bottom View

8-ball VFBGA



Bottom View

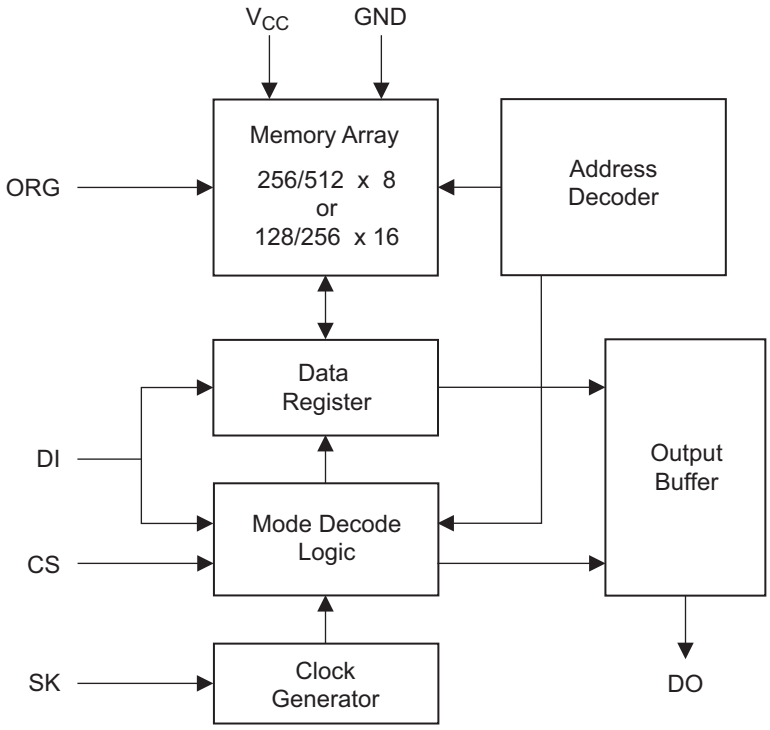
Note: Drawings are not to scale.

2. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram



Note: When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, and the application does not load the input beyond the capability of the internal 1MΩ pull-up resistor, then the x 16 organization is selected.

4. Memory Organization

4.1 Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized, and is not 100% tested.

4.2 DC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.7		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
V_{IL1}[1]	Input Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	V
V_{IH1}[1]	Input High Voltage	2.5V ≤ V_{CC} ≤ 5.5V		2.0		V_{CC} + 1	V
V_{IL2}[1]	Input Low Voltage	1.7V ≤ V_{CC} ≤ 2.5V		–0.6		V_{CC} x 0.3	V
V_{IH2}[1]	Input High Voltage	1.7V ≤ V_{CC} ≤ 2.5V		V_{CC} x 0.7		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA			0.4	V
V_{OH1}	Output High Voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OH} = –0.4mA	2.4			V
V_{OL2}	Output Low Voltage	1.7V ≤ V_{CC} ≤ 2.5V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High Voltage	1.7V ≤ V_{CC} ≤ 2.5V	I_{OH} = –100µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only, and are not tested.

4.3 AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, V_{CC} = as specified, CL = 1 TTL gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$		0	2	MHz
		$2.5V \le V_{CC} \le 5.5V$		0	1	MHz
		$1.7V \le V_{CC} \le 5.5V$		0	250	kHz
t_{SKH}	SK High Time	$2.5V \le V_{CC} \le 5.5V$		250		ns
		$1.7V \le V_{CC} \le 5.5V$		1000		ns
t_{SKL}	SK Low Time	$2.5V \le V_{CC} \le 5.5V$		250		ns
		$1.7V \le V_{CC} \le 5.5V$		1000		ns
t_{CS}	Minimum CS Low Time	$2.5V \le V_{CC} \le 5.5V$		250		ns
		$1.7V \le V_{CC} \le 5.5V$		1000		ns
t_{CSS}	CS Setup Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$	50		ns
			$1.7V \le V_{CC} \le 5.5V$	200		ns
t_{DIS}	DI Setup Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$	100		ns
			$1.7V \le V_{CC} \le 5.5V$	400		ns
t_{CSH}	CS Hold Time	Relative to SK		0		ns
t_{DIH}	DI Hold Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$	100		ns
			$1.7V \le V_{CC} \le 5.5V$	400		ns
t_{PD1}	Output Delay to 1	AC Test	$2.5V \le V_{CC} \le 5.5V$		250	ns
			$1.7V \le V_{CC} \le 5.5V$		1000	ns
t_{PD0}	Output Delay to 0	AC Test	$2.5V \le V_{CC} \le 5.5V$		250	ns
			$1.7V \le V_{CC} \le 5.5V$		1000	ns
t_{SV}	CS to Status Valid	AC Test	$2.5V \le V_{CC} \le 5.5V$		250	ns
			$1.7V \le V_{CC} \le 5.5V$		1000	ns
t_{DF}	CS to DO in High-impedance	AC Test	$2.5V \le V_{CC} \le 5.5V$		150	ns
		CS = V_{IL}	$1.7V \le V_{CC} \le 5.5V$		400	ns
t_{WP}	Write Cycle Time		$1.7V \le V_{CC} \le 5.5V$		5	ms
Endurance[1]	5.0V, 25°C			1,000,000		Write Cycles

Note: 1. This parameter is characterized, and is not 100% tested.

4.4 AT93C56B/66B Instruction Set

Instruction	SB	Opcode	Address		Data		Comments
			x 8[1]	x 16[1]	x 8	x 16	
READ	1	10	$A_8 – A_0$	$A_7 – A_0$			Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable must precede all programming modes.
ERASE	1	11	$A_8 – A_0$	$A_7 – A_0$			Erases memory location $A_N – A_0$.
WRITE	1	01	$A_8 – A_0$	$A_7 – A_0$	$D_7 – D_0$	$D_{15} – D_0$	Writes memory location $A_N – A_0$.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC3} (Section 4.2, “DC Characteristics” on page 4).
WRAL	1	00	01XXXXXXX	01XXXXXX	$D_7 – D_0$	$D_{15} – D_0$	Writes all memory locations. Valid only at V_{CC3} (Section 4.2) and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Note: 1. The Xs in the address field represent don’t care values, and must be clocked.

5. Functional Description

The AT93C56B/66B is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (Logic 1), followed by the appropriate opcode, and the desired memory address location.

Read: The Read instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output pin, DO. Output data changes are synchronized with the rising edges of the Serial Clock pin, SK. It should be noted that a dummy bit (Logic 0) precedes the 8-bit or 16-bit data output string. The AT93C56B/66B supports sequential Read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic 0) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

Erase/Write Enable (EWEN): To ensure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed, or V_{CC} power is removed from the part.

Erase: The Erase instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A Logic 1 at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

Write: The Write instruction contains the 8-bits or 16-bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at Serial Data Input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP}.

Erase All (ERAL): The Erase All (ERAL) instruction programs every bit in the Memory Array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. The ERAL instruction is valid only at V_{CC3} (Section 4.2, “DC Characteristics” on page 4).

Write All (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. The WRAL instruction is valid only at V_{CC3} (Section 4.2).

Erase/Write Disable (EWDS): To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing

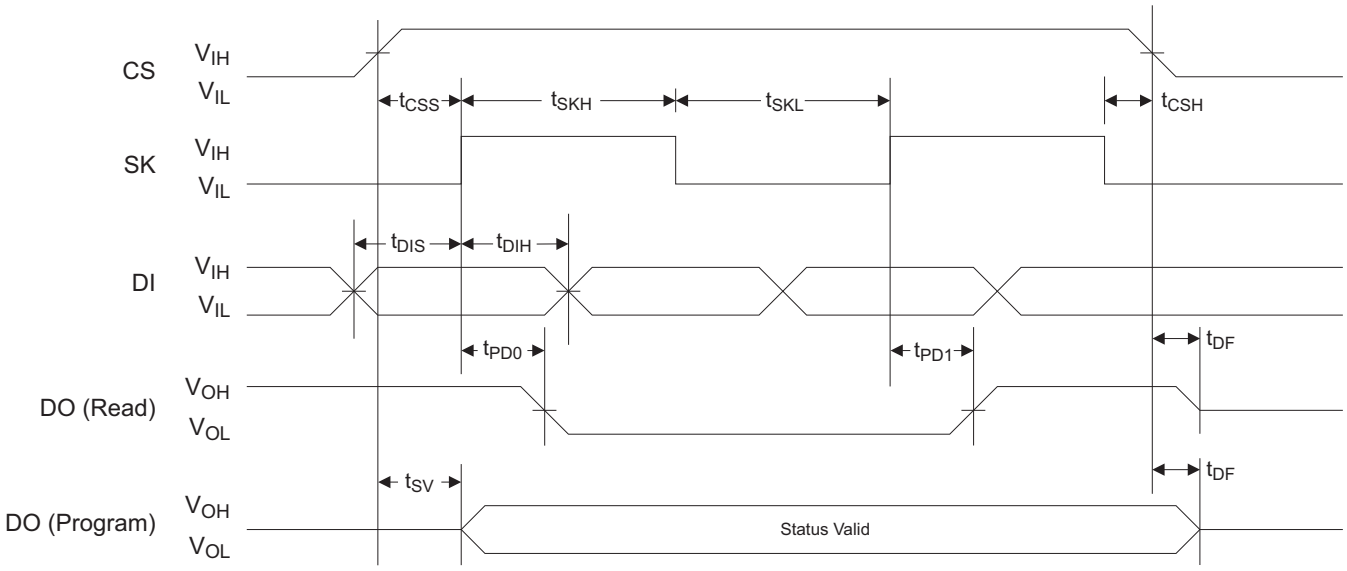


Table 6-1. Organization Key for Timing Diagrams

I/O	AT93C56B (2K)		AT93C66B (4K)	
	x 8	x 16	x 8	x 16
A_N	A_8[1]	A_7[2]	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}

Notes: 1. A_8 is a don't-care value, but the extra clock is required.
2. A_7 is a don't-care value, but the extra clock is required.

Figure 6-2. Read Timing

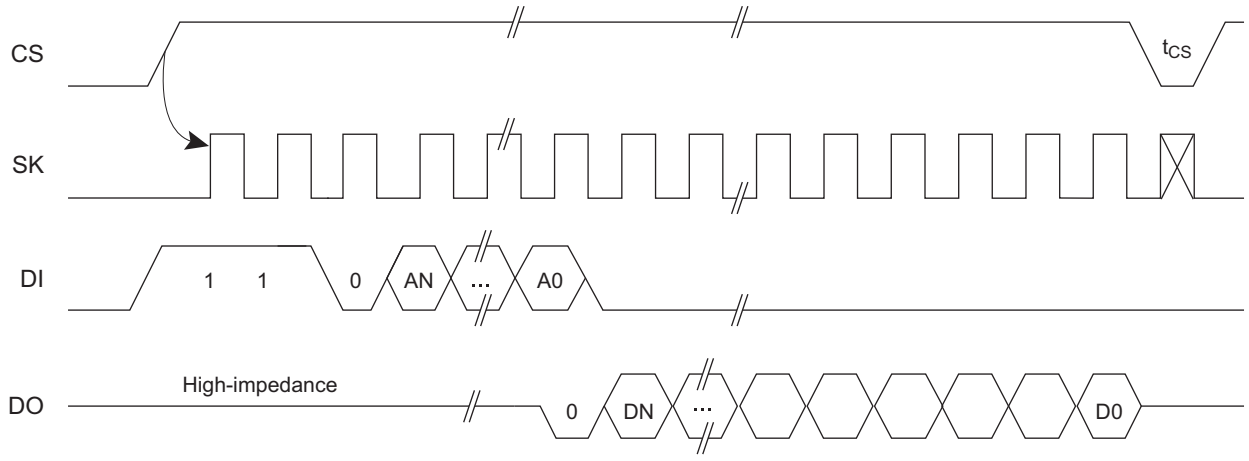


Figure 6-3. EWEN Timing

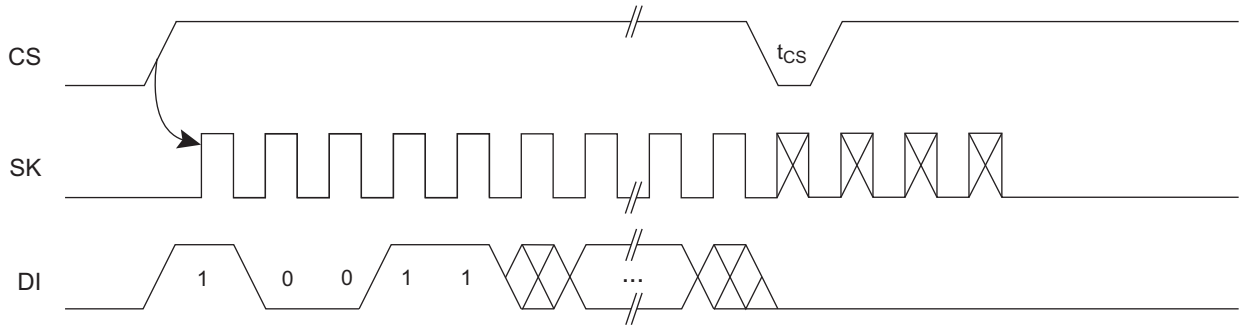


Figure 6-4. EWDS Timing

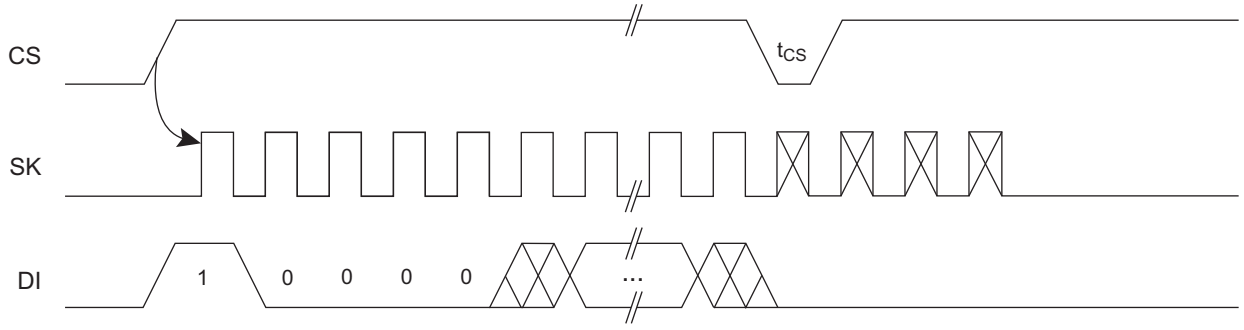


Figure 6-5. Write Timing

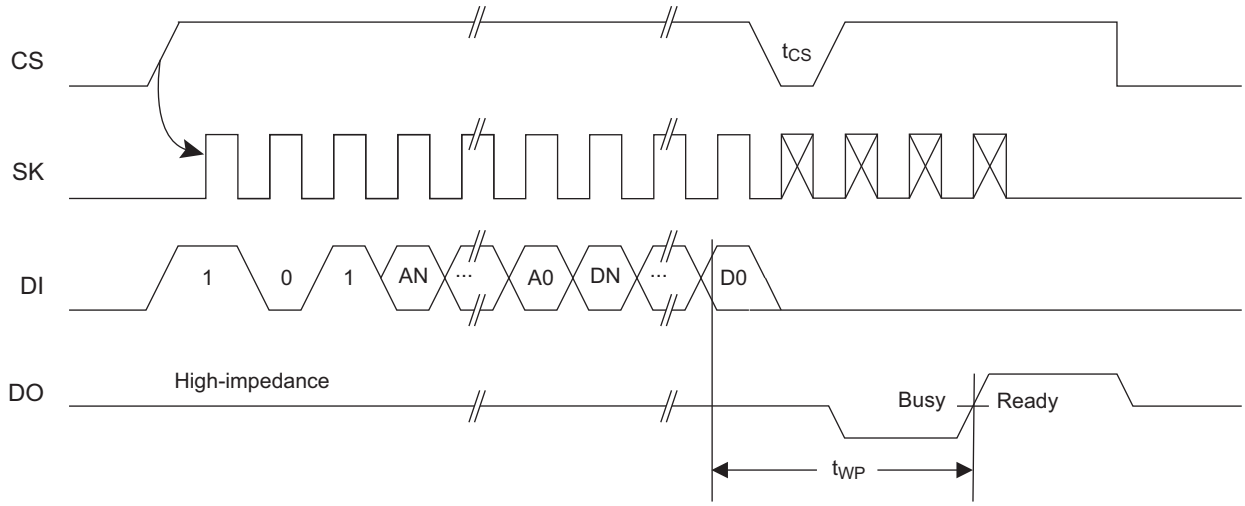
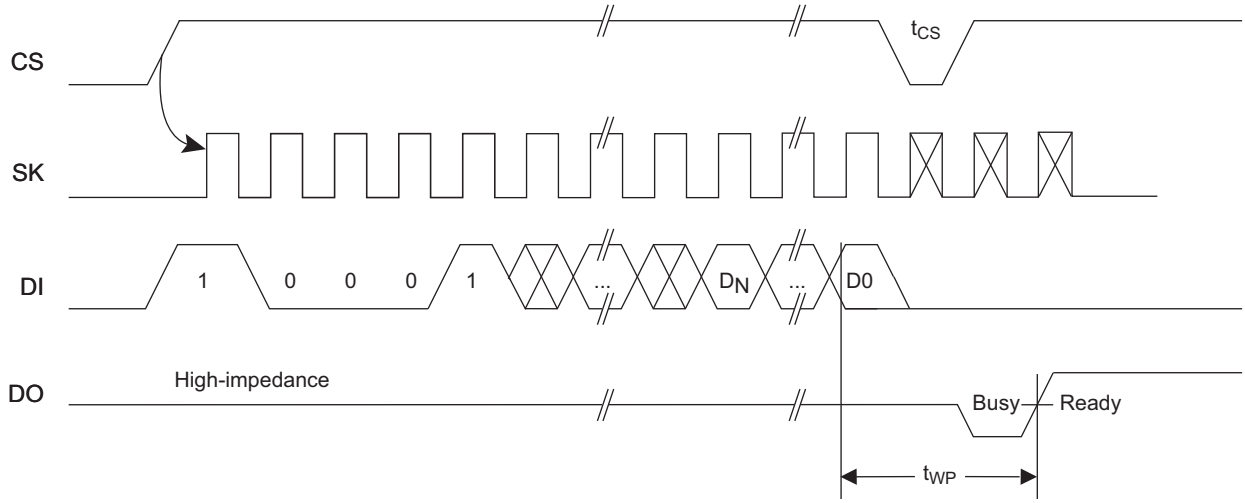


Figure 6-6. WRAL Timing[1]



Note: 1. Valid only at V_{CC3} (Section 4.2, “DC Characteristics” on page 4).

Figure 6-7. Erase Timing

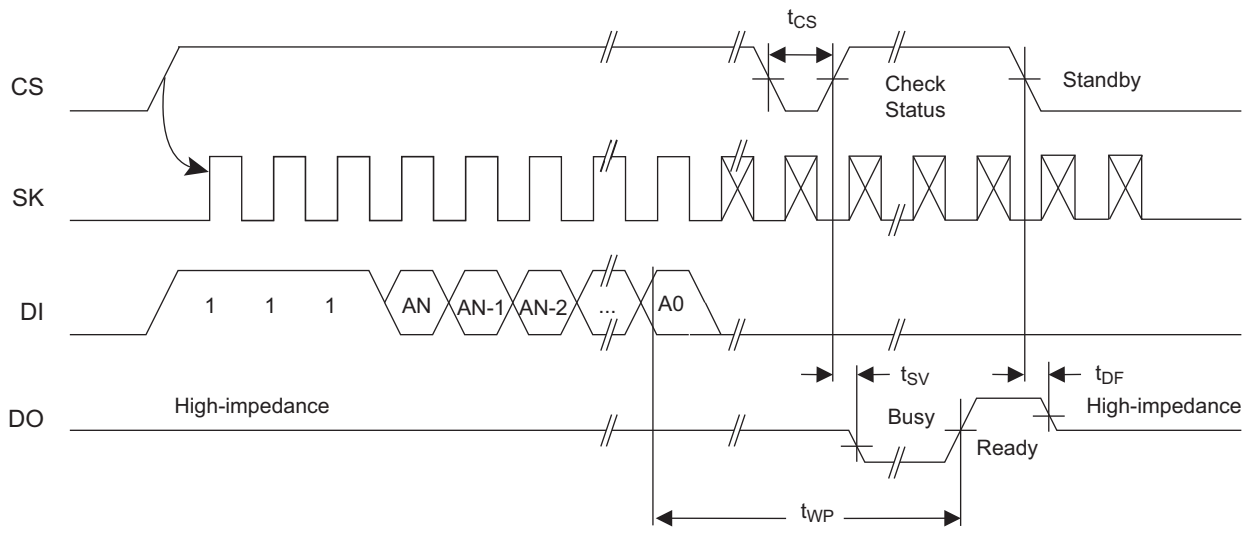
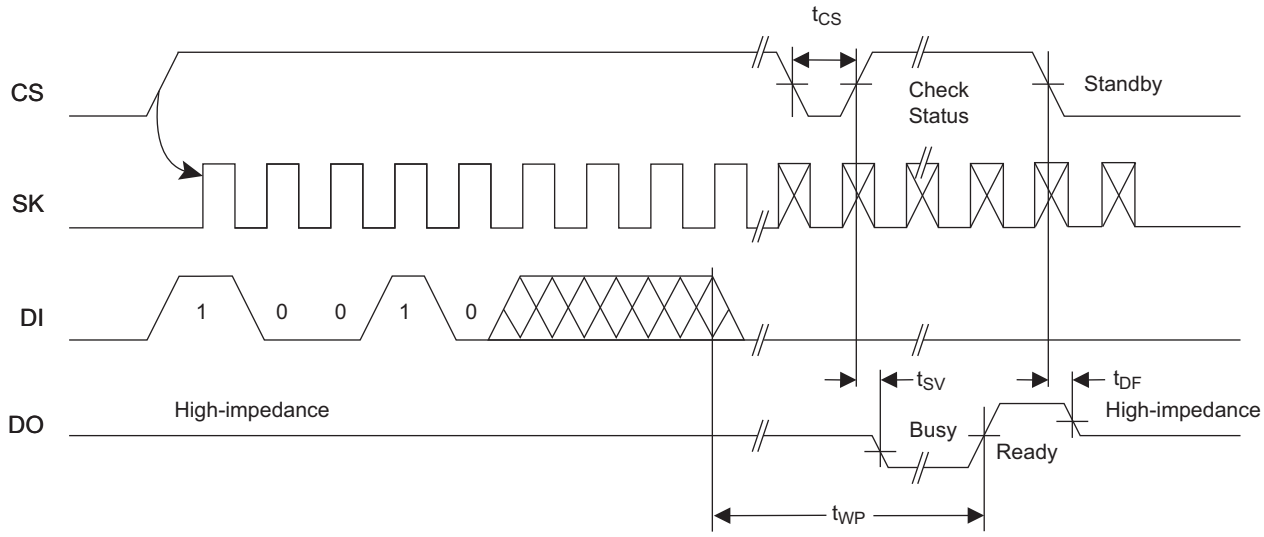
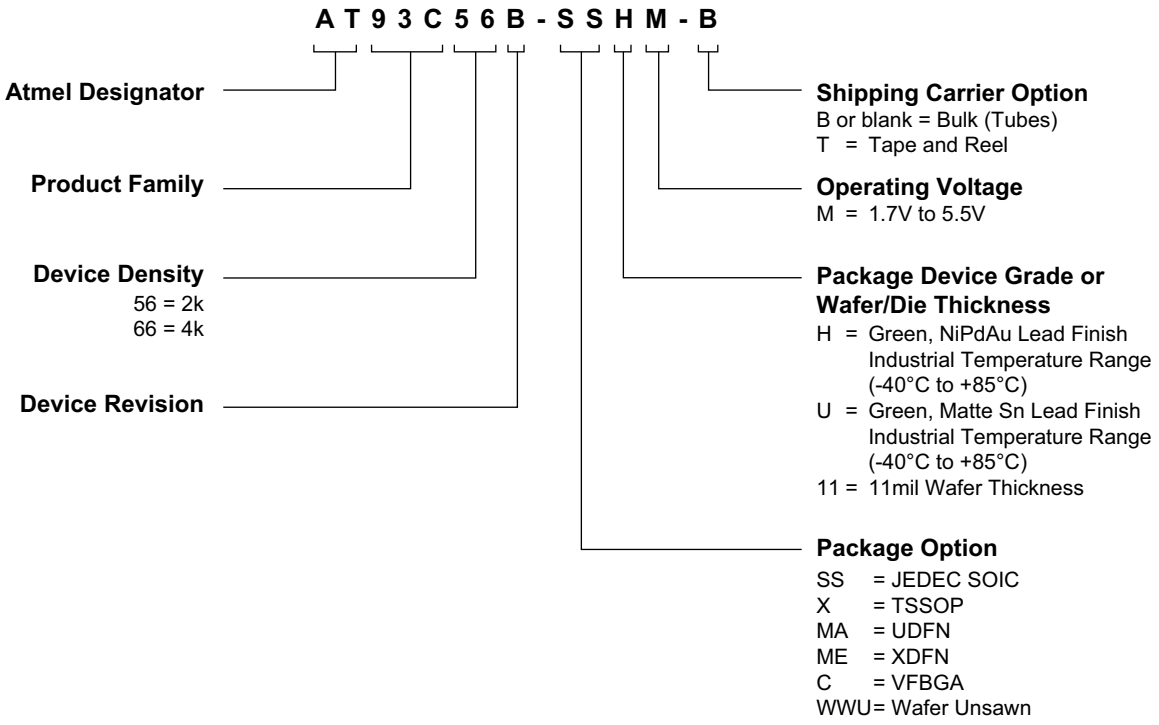


Figure 6-8. ERAL Timing[1]



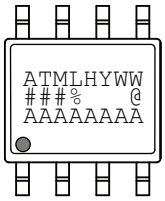
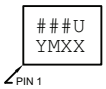
Note: 1. Valid only at V_{CC3} (Section 4.2, “DC Characteristics” on page 4).

7. Ordering Code Detail



8. Part Markings

AT93C56B and AT93C66B: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-pad UDFN
		2.0 x 3.0 mm Body
8-pad XDFN	**8-ball VFBGA**	
1.8 x 2.2 mm Body 	1.5 x 2.0 mm Body 	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT93C56B		Truncation Code ###: 56B	
AT93C66B		Truncation Code ###: 66B	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019 6: 2016 0: 2020	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		U: Industrial/Matte Tin/SnAgCu H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/22/13

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **93C56-66BSM**, AT93C56B and AT93C66B Package Marking Information	**DRAWING NO.** 93C56-66BSM	**REV.** B

9. Ordering Information

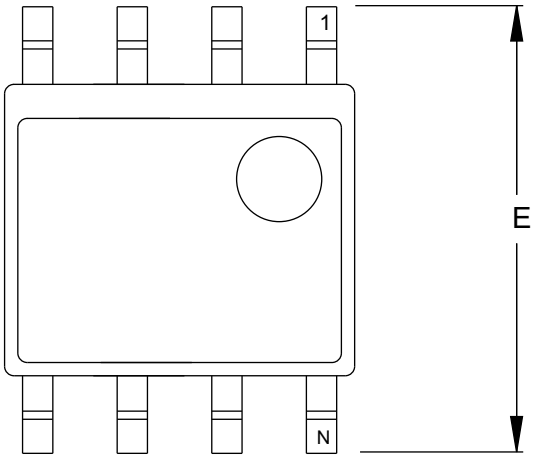
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT93C56B-SSHM-B[1]	NiPdAu (Lead-free/Halogen-free)	8S1	1.7V to 5.5V	Industrial Temperature (–40°C to 85°C)
AT93C56B-SSHM-T[2]				
AT93C56B-XHM-B[1]		8X		
AT93C56B-XHM-T[2]				
AT93C56B-MAHM-T[2]		8MA2		
AT93C56B-MEHM-T[2]		8ME1		
AT93C56B-CUM-T[2]	SnAgCu (Lead-free/Halogen-free)	8U3-1		
AT93C56B-WWU11M[3]	—	Wafer Sale		
AT93C66B-SSHM-B[1]	NiPdAu (Lead-free/Halogen-free)	8S1	1.7V to 5.5V	Industrial Temperature (–40°C to 85°C)
AT93C66B-SSHM-T[2]				
AT93C66B-XHM-B[1]		8X		
AT93C66B-XHM-T[2]				
AT93C66B-MAHM-T[2]		8MA2		
AT93C66B-MEHM-T[2]		8ME1		
AT93C66B-CUM-T[2]	SnAgCu (Lead-free/Halogen-free)	8U3-1		
AT93C66B-WWU11M[3]	—	Wafer Sale		

Notes:
1. B = Bulk
2. T = Tape and Reel
   - SOIC = 4k per reel
   - TSSOP, UDFN, XDFN, and VFBGA = 5k per reel
3. For wafer sales, please contact Atmel sales.

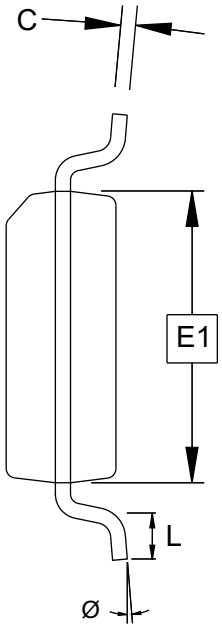
Package Type	
8S1	8-lead, 0.150” wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170” wide, Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin Dual No Lead (UDFN)
8ME1	8-pad, 1.80mm x 2.20mm body, Extra Thin Dual No Lead (XDFN)
8U3-1	8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Small Die Ball Grid Array (VFBGA)

10. Packaging Information

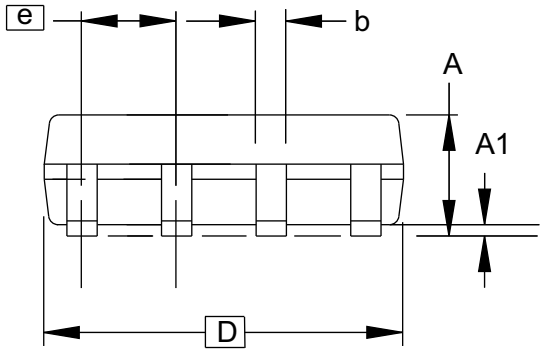
10.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

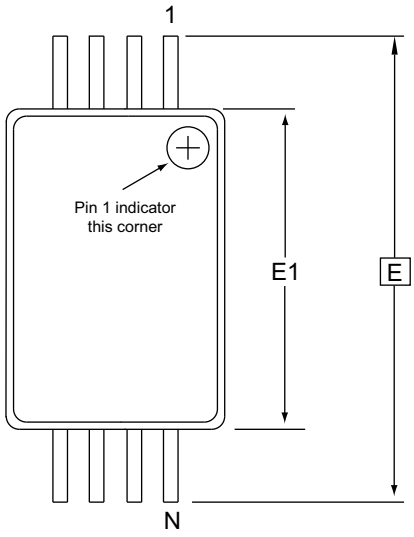
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

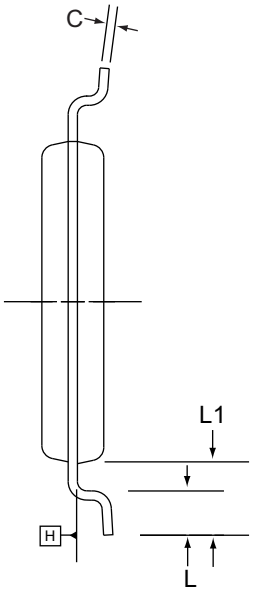
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

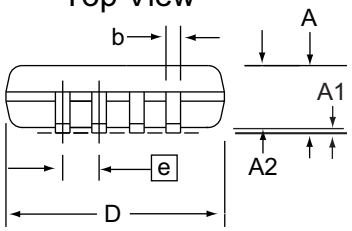
10.2 8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

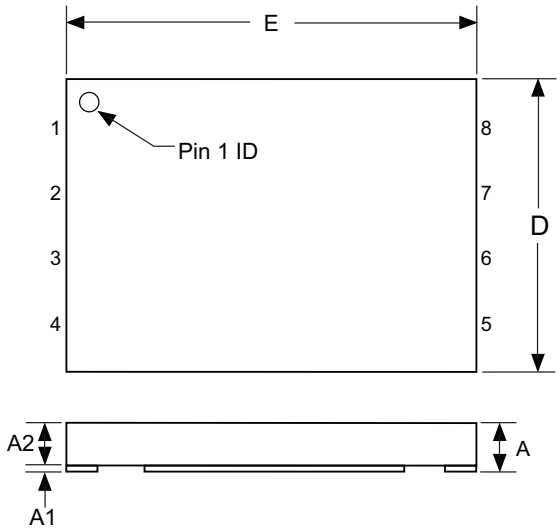
COMMON DIMENSIONS
(Unit of Measure = mm)

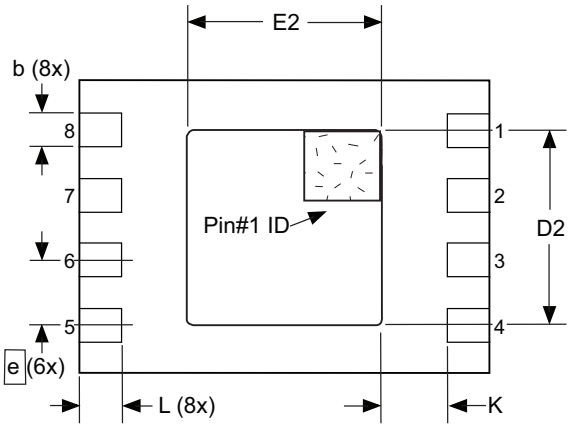
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

10.3 8MA2 — 8-pad UDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

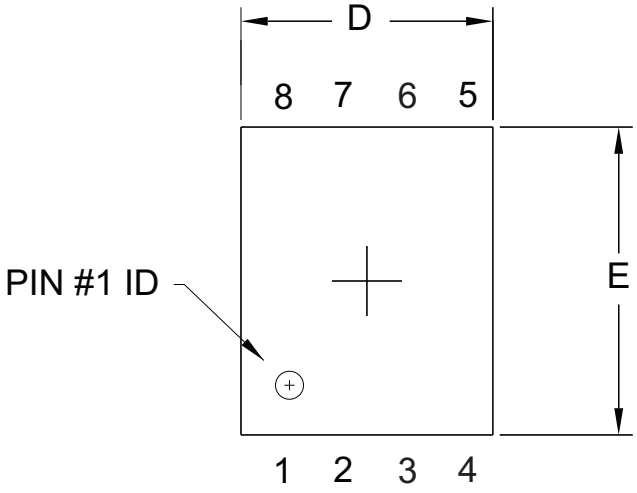
SYMBOL	MIN	NOM	MAX	NOTE
D	1.90	2.00	2.10	
E	2.90	3.00	3.10	
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	–	–	0.55	
C	0.152 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
b	0.18	0.25	0.30	3
K	0.20	–	–	

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

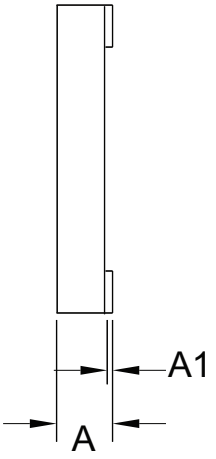
9/6/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** C

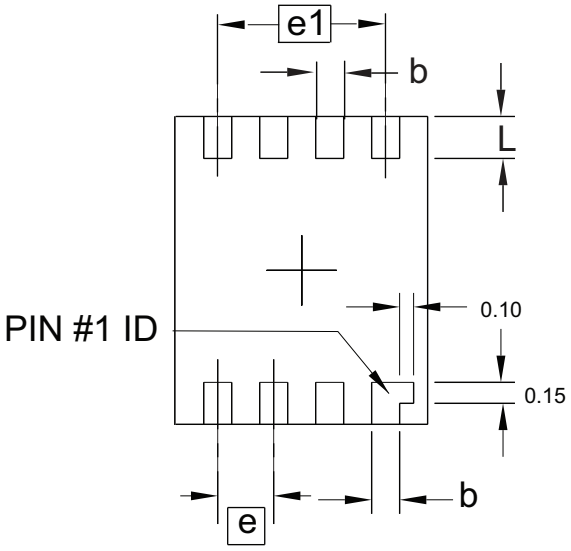
10.4 8ME1 — 8-pad XDFN



Top View



Side View



End View

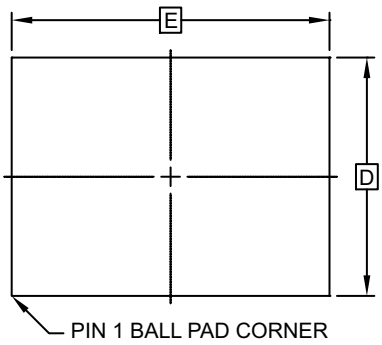
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

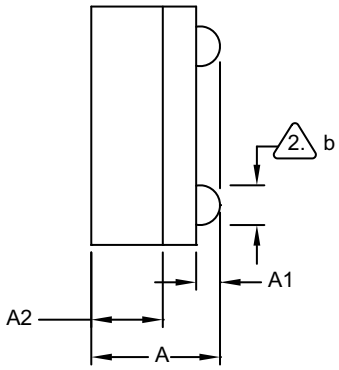
9/10/2012

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **8ME1**, 8-pad (1.80mm x 2.20mm body) Extra Thin DFN (XDFN)	**GPC** DTP	**DRAWING NO.** 8ME1	**REV.** B

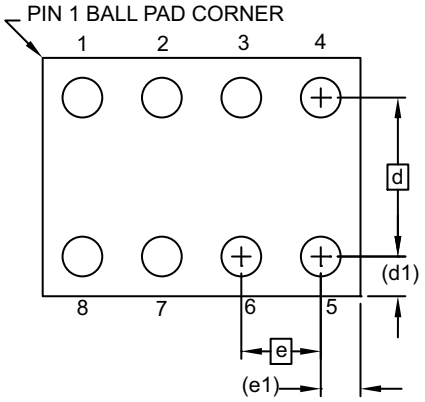
10.5 8U3-1 — 8-ball VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

3/27/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, VFBGA Package	GPC GXU	DRAWING NO. 8U3-1	REV. E

11. Revision History

Revision No.	Date	Comments
8735B	04/2013	Correct Synchronous Data Timing figure and remove note. Update TSSOP package option from 8A2 to 8X. Update UDFN package option from 8Y6 to 8MA2. Update template and Atmel logos.
8735A	01/2011	Initial document release.

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