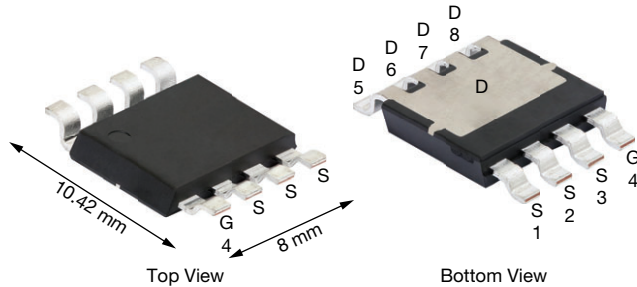


Automotive N-Channel 80 V (D-S) 175 °C MOSFET

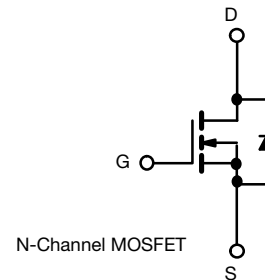
PowerPAK® 8 x 8LR


FEATURES

- TrenchFET® Gen V power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.9 mm height
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY

V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.00144
I_D (A) ^e	352
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ580ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ^e	I_D	352	A
$T_C = 25$ °C		203	
Continuous source current (diode conduction) ^e	I_S	340	
Pulsed drain current ^{a, e}	I_{DM}	700	
Single pulse avalanche current	I_{AS}	75	mJ
Single pulse avalanche energy	E_{AS}	285	
Maximum power dissipation ^{c, e}	P_D	375	W
		125	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	40	°C/W
Junction-to-case (drain lead) ^d	R_{thJL}	0.7	
Junction-to-case (pad) as measured at drain pad	R_{thJC}	0.4	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

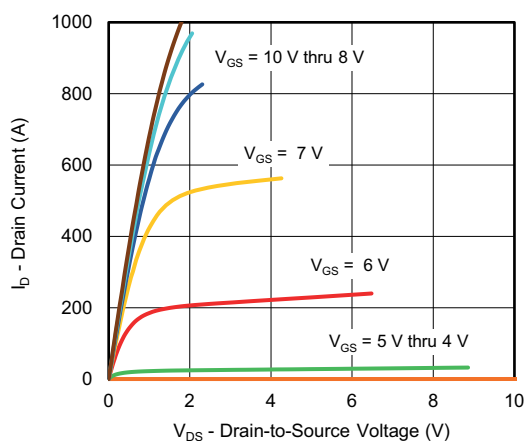
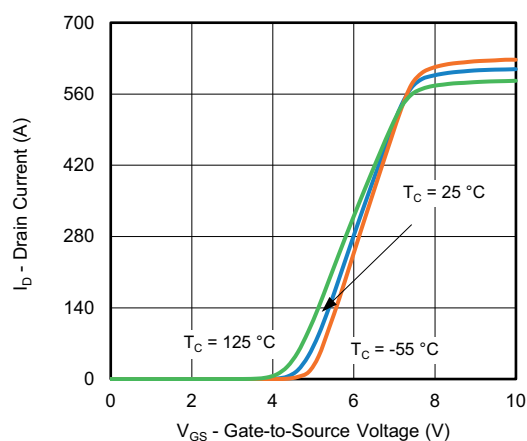
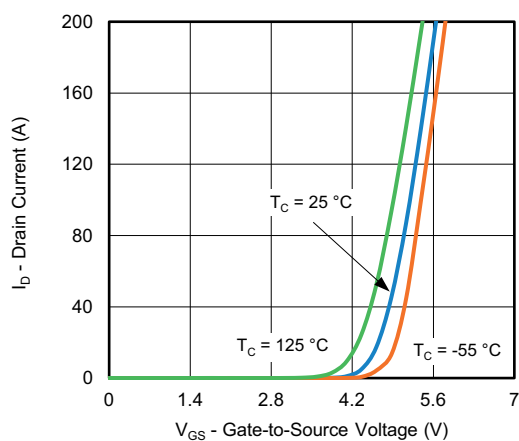
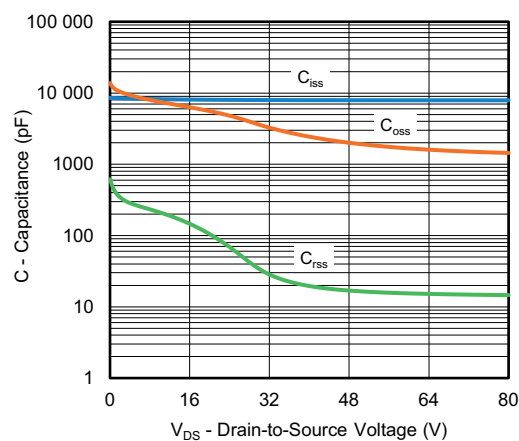
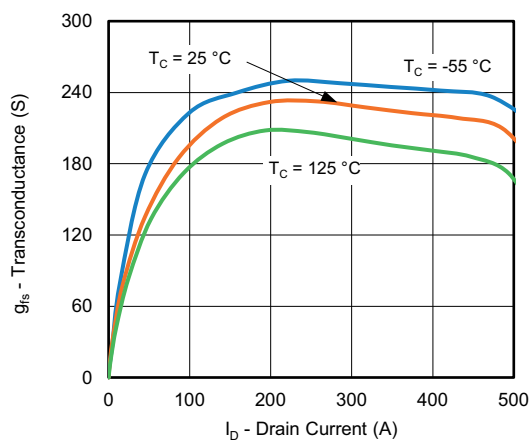
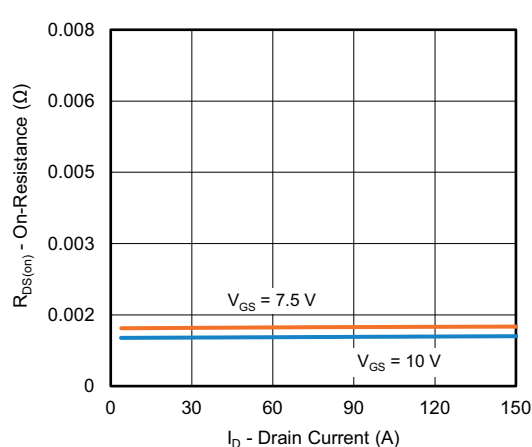


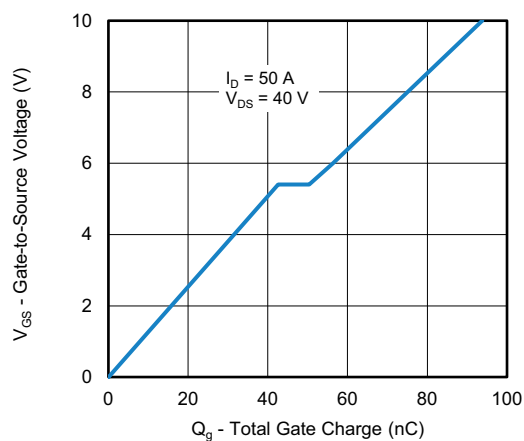
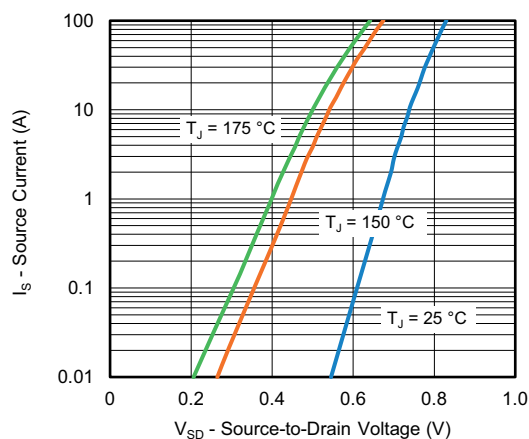
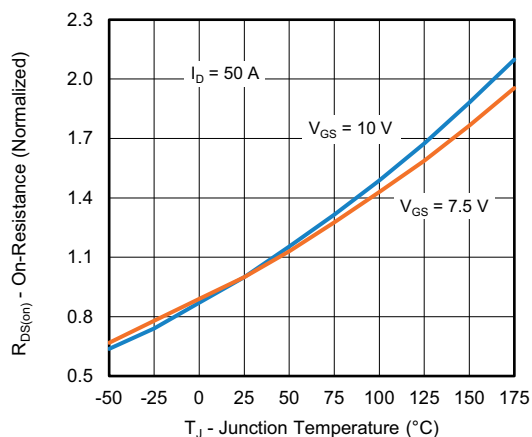
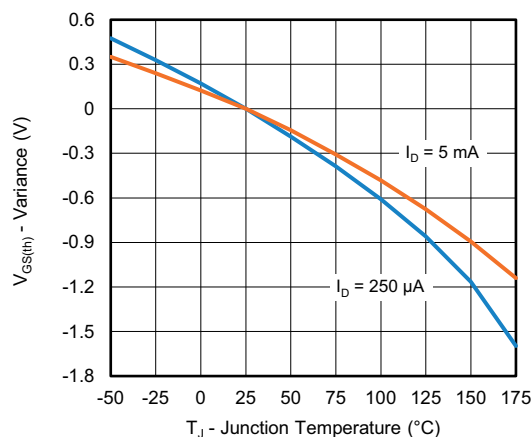
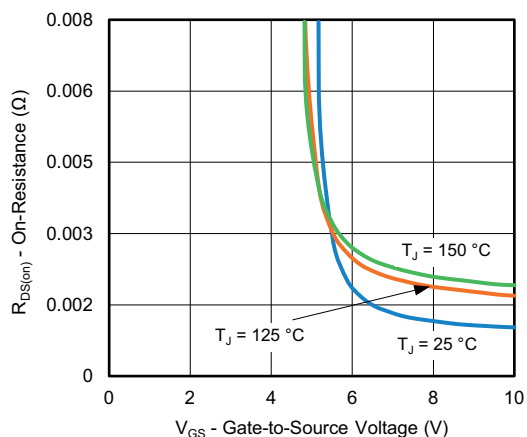
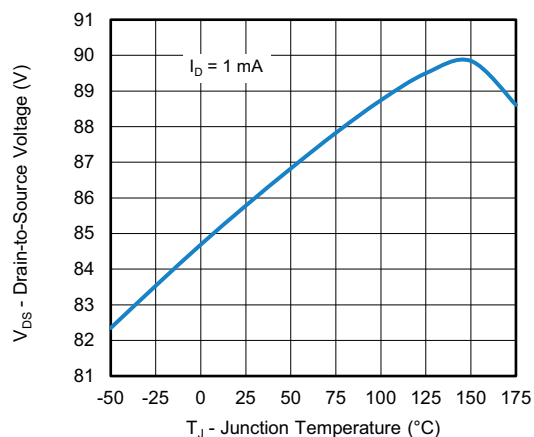
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.2	2.8	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	500	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	50	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.00120	0.00144	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0025	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0031	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 25 A		-	100	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	8037	11 252	pF
Output capacitance	C _{oss}			-	4450	6250	
Reverse transfer capacitance	C _{rss}			-	52	73	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 40 V, I _D = 50 A	-	93	140	nC
Gate-source charge ^c	Q _{gs}			-	46	-	
Gate-drain charge ^c	Q _{gd}			-	8	-	
Gate resistance	R _g	f = 1 MHz		0.9	1.8	2.7	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 40 V, R _L = 0.8 Ω, I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1 Ω		-	21	32	ns
Rise time ^c	t _r			-	16	24	
Turn-off delay time ^c	t _{d(off)}			-	37	56	
Fall time ^c	t _f			-	11	17	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	700	A
Forward voltage	V _{SD}	I _F = 40 A, V _{GS} = 0 V		-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 40 A, di/dt = 100 A/μs		-	97	194	ns
Body diode reverse recovery charge	Q _{rr}			-	254	508	nC
Reverse recovery fall time	t _a			-	60	-	ns
Reverse recovery rise time	t _b			-	37	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-4.6	-	A

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

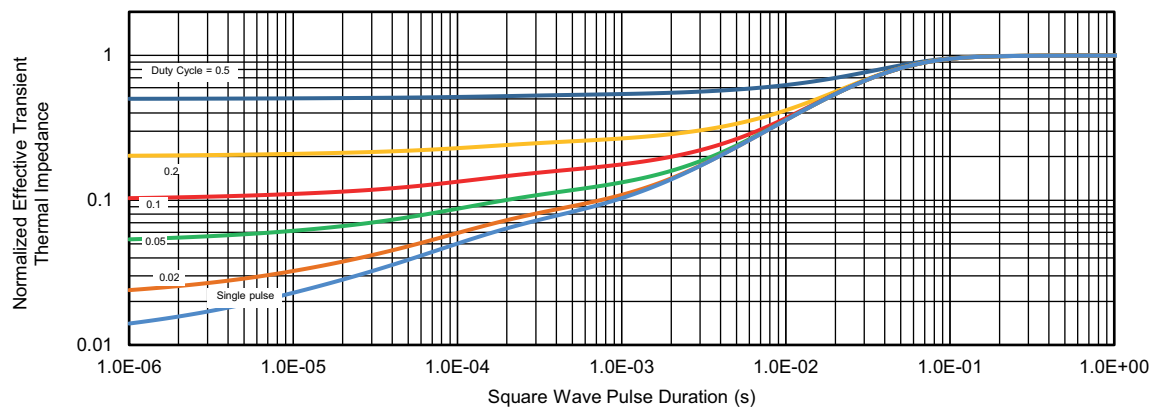
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Capacitance

Transconductance

On-Resistance vs. Drain Current

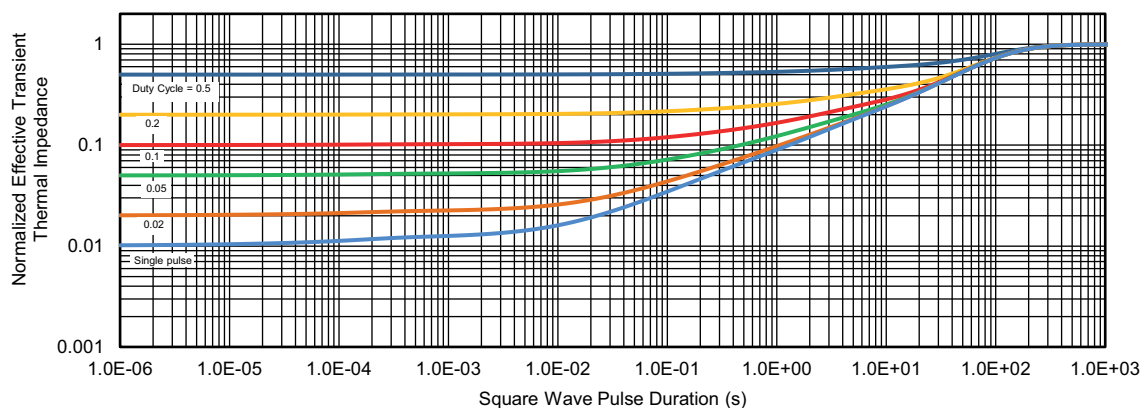
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate Charge

Source Drain Diode Forward Voltage

On-Resistance vs. Junction Temperature

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

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