48V Input, 1A Output, 2.2 MHz Switching Frequency, Integrated Switch Step-Down Regulator

MCP16364/5/6

Description

The MCP16364/5/6 family of devices are highly integrated, high-efficiency, fixed-frequency, step-down DC-DC converters in a compact 8-lead 3 mm x 3 mm VDFN package that operates from input voltage sources up to 48V. Integrated features include a high-side switch, fixed-frequency Peak Current Mode Control, Internal Compensation, Power Good, Peak Current Limit and Overtemperature Protection. The MCP16364/5/6 provides all the active functions for local DC-DC conversion, with fast transient response and accurate regulation.

High efficiency conversion is achieved by integrating the current-limited, high-speed N-Channel MOSFET and associated drive circuitry. High switching frequency minimizes the size of external filtering components resulting in a small size solution.

The MCP16364/5/6 can supply 1A of continuous current while regulating the output voltage from 2.0V to 24V. An integrated, high-performance peak current mode control architecture keeps the output voltage tightly regulated, even during input voltage steps and output current transient conditions that are common in power systems.

The MCP16364 is capable of running in PFM/PWM mode. It switches in PFM mode for light load conditions and for large step-down conversion ratios. This results in a higher efficiency over all load ranges.

By comparison, the MCP16365 runs in PWM-only mode and is recommended for applications where the low-frequency component associated with the PFM mode of operation is not desirable.

Besides the two aforementioned options, the MCP16366 is designed for EMI constrained applications where reduced peak emissions are required. This is achieved by sweeping the switching frequency over a 10% range above the 2.2 MHz nominal value.

Output voltage is set with an external resistor divider. The Power Good output pin will go from logic-low to logic-high (through an external pull-up resistor) when the output voltage is within 93% of the nominal set point. The EN input is used to turn the device on and off. While off, only a few micro-amps of current are consumed from the input.

The MCP16364/5/6 is offered in a space-saving 8-lead 3 mm x 3 mm VDFN wettable flanks surface mount package.

The MCP16364/5/6 also passes automotive AEC-Q100 reliability testing.

Features

- Input Voltage Range: 4.0V (After Start-up) to 48V
- Adjustable Output Voltage Range: 2.0V to 24V
- Integrated N-Channel Buck Switch: 500 mΩ
- 1A Output Current
- 2.2 MHz Fixed Switching Frequency
- Shutdown Current: 3 µA Typical
- Quiescent Current: 18 µA Typical (Not Switching)
- Device Selectable Switching Mode:
  - Automatic Pulse Frequency Modulation/Pulse Width Modulation (PFM/PWM) Operation - **MCP16364**

  - PWM only Mode of Operation - **MCP16365**
  - PWM only Mode of Operation with Switching Frequency Dithering for EMI constrained applications - **MCP16366**
- Power Good Output
- Undervoltage Lockout (UVLO)
- Peak Current Mode Control
- Internal Compensation
- Internal Soft-Start
- Internal Bootstrap Diode
- Cycle-by-Cycle Peak Current Limit
- Overtemperature Protection
- Available Package: 8-lead 3 mm x 3 mm Wettable Flanks VDFN, see Package
- AEC-Q100 Automotive Qualified, see Product Identification System

Applications

- Automotive DC/DC and 48V Systems
- Microcontroller Bias Supply
- 24V Industrial Input DC-DC Conversion
- Set-Top Boxes, DSL Cable Modems
- Wall Cube Regulation
- SLA Battery-Powered Devices
- AC-DC Digital Control Power Sources
- Power Meters
- Medical and Health Care
- Distributed Power Supplies

1. Typical Application

Figure 1-1. Typical Application Circuits

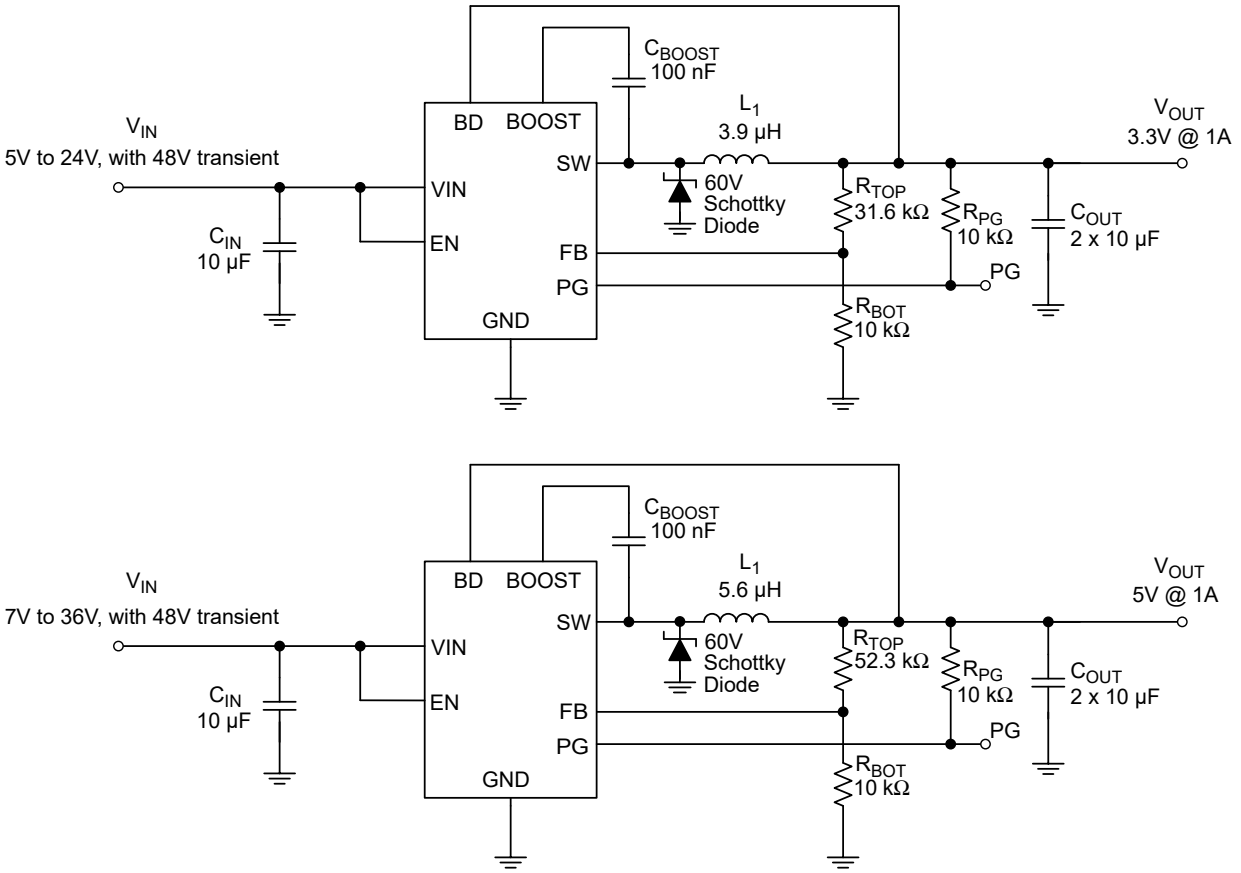
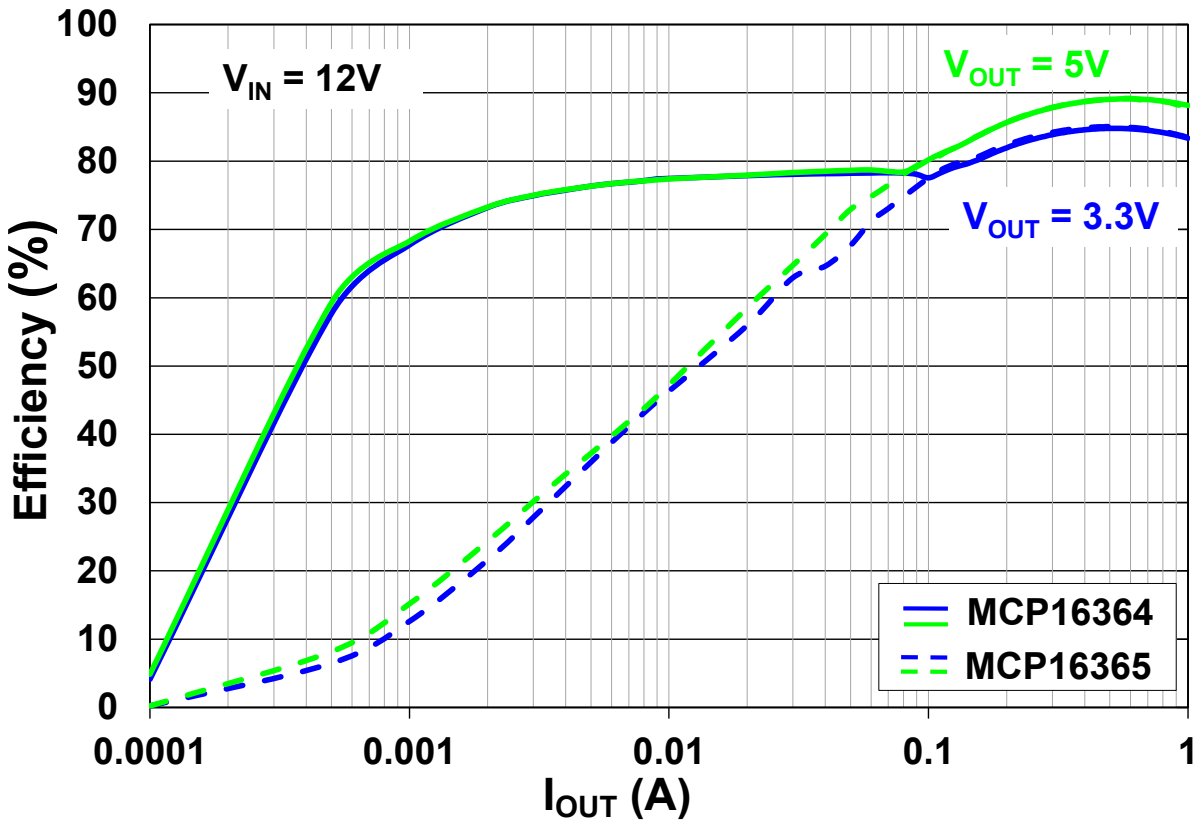


Figure 1-2. Efficiency vs. Output Current



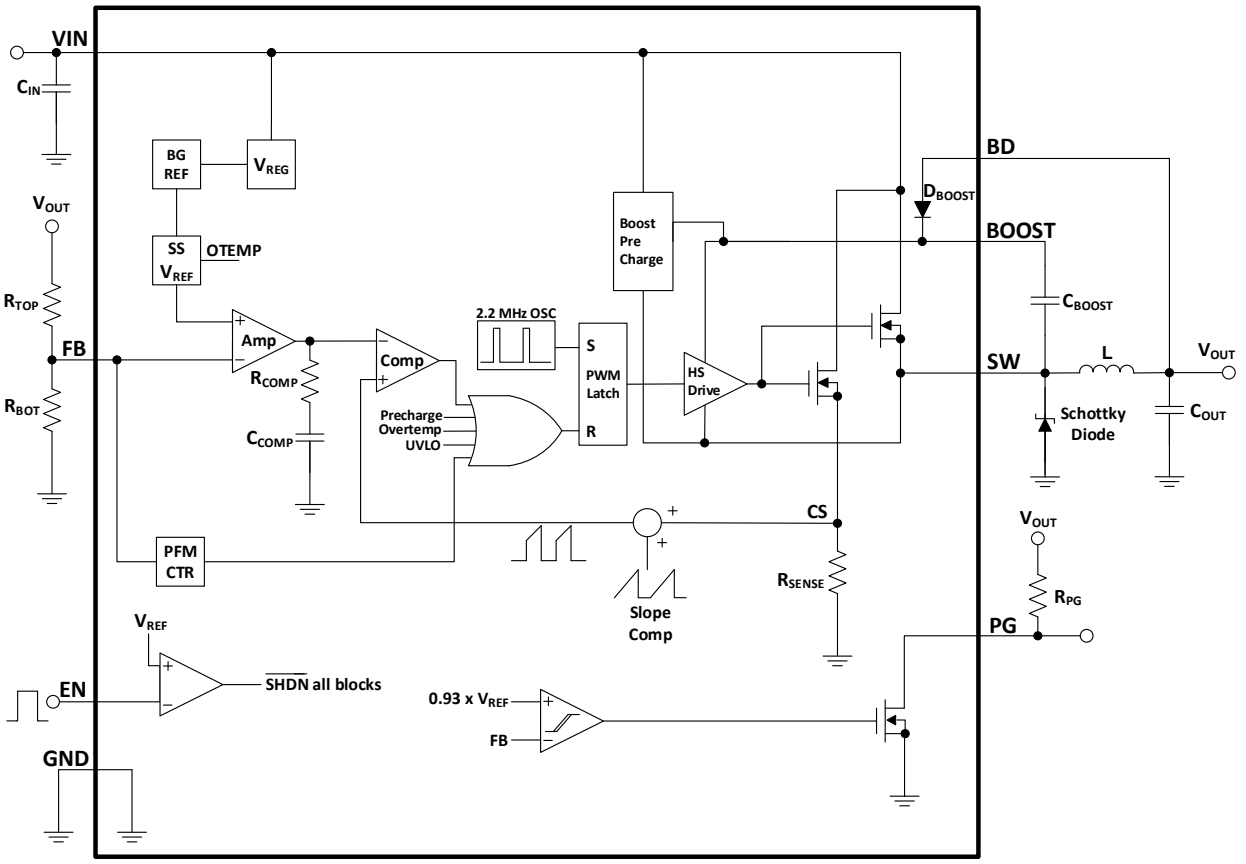
2. Product Family

Table 2-1. Device Options

Part Number	Switching Mode Option	Switching Frequency
MCP16364	PFM/PWM	Fixed 2.2 MHz
MCP16365	PWM Only	Fixed 2.2 MHz
MCP16366	PWM Only	2.2 MHz with +10% Frequency Dithering

3. Block Diagram

Figure 3-1. Simplified Block Diagram



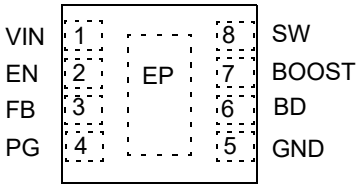
4. Pin Configuration

Table 4-1. Pin Function Table

Pin Number	Symbol	Description
1	VIN	Input supply voltage pin for power and internal biasing.
2	EN	Enable pin. Logic high enables the operation. Do not allow this pin to float.
3	FB	Output voltage feedback pin. Connect FB to an external resistor divider to set the output voltage.
4	PG	Open Drain Power Good Output.
5	GND	Signal and Power Ground Reference.
6	BD	The anode of the internal bootstrap diode. Connect it to V_{OUT} or to a power source < 5.5V.
7	BOOST	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
8	SW	Output switch node, connects to the inductor, freewheeling diode and the bootstrap capacitor.
9	EP	Exposed Pad. Must be connected to the GND plane to help dissipate power.

4.1 Package

Figure 4-1. Pin Configuration 8-Lead 3 mm x 3 mm VDFN (Top View)



4.2 Pin Description

Power Supply Input Voltage Pin (VIN)

The VIN pin is the input voltage for the buck converter power stage and internal circuitry. This pin is connected to the drain terminal of the internal high-side N-Channel MOSFET. A 10 µF minimum ceramic capacitor must be connected from the VIN to the GND pin, as close as possible to the device. A combination of multiple ceramic capacitors of different sizes is recommended.

Enable Pin (EN)

The EN pin is a logic-level input used to enable or disable the device switching and lower the quiescent current while disabled. To turn off the device, the EN pin must be pulled low. Do not leave this pin floating.

Feedback Voltage Pin (FB)

The FB pin is used to provide output voltage regulation by using a resistor divider. The V_{FB} voltage will be 0.800V typical with the output voltage in regulation.

Power Good Output Pin (PG)

The PG pin is the drain connection of an internal N-channel FET. When the output voltage is within 93% of the nominal set point, this pin will go from logic-low to logic-high (through an external pull-up resistor).

Ground Pin (GND)

The ground or return pin is used for circuit ground connection. The length of the trace from the input capacitor return, output capacitor return and GND pin must be made as short as possible to minimize the noise on the GND pin.

Boost Diode Pin (BD)

The BD pin is the anode of a diode, which is connected to the BOOST pin. The BD pin must be connected to a voltage output between 3V and 5.5V. If the output voltage of the converter is set between these values, connecting the BD pin to the output is recommended.

Boost Pin (BOOST)

The BOOST pin is used to supply voltage for the driver of the high-side N-Channel power MOSFET. Connect the bootstrap capacitor to this pin.

Switch Node Pin (SW)

The switch node pin is connected internally to the source of the high-side N-channel MOSFET and externally to the SW node consisting of the inductor, Schottky diode and bootstrap capacitor. The external components must be placed as close as possible to the SW pin such that the switching node is minimized as much as possible.

Exposed Pad (EP)

The Exposed Pad is not electrically connected to the GND pin. Connect with thermal vias to the ground plane to ensure adequate heat-sinking.

5. Functional Description

The MCP16364/5/6 is a high input voltage step-down regulator, capable of supplying 1A to a regulated output voltage from 2.0V to 24V. Internally, the trimmed 2.2 MHz oscillator provides a fixed frequency, while the Peak Current Mode Control architecture varies the duty cycle for output voltage regulation. An internal floating driver is used to turn the high-side integrated N-Channel MOSFET on and off. The power for this driver is derived from an external bootstrap capacitor whose energy is supplied from a fixed voltage ranging between 3.0V and 5.5V, typically the input or output voltage of the converter. For applications with an output voltage outside of this range, 12V for example, the bootstrap capacitor bias can be derived from the output using a simple Zener diode regulator.

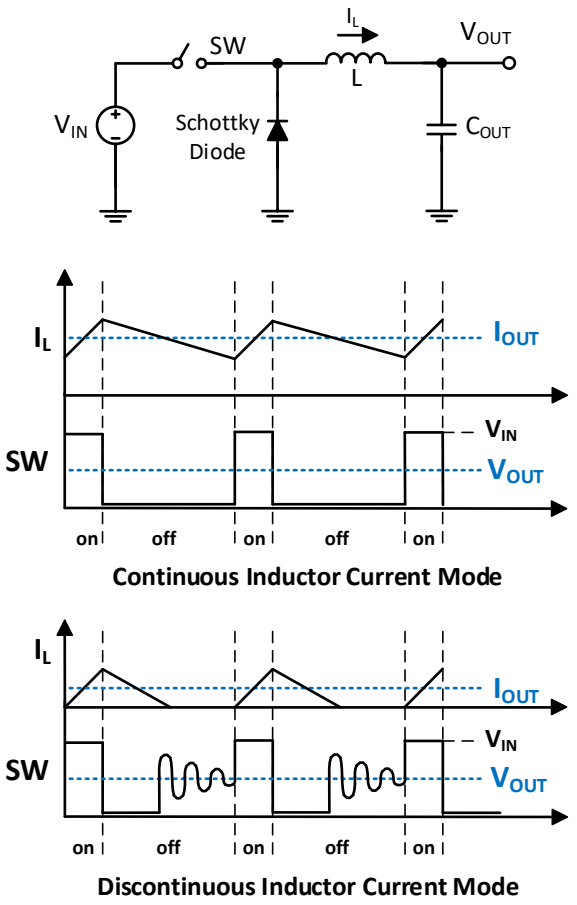
5.1 Theory of Operation

The integrated high-side switch is used to chop or modulate the input voltage using a controlled duty cycle for output voltage regulation. High efficiency is achieved by using a low-resistance switch, low forward voltage drop diode, low equivalent series resistance inductor (DCR) and capacitor (ESR). When the switch is turned on, a DC voltage is applied to the inductor ($V_{IN} – V_{OUT}$), resulting in a positive linear ramp of inductor current. When the switch is turned off, the applied inductor voltage is equal to $-V_{OUT}$, resulting in a negative linear ramp of inductor current (ignoring the forward voltage drop of the Schottky diode).

For steady-state, continuous inductor current operation, the positive inductor current ramp must equal the negative current ramp in magnitude. While operating in steady state, the switch duty cycle must be equal to the relationship of V_{OUT}/V_{IN}, for constant output voltage regulation, under the condition that the inductor current is continuous or never reaches zero. For discontinuous inductor current operation, the steady-state duty cycle will be less than V_{OUT}/V_{IN} to maintain voltage regulation. The average of the chopped input voltage or SW node voltage is equal to the output voltage, while the average of the inductor current is equal to the output current.

For a graphical representation of the switching waveform and inductor current for continuous and discontinuous inductor current modes, see Figure 5-1.

Figure 5-1. Step-Down Converter



The MCP16364/5/6 integrates a Peak Current Mode Control architecture, resulting in superior AC regulation while minimizing the number and size of the voltage loop compensation components integrated in the device. Peak Current Mode Control takes a small portion of the inductor current, replicates it and compares this replicated current sense signal with the output voltage of the integrated error amplifier. In practice, the inductor current and the internal switch current are equal during the switch-on time. By adding this peak current sense to the system control, the step-down power train system is reduced from a 2nd order to a 1st order. This reduces the system complexity and increases its dynamic performance.

5.2 Pulse-Width Modulation

For Pulse-Width Modulation (PWM) duty cycles that exceed 50%, the control system can become bimodal, where a wide pulse followed by a short pulse repeats instead of the desired fixed pulse width. To prevent this mode of operation, an internal compensating ramp is summed into the current shown in Figure 5-1.

The internal oscillator starts the switching period, which for MCP16364/5/6 occurs at a 2.2 MHz frequency. With the integrated switch turned on, the inductor current ramps up until the sum of the current sense and slope compensation ramp exceeds the integrated error amplifier output. The error amplifier output slews up or down to increase or decrease the inductor peak current feeding into the output LC filter. If the regulated output voltage is lower than its target, the inverting error amplifier output rises. This results in an increase in the inductor current, to correct for error in the output voltage. The fixed frequency duty cycle is terminated when the sensed inductor peak current summed with the internal slope compensation exceeds the output voltage of the error amplifier. The PWM latch is set by turning off the internal switch and preventing it from turning on until the

beginning of the next cycle. An overtemperture signal or bootstrap capacitor undervoltage can also reset the PWM latch to asynchronously terminate the switching cycle.

5.3 Pulse Frequency Mode of Operation (PFM)

The MCP16364 selects the best operating switching mode (PFM or PWM) for high efficiency across a wide range of load currents, while in PFM, the duty cycle is determined by a fixed peak current. This allows for the output voltage to increase slightly above the typical regulation point. When the output voltage increases and the feedback voltage exceeds 810 mV typical, the MCP16364 stops switching and enters Sleep mode. The part resumes normal operation when the output voltage decreases. Switching to PFM mode at light load currents, combined with the very low I_Q current when not switching, results in obtaining very high efficiency at very low loads. During the sleep period (between two switching packets), the MCP16364 draws 18 µA (typical) from the supply line. The switching pulse packets represent a small percentage of the total running cycle, and the overall average current drawn from power line is small.

The disadvantages of the PFM/PWM mode are higher output voltage ripple and variable PFM mode frequency. The PFM mode threshold is a function of the input voltage, output voltage and load.

5.4 Internal Reference Voltage V_{REF}

An integrated precise 0.8V reference combined with an external resistor divider sets the desired converter output voltage. The resistor divider range can vary without affecting the control system gain. High-value resistors consume less current but are more susceptible to noise.

5.5 Internal Compensation

All control system components necessary for stable operation over the entire device operating range are integrated, including the error amplifier and inductor current slope compensation. To add the proper amount of slope compensation, the inductor value changes along with the output voltage (see Table 8-1).

5.6 Enable Input

Enable (EN) input is used to disable the device. If disabled, the MCP16364/5/6 device consumes a minimal amount of current from the input. When enabled, the internal soft start controls the output voltage rate of rise, preventing high-inrush current and output voltage overshoot. To achieve automatic turn-on as soon as enough voltage is present, connect the EN to the input.

5.7 Soft Start

The internal reference voltage rate of rise is controlled during start-up, minimizing the output voltage overshoot and the inrush current. The soft-start time is typically 750 µs.

5.8 Undervoltage Lockout

An integrated Undervoltage Lockout (UVLO) prevents the converter from starting until the input voltage is high enough for normal operation. The converter will typically start at 4V and operate down to 3.6V. Hysteresis is added to prevent starting and stopping during start-up as a result of loading the input voltage source.

5.9 Overtemperature Protection

Overtemperature protection limits the silicon die temperature to 155°C by turning the converter off. The normal switching resumes at 125°C.

5.10 High-Side Drive and Bootstrap

The MCP16364 features an integrated high-side N-Channel MOSFET for high efficiency step-down power conversion. An N-Channel MOSFET is used for its low resistance and size (instead of a P-Channel MOSFET). The N-Channel MOSFET gate must be driven above its source to fully turn on the transistor. A gate drive voltage above the input supply is necessary to turn on the high-side N-Channel MOSFET. The high-side drive voltage must be between 3.0V and 5.5V.

The N-Channel MOSFET source is connected to the inductor and Schottky diode or switch node. When the switch is off, the inductor current flows through the Schottky diode, providing a path to recharge the bootstrap capacitor from the boost voltage source, typically the output voltage for 3.0V to 5.5V output applications.

Prior to start-up, the bootstrap capacitor has no stored charge to drive the switch. An internal regulator is used to *precharge* the bootstrap capacitor. When precharged, the switch is turned on and the inductor current starts to flow. When the switch turns off, the inductor current free-wheels through the Schottky diode, providing a path to recharge the bootstrap capacitor. Worst case conditions for recharge occur when the switch turns off for a very short time, at light load, limiting the inductor current ramp. In this case, there is a small amount of time for the bootstrap capacitor to recharge. For high-input voltages, there is enough precharge current to replenish the bootstrap capacitor charge. For input voltages above 5.5V typical, the MCP16364/5/6 device will regulate the output voltage with no load. After starting, the MCP16364/5/6 will regulate the output voltage until the input voltage decreases below 4V.

5.11 Integrated Bootstrap Diode

To minimize the number of external components used in the application, the bootstrap diode was integrated into the device such that the anode is connected to the BD pin and cathode to the BOOST pin.

The permissible voltage to be used on this pin is between 3V and 5.5V.

5.12 Frequency Dithering

When designing a DC-DC switching power supply, one of the challenges that must be overcome is controlling the electromagnetic interference (EMI) emissions produced during normal operation. The EMI is most relevant at the switch mode power supply fundamental switching frequency and is reduced for each higher order harmonic. To decrease this peak emission, modulating or dithering the switching frequency is used so that the EMI is spread over a band of frequencies.

For the MCP16366, the switching frequency will vary above the 2.2 MHz by +10% to reduce the EMI peak.

5.13 Power Good

Power Good (PG) is an open-drain output. For asserting a logic-high level, PG requires an external resistor connected to a pull-up voltage, which must not exceed the input voltage.

PG is asserted when the output voltage reaches 93% of its target regulation voltage. PG is deasserted with a typical delay of 50 µs when the output voltage falls below 90% of its target regulation voltage. The PG falling delay acts as a deglitch timer against very short spikes. The PG output is always immediately deasserted when the EN pin is below the power delivery enable threshold. The value of the pull-up resistor must be high enough to limit the PG pin current to below 5 mA.

The PG is also immediately deasserted (with no delay) whenever an undervoltage condition is detected or for a thermal shutdown.

5.14 Overcurrent Protection

The MCP16364/5/6 features instantaneous cycle-by-cycle current limit by sensing the current through the high-side switch.

A leading edge blanking is provided on the high-side switch to prevent falsely triggering the overcurrent limit.

The device also offers frequency fold-back and overcurrent protection that inhibits future pulses for prolonged overloads or short-circuit condition.

If prolonged overloads at high input voltages occur and the overcurrent protection is tripped, the next three switching pulses will be inhibited such that the inductor current is allowed to decrease to lower values.

At the same time, if the feedback voltage decreases, the switching frequency will also decrease down to 200 kHz.

5.15 Overvoltage Protection

The MCP16364/5/6 incorporates an Overvoltage Protection (OVP) to minimize the output voltage overshoot when recovering from strong unload transients in designs with low-output capacitance. For example, in applications where the output voltage is overloaded when the load is removed, the regulator output can increase faster than the response of the error amplifier, resulting in an output overshoot.

The OVP circuitry compares the FB voltage to the OVP threshold, which is typically set at 860 mV, and immediately turns off the high-side MOSFET.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameters	Minimum	Maximum	Unit
VIN, SW	-0.5	+53	V
BOOST – GND	-0.5	+60	V
BOOST – SW Voltage	-0.5	+5.5	V
FB, BD	-0.5	+5.5	V
PG, EN	-0.5	V_{IN} + 0.3	V
Storage Temperature	-65	+150	°C
Operating Junction Temperature	-40	+125	°C

Table 6-2. ESD Protection on All Pins

Parameters	Minimum	Maximum	Unit
HBM	-2	+2	kV
CDM	-2	+2	kV

Note: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

Electrical Characteristics: Unless otherwise indicated, $T_A = T_J$ = +25°C, $V_{IN} = V_{EN}$ = 12V, $V_{BOOST} - V_{SW}$ = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 100 mA, L = 3.9 µH, C_{IN} = 10 µF X7R Ceramic Capacitor, C_{OUT} = 2 x 10 µF X7R Ceramic Capacitors. **Boldface** specifications apply over the T_J range of -40°C to 125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Voltage	V_{IN}	**4.1**	—	**48**	V	**Note 1**
Feedback Voltage	V_{FB}	**0.776**	0.800	**0.824**	V	V_{IN} = 12V, PWM mode, Standard Part
		0.784	0.800	**0.816**	V	V_{IN} = 12V, PWM mode, AEC-Q100 Automotive Qualified
Output Voltage Adjust Range	V_{OUT}	**2**	—	**24**	V	**Note 2**, **Note 4**
Feedback Voltage Line Regulation	$(\Delta V_{FB}/V_{FB})/\Delta V_{IN}$	—	0.01	—	%/V	MCP16365, V_{IN} = 5V to 16V
Feedback Voltage Load Regulation	$(\Delta V_{FB}/V_{FB})$	—	0.3	—	%	MCP16365, I_{OUT} = 10 mA to 1A
Feedback Input Bias Current	I_{FB}	—	+/- 10	—	nA	Sink/Source
Undervoltage Lockout Start	$UVLO_{STRT}$	—	4	—	V	V_{IN} Rising
Undervoltage Lockout Stop	$UVLO_{STOP}$	—	3.6	—	V	V_{IN} Falling
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	0.4	—	V	—

Notes:

1. The input voltage must be > output voltage + headroom voltage; higher load currents increase the input voltage necessary for regulation. See the characterization graphs for typical input to output operating voltage range.
2. For the conditions explained in Input Voltage Limitations
3. V_{BOOST} supply is derived from V_{OUT}.
4. Determined by characterization; not production tested.

.....continued

Electrical Characteristics: Unless otherwise indicated, $T_A = T_J = +25°C$, $V_{IN} = V_{EN} = 12V$, $V_{BOOST} - V_{SW} = 3.3V$, $V_{OUT} = 3.3V$, $I_{OUT} = 100$ mA, L = 3.9 µH, $C_{IN} = 10$ µF X7R Ceramic Capacitor, $C_{OUT} = 2 \times 10$ µF X7R Ceramic Capacitors. **Boldface** specifications apply over the T_J range of -40°C to 125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Switching Frequency	f_{SW}	**1.8**	2.2	**2.6**	MHz	PWM mode
Switching Frequency Dithering	$f_{SW,dither}$	—	+10	—	%	MCP16366
Maximum Duty Cycle	DC_{MAX}	—	87	—	%	**Note 4**
Minimum On Time	Ton_{MIN}	—	65	—	ns	**Note 4**
NMOS Switch On Resistance	$R_{DS(ON)}$	—	0.5	—	Ω	$V_{BOOST} - V_{SW} = 3.3V$ (**Note 4**)
NMOS Switch Current Limit	$I_{N(MAX)}$	—	1.8	—	A	$V_{BOOST} - V_{SW} = 3.3V$ (**Note 4**)
Quiescent Current – PWM	$I_{Q,PWM}$	—	1.8	**3.8**	mA	$V_{BOOST} = 3.3V$; MCP16365 Switching
Quiescent Current – PFM	$I_{Q,PFM}$	—	55	**135**	µA	$V_{BOOST} = 3.3V$; MCP16364 Switching
Quiescent Current – PFM – Non-Switching	I_Q	—	18	**24**	µA	$V_{BOOST} = 3.3V$; MCP16364 Non-Switching
Quiescent Current – Shutdown	$I_{Q,SHD}$	—	3	**6**	µA	V_{OUT} = EN = 0V
EN Input Logic High	V_{IH}	**1.8**	—	—	V	—
EN Input Logic Low	V_{IL}	—	—	**0.4**	V	—
EN Input Leakage Current	I_{ENLK}	—	0.1	**0.15**	µA	$V_{EN} = 12V$
Soft-Start Time	t_{SS}	—	750	—	µs	EN Low to High, 90% of V_{OUT} (**Note 4**)
Power Good Threshold	V_{PG}	**89**	93	**97**	%	—
Power Good Hysteresis	$V_{PG,hyst}$	—	3	—	%	—
Power Good Blanking	$PG_{Blanking}$	—	55	**57**	µs	**Note 4**
Thermal Shutdown Die Temperature	T_{SD}	—	155	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	25	—	°C	—

Notes:

1. The input voltage must be > output voltage + headroom voltage; higher load currents increase the input voltage necessary for regulation. See the characterization graphs for typical input to output operating voltage range.
2. For the conditions explained in Input Voltage Limitations
3. V_{BOOST} supply is derived from V_{OUT}.
4. Determined by characterization; not production tested.

6.3 Temperature Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady State
Storage Temperature Range	T_A	-65	—	+150	°C	—
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Package Thermal Resistances						
Thermal Resistance Junction to Ambient (**Note 1**)	$R_{\theta JA}$	—	61.1	—	°C/W	—
Thermal Resistance Junction to Case (**Note 1**)	$R_{\theta JC}$	—	76.4	—	°C/W	—
Thermal Resistance Junction to Top of Package (**Note 1**)	Ψ_{JT}	—	2.4	—	°C/W	—
Thermal Resistance Junction to Board (**Note 1**)	$R_{\theta JB}$	—	21.8	—	°C/W	—
Thermal Resistance Junction to Board Characterization Parameter (**Note 1**)	Ψ_{JB}	—	15.8	—	°C/W	—

Note:

1. Simulated on the MCP16364/5/6 Evaluation Board EV61A73A, a 50 mm x 50 mm, 1 oz, 2-layer PCB.

7. Typical Performance Curves

Notes:

- The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and, therefore, outside the warranted range.
- Unless otherwise indicated, T_A = +25°C, V_{IN} = V_{EN} = 12V, V_{BOOST} – V_{SW} = 5V, V_{OUT} = 5V, I_{OUT} = 100 mA, L = 5.6 µH, C_{IN} = 10 µF X7R Ceramic Capacitor, C_{OUT} = 2 x 10 µF X7R Ceramic Capacitors.

Figure 7-1. 3.3V V_{OUT} Efficiency vs. I_{OUT}

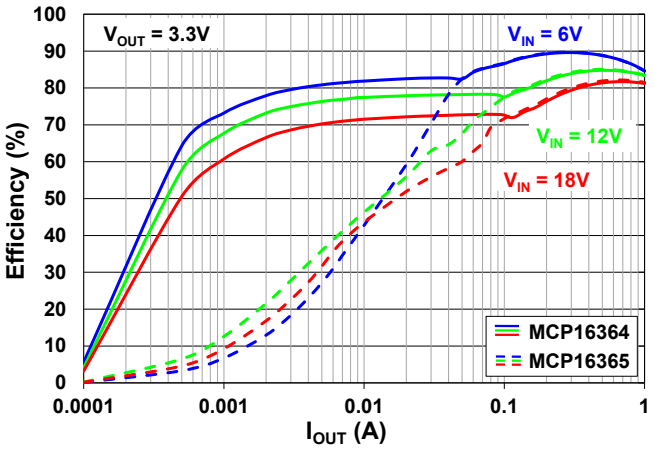


Figure 7-2. 3.3V V_{OUT} vs. I_{OUT}

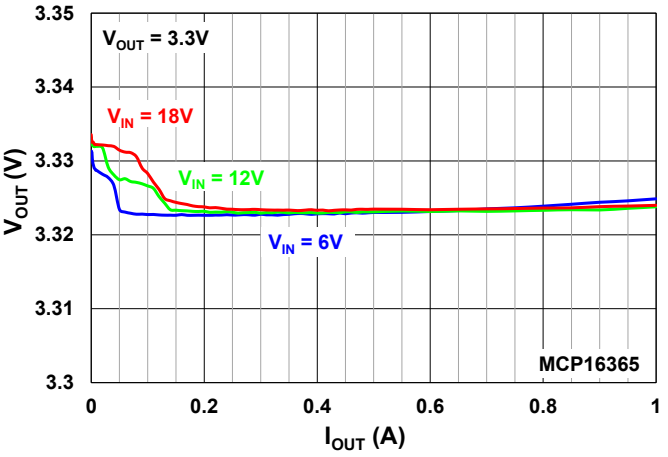


Figure 7-3. 5V V_{OUT} Efficiency vs. I_{OUT}

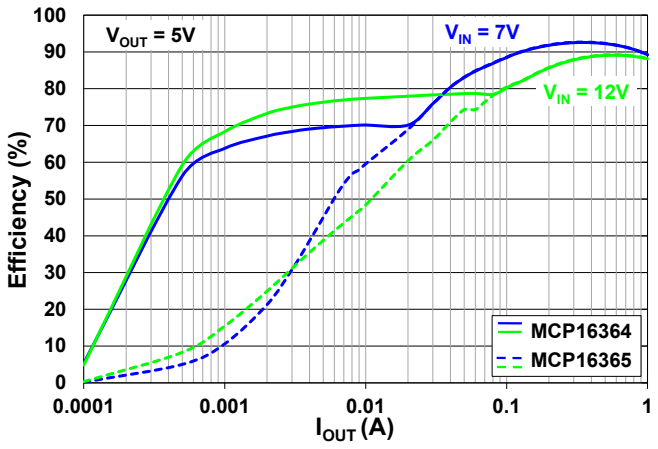


Figure 7-4. 5V V_{OUT} vs. I_{OUT}

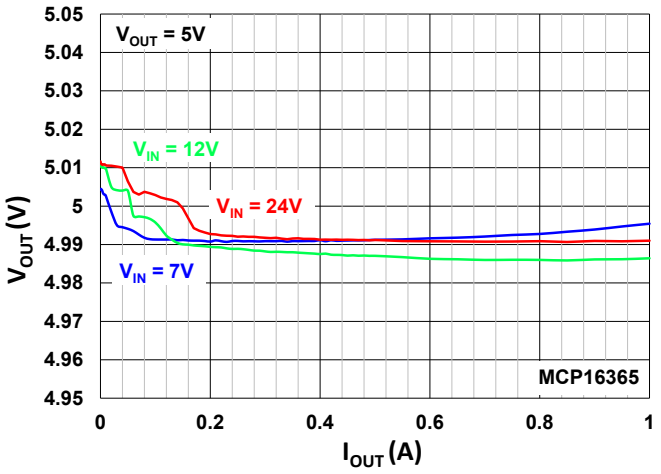


Figure 7-5. 12V V_{OUT} Efficiency vs. I_{OUT}

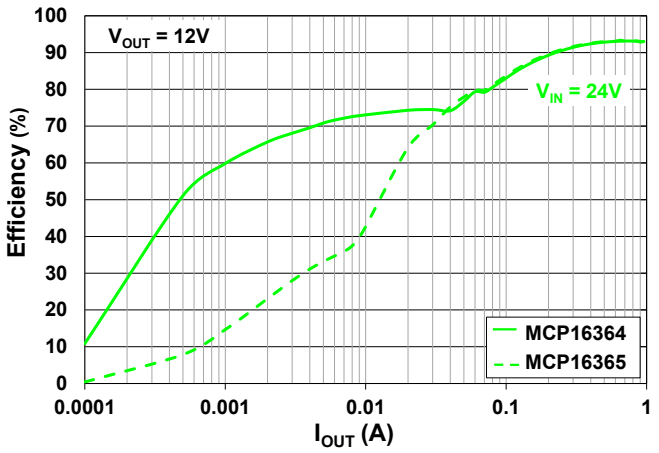


Figure 7-6. 12V V_{OUT} vs. I_{OUT}

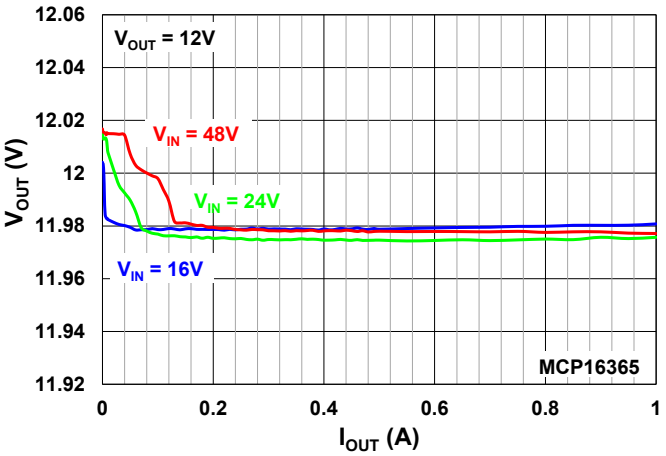


Figure 7-7. V_{OUT} vs. V_{IN}

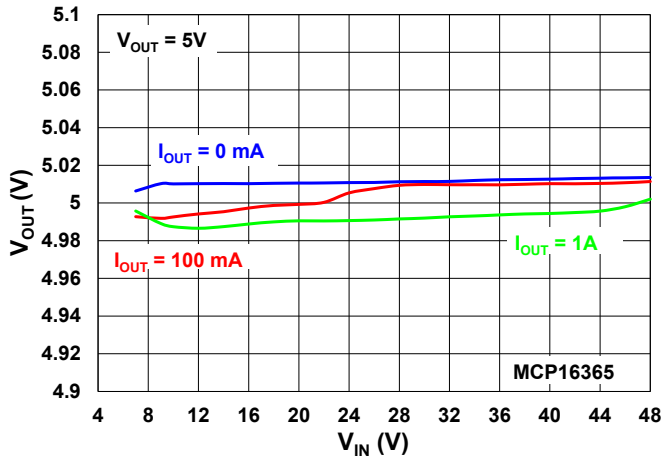


Figure 7-8. Switch R_{DSON} vs. Temperature

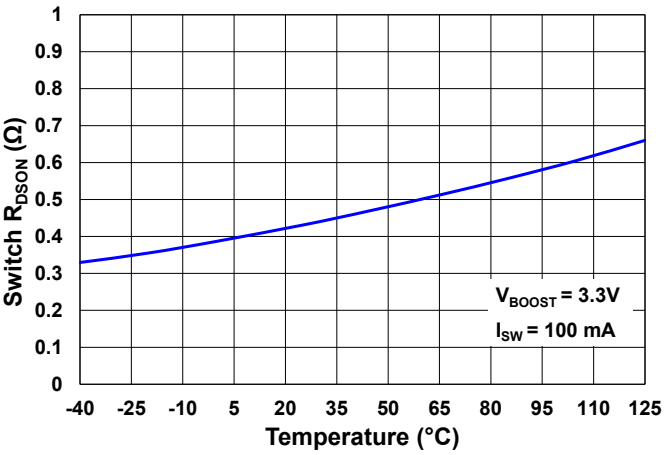


Figure 7-9. V_{FB} vs. Temperature

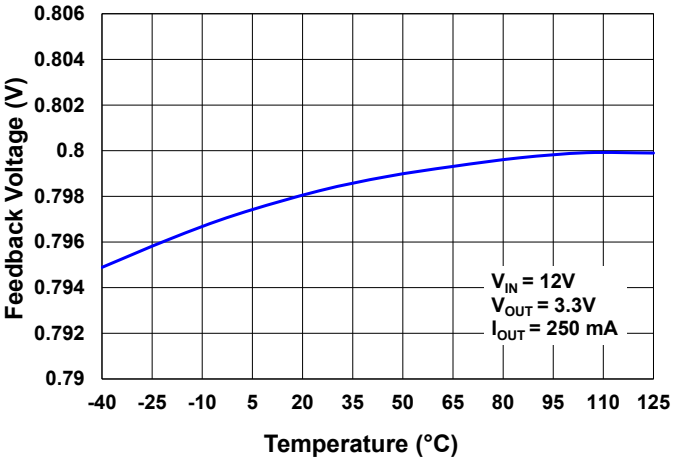


Figure 7-10. Switch R_{DSON} vs. V_{BOOST}

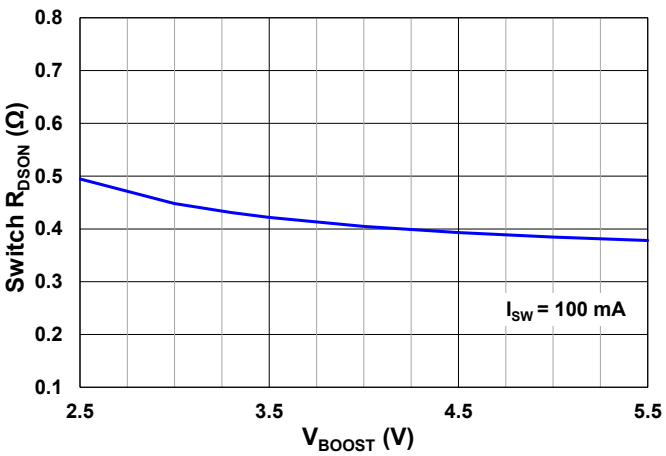


Figure 7-11. Peak Current Limit vs. Temperature

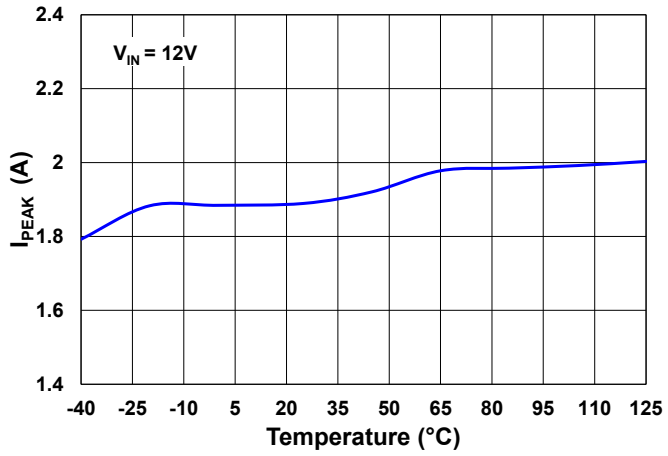


Figure 7-12. Undervoltage Lockout vs. Temperature

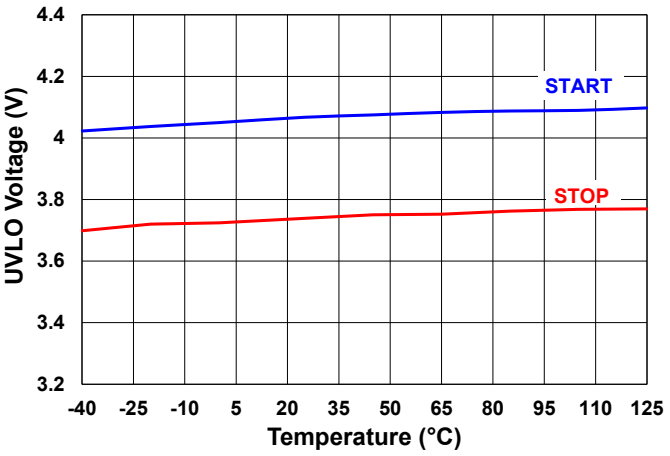


Figure 7-13. EN Threshold Voltage vs. Temperature

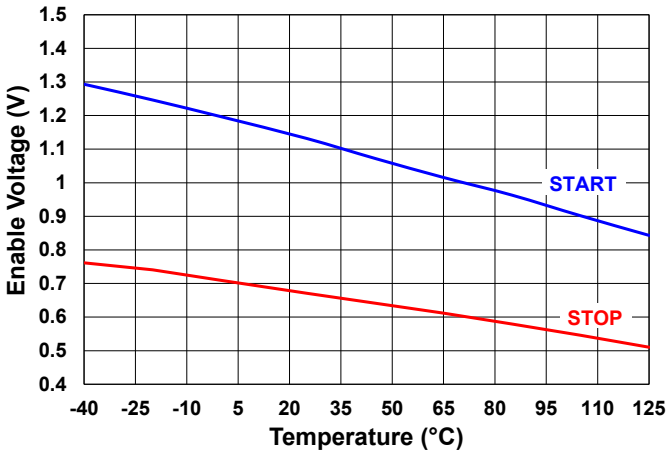


Figure 7-14. No Load Input Current vs. V_{IN}, MCP16364

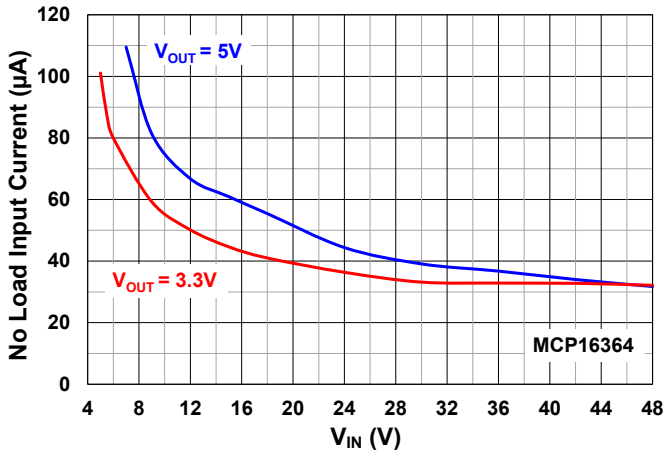


Figure 7-15. Input Quiescent Current vs. V_{IN}

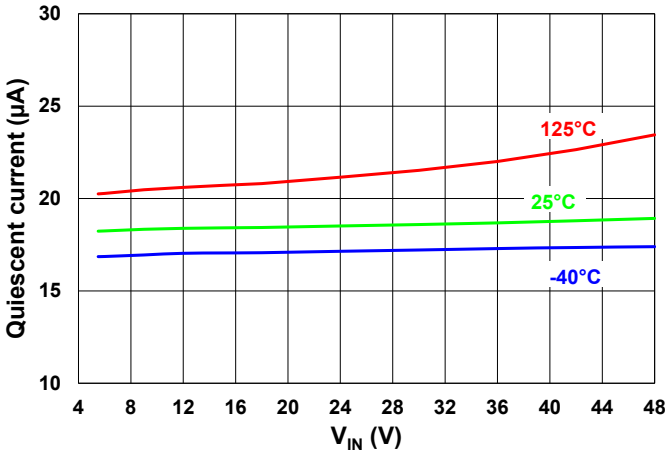


Figure 7-16. No Load Input Current vs. V_{IN}, MCP16365

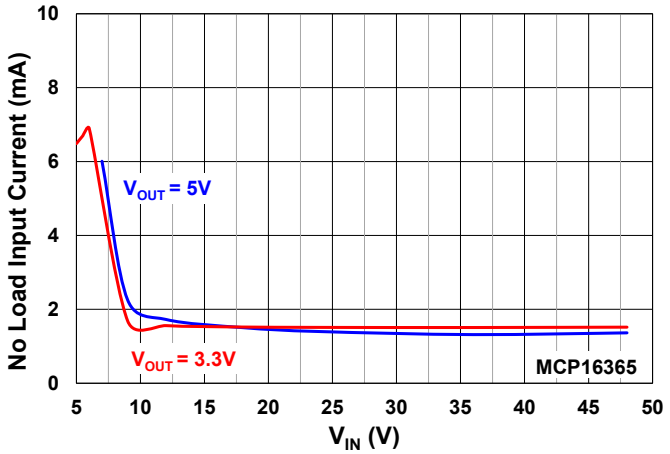


Figure 7-17. Shutdown Current vs. V_{IN}

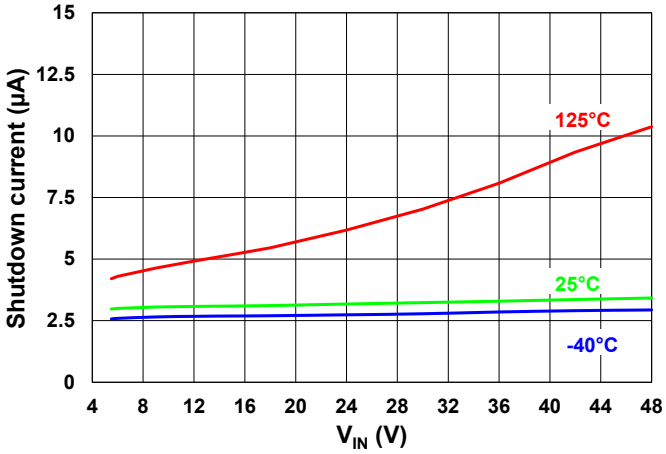


Figure 7-18. PFM/PWM Threshold

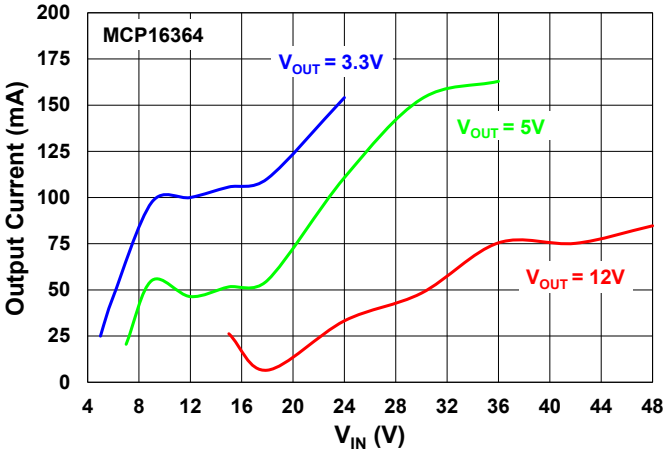


Figure 7-19. PWM/Skipping Threshold

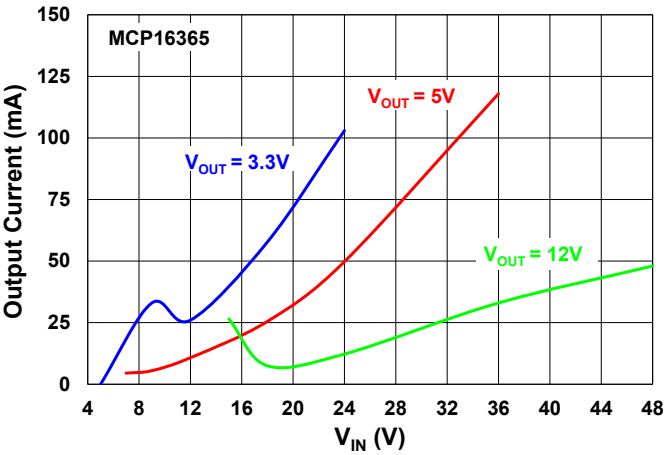


Figure 7-20. Switching Frequency vs. Feedback Voltage

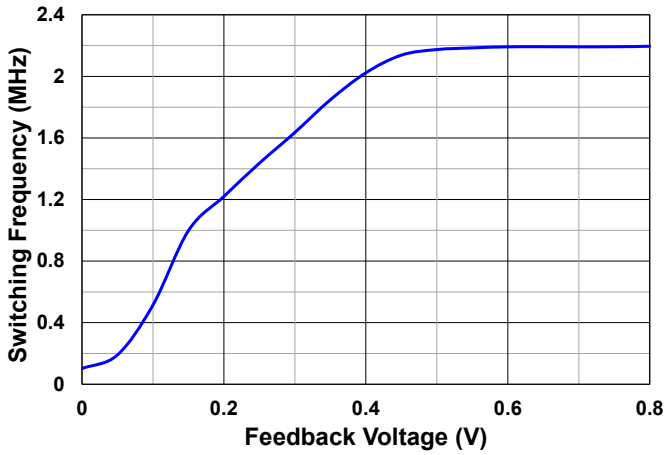


Figure 7-21. Minimum Input Voltage vs. Output Current

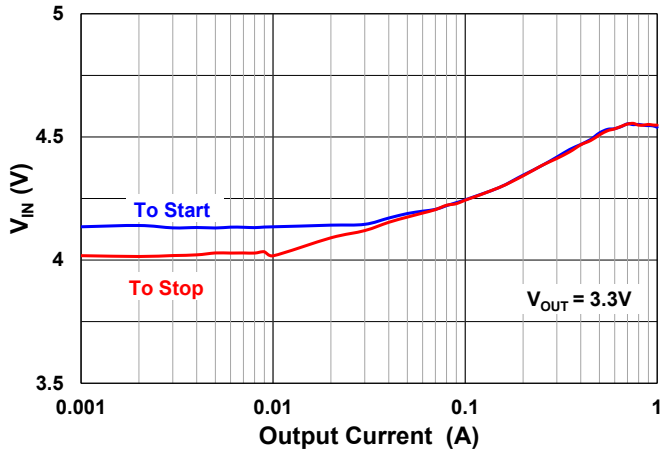


Figure 7-22. Switching Frequency vs. Temperature

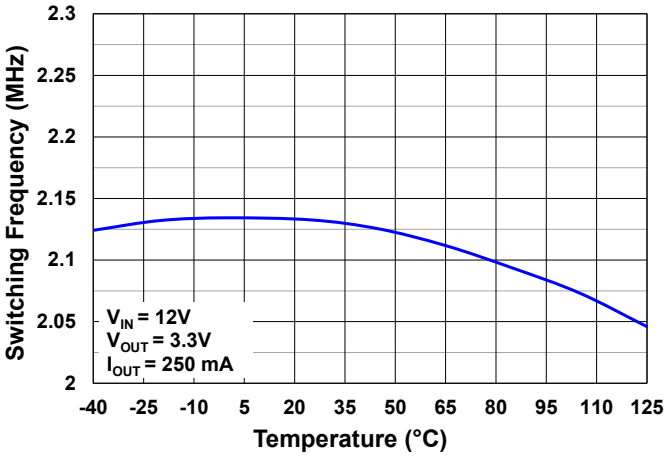


Figure 7-23. Heavy Load Switching Waveforms

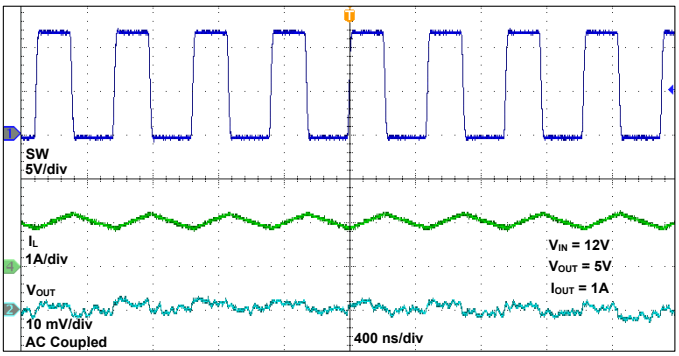


Figure 7-24. PFM to PWM Transition

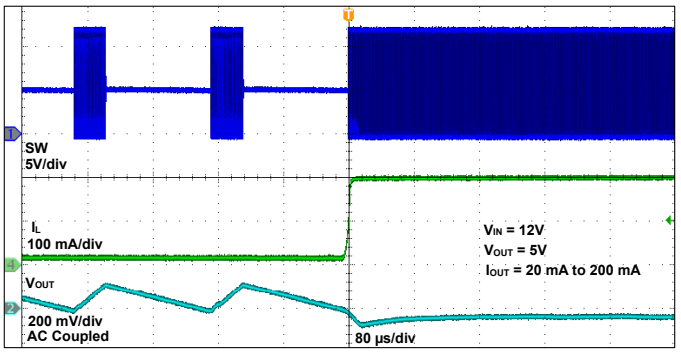


Figure 7-25. Light Load Switching Waveforms – MCP16364

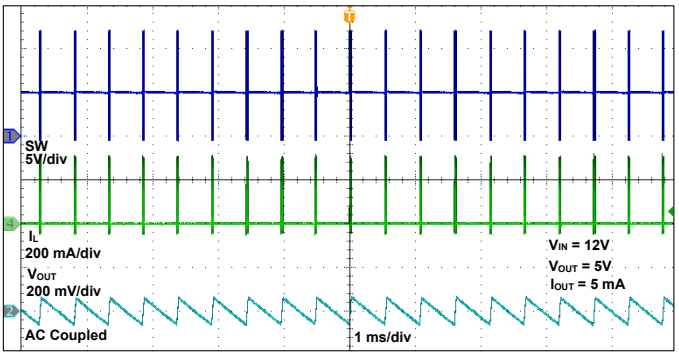


Figure 7-26. Start-Up from V_{IN}

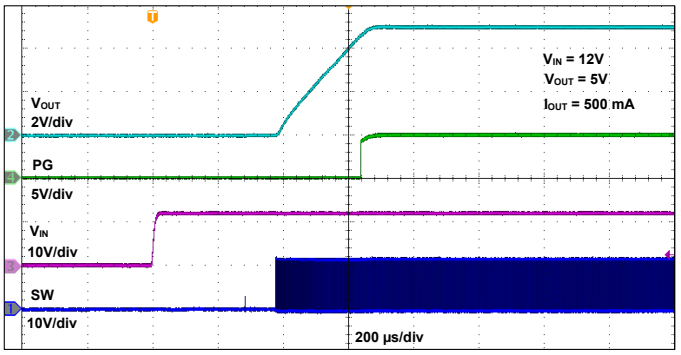


Figure 7-27. Light Load Switching Waveforms – MCP16365

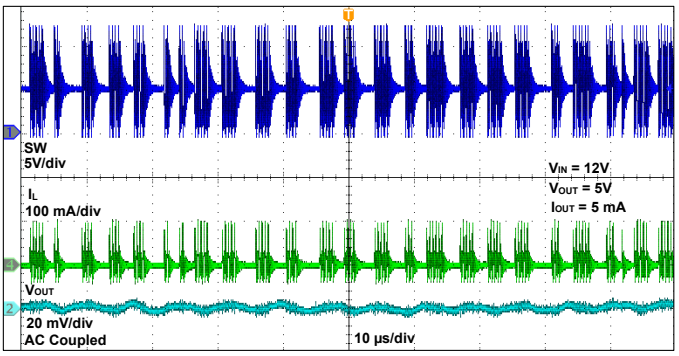


Figure 7-28. Start-Up from EN

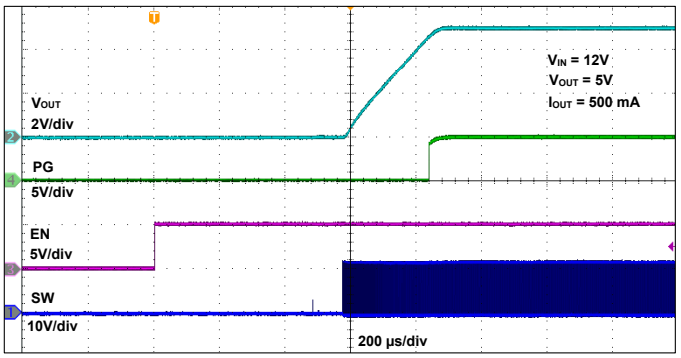


Figure 7-29. MCP16365 Load Transient Response (2.5 mA to 400 mA)

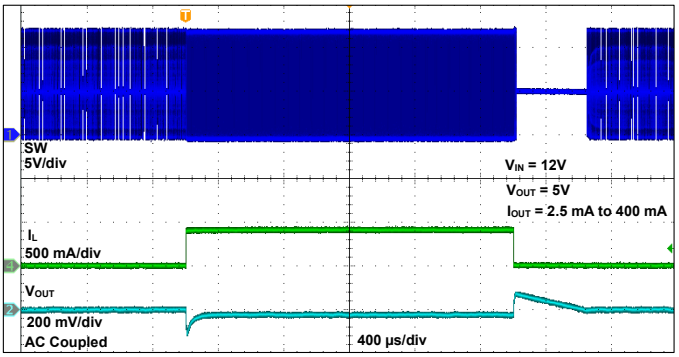


Figure 7-30. MCP16365 Load Transient Response (200 mA to 800 mA)

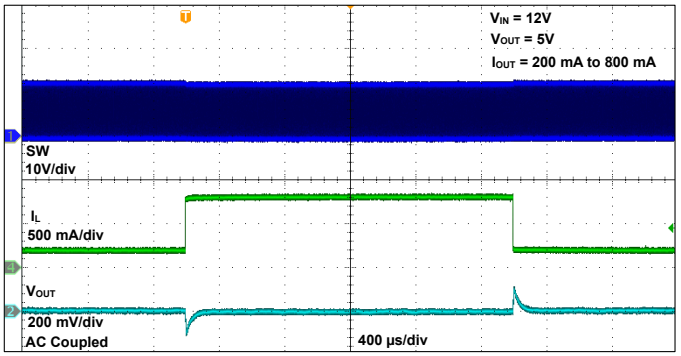
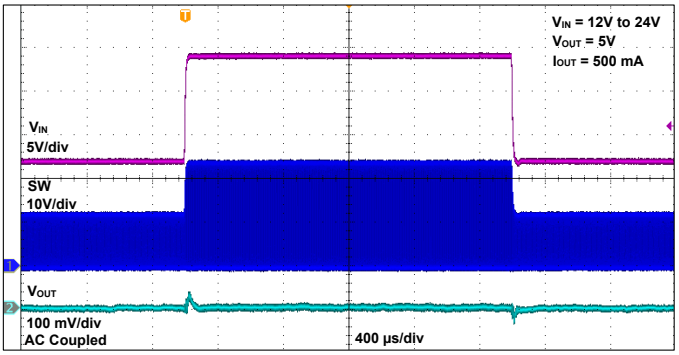


Figure 7-31. Line Transient Response



8. Application Information

8.1 Adjustable Output Voltage Calculations

To calculate the resistor divider values for the MCP16364/5/6, the equation below can be used. R_{TOP} is connected to V_{OUT}, R_{BOT} is connected to GND, and both are connected to the FB input pin.

Equation 8-1. Resistor Divider Values

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

3.3V Output Example

V_{OUT_target}	=	3.3V
V_{FB}	=	0.8V
R_{BOT}	=	10 kΩ
R_{TOP}	=	31.25 kΩ (Standard Value = 31.6 kΩ)

The transconductance error amplifier gain is controlled by its internal impedance. The external divider resistors have no effect on system gain, so a wide range of values can be used. It is recommended to use feedback resistors with 1% tolerances or better. To improve the efficiency at light load, using large value resistors is recommended. However, if the values are too high, the regulator will be more susceptible to noise.

8.2 Inductor Selection and Slope Compensation

To select the best inductor for the application, the following factors must be considered: inductance value, RMS rated current, saturation current and DC Resistance (DCR).

The inductance value is critical to correctly operate the MCP16364/5/6. For stable current loop operation where duty cycle is above 50%, slope compensation is internally added according to the output voltage and the input-output voltage ratio.

For the proper amount of slope compensation, it is recommended to keep the inductor down-slope current constant by varying the inductance with V_{OUT}.

Table 8-1. Recommended Inductor Values

V_{OUT}	$L_{STANDARD}$
2.0V	2.2 µH
3.3V	3.9 µH
5.0V	5.6 µH
12V	15 µH
15V	15 µH

The inductor RMS current represents the current at which the inductor's temperature rises by +20°C to +40°C, depending on the manufacturer. For the inductor saturation current, it represents the peak current where the inductor exhibits a loss of inductance value between 10% and 30%, depending on the manufacturer. For proper operation, ensure that the nominal and peak currents of the application are well within the permissible current ratings of the inductor.

The peak inductor current can be calculated with Equation 8-2:

Equation 8-2. Peak Inductor Current

$$I_{LPEAK} = \left(I_{OUT} + V_{OUT} \times \frac{1 - V_{OUT}/V_{IN}}{2 \times f_{sw} \times L}\right)$$

Where:

I_{OUT}	=	Nominal output current
V_{OUT}	=	Output voltage
V_{IN}	=	Input voltage
f_{SW}	=	Switching frequency
L	=	Inductance value

When choosing the inductor, sufficient design margin must be taken into account such that the inductor does not enter deep saturation. Overcurrent situations must also be taken into account, especially at very high input voltages where the inductor current can increase very rapidly.

8.3 Freewheeling Diode

The MCP16364/5/6 requires a freewheeling diode to create a path for the inductor current flow after the internal switch is turned off. The diode must have a reverse voltage rating greater than the maximum input voltage possible in the application. The peak current rating of the diode must be higher than the maximum inductor current. The lower the forward voltage of the diode, the higher the efficiency of the regulator, and that is why Schottky diodes are typically a good choice for this purpose.

On the other hand, the diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch, and, therefore, in high V_{IN} to V_{OUT} ratios, the conduction losses of the diode may become significant. The conduction losses can be estimated using Equation 8-3.

Equation 8-3. Diode Conduction Losses

$$P_D = \frac{(V_{IN} - V_{OUT}) \times I_{OUT} \times V_{FW}}{V_{IN}}$$

Where:

I_{OUT}	=	Nominal output current
V_{OUT}	=	Output voltage
V_{IN}	=	Input voltage
V_{FW}	=	Forward voltage drop of the diode

Because of the high switching frequency, the AC losses of the diode must also be taken into account. These losses are caused by the charging and discharging of the junction capacitance and the reverse recovery charge.

8.4 Input Capacitor Selection

The step-down converter input capacitor must filter the high input current ripple as a result of pulsing or chopping the input voltage. The MCP16364/5/6 input voltage pin is used to supply voltage for the power train and as a source for internal bias. A low equivalent series resistance (ESR), preferably a ceramic capacitor of at least 10 µF capacitance, is recommended. Depending on the loading profile and conditions, the application will benefit from additional bulk capacitance.

The minimum capacitance needed for a given input peak-to-peak voltage ripple can be calculated using Equation 8-4:

Equation 8-4. Input Capacitor Ripple

$$C_{IN(MIN)} = \frac{I_{OUT} \times D \times (1 - D)}{\Delta V_{ripple,in} \times f_{SW}}$$

Where:

I_{OUT}	=	Nominal output current
D	=	Duty-cycle
$\Delta V_{ripple,in}$	=	Required input voltage ripple
f_{SW}	=	Switching frequency

The value of ceramic capacitors varies significantly with temperature and DC bias; therefore, design margins must be taken into account to ensure enough capacitance at the input of the regulator. To mitigate temperature variations, X5R and X7R capacitors are recommended. The DC bias must also be considered, as the capacitance decreases with the voltage applied.

8.5 Output Capacitor Selection

The output capacitor helps in providing a stable output voltage during sudden load transients and reduces the output voltage ripple. As with the input capacitor, X5R and X7R ceramic capacitors are well suited for this application.

The output capacitor voltage rating must be a minimum of V_{OUT} plus margin.

To determine the steady-state voltage ripple, the ESR component and the capacitive ripple need to be taken into account (Equation 8-5):

Equation 8-5. Output Capacitor Ripple

$$\Delta V_{ripple,out} = ESR \times \Delta I_L + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

Where:

ESR	=	Output capacitor series resistance
f_{SW}	=	Switching frequency
C_{OUT}	=	Output capacitance
ΔI_L	=	Inductor current ripple

The worst case load transient for output capacitor calculations is an instantaneous load release from full load to no load. In this situation, the energy stored in the inductor, which is at its peak value, must be absorbed by the output capacitor.

The output voltage overshoot in such situations can be calculated using Equation 8-6:

Equation 8-6. Output Voltage Overshoot

$$\Delta V_{OUT} = \sqrt{{V_{OUT}}^2 + \frac{L}{C_{OUT}} \times {I_{LPEAK}}^2} - V_{OUT}$$

Where:

V_{OUT}	=	Output voltage
L	=	Inductance value
I_{LPEAK}	=	Inductor peak current
C_{OUT}	=	Output capacitance

As in the case of the input capacitors, enough design margin needs to be taken into account to mitigate temperature and DC bias variations.

8.6 Bootstrap Charging and Maximum Duty Cycle Limitations

The bootstrap capacitor is used to supply current for the internal high-side drive circuitry that is above the input voltage of the converter. The bootstrap capacitor must store enough energy to completely drive the high-side switch on and off. A 0.1 µF X5R or X7R capacitor is recommended for all applications. The bootstrap capacitor maximum voltage is 5.5V, so a 6.3V- or 10V-rated capacitor is recommended.

The charging of the bootstrap capacitor is done during the off-time of the switching cycle, when the SW node is pulled to GND, through the BD pin. When operating at a low voltage difference between input and output, the duty cycle will reach the maximum limitation at around 87%. This in turn, coupled with the high switching frequency of 2.2 MHz, allows for only 50 ns of charging time for the bootstrap capacitor.

In most cases, this 50 ns time is sufficient to replenish the energy lost for the switching activity during each cycle. However, when the voltage applied on the BD pin is below 3V and the maximum duty cycle is reached, the voltage on the bootstrap capacitor can decrease, reaching 2V and forcing an internal charge of the bootstrap capacitor and, therefore, a stop in switching activity.

To improve the behavior at low input voltages, where the boost charge time reaches 50 ns, the MCP16364/5/6 further limits the maximum duty cycle to 75% typical for input voltage below 5.1V. Due to this, the parts can continue switching and operating correctly, although with a larger headroom between V_{IN} and V_{OUT}. When the V_{IN} recovers and is above 6V, the maximum duty cycle is again set to 87% for normal operation.

When the maximum duty cycle operation is expected to improve the operation at low V_{IN}, an ultra-fast external bootstrap diode can be connected to the boost pin to improve the charging of the bootstrap capacitor.

8.7 Input Voltage Limitations

Although the high switching frequency has advantages when it comes to the requirement of external passive components and possible transient response, when operating in these conditions, there are certain limitations that need to be considered when designing the application:

- Dropout operation
- Minimum on-time

To determine the two ends of the operating range, Equation 8-7 can be used.

Equation 8-7. Input Voltage Range

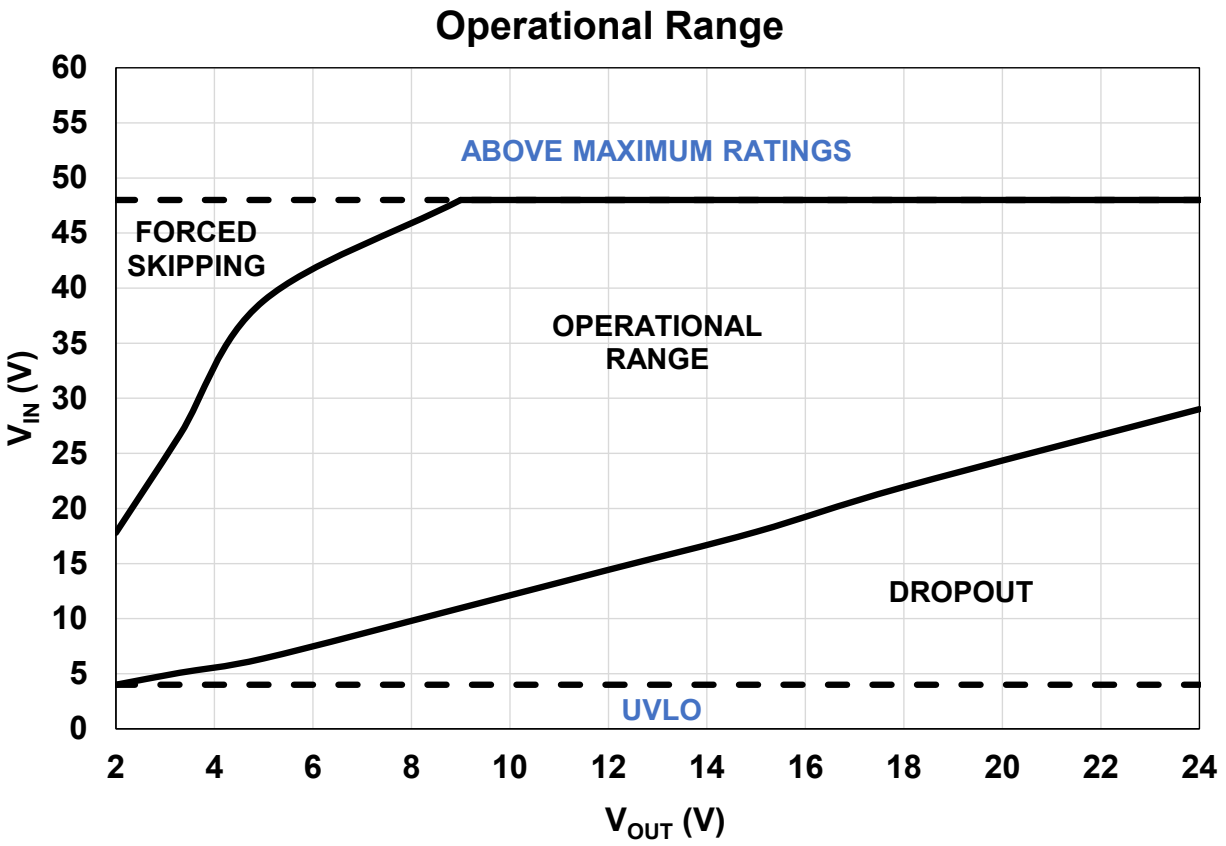
$$V_{IN} = \frac{V_{OUT} + I_{OUT} \times (R_{DCR} + R_{DSON}) + V_{FW} \times (1 - D)}{D}$$

Where:

V_{OUT}	=	Output voltage
I_{OUT}	=	Output current
L	=	Inductance value
R_{DCR}	=	DCR of the selected inductor
R_{DSON}	=	On-resistance of the internal high-side switch
D	=	Duty cycle
V_{FW}	=	Forward voltage drop of the diode

To determine the minimum input voltage required for proper regulation, the duty cycle must be replaced by the maximum duty cycle; whereas, to determine the maximum voltage, the duty cycle must be calculated to avoid going below the minimum on-time.

Figure 8-1. Input Voltage Range vs. Output Voltage



8.8 Light Load Efficiency Guidelines

To increase efficiency at light load conditions, the MCP16364 operates in PFM to keep the output voltage regulated while minimizing the input current consumption. In this mode of operation, the MCP16364 delivers a packet of current pulses that is followed by sleep periods where the output is maintained by the output capacitor. When in the Sleep mode, the MCP16364 consumes around 18 µA from the input. As the output load decreases, the frequency and length of the packet of pulses decrease such that the sleep period extends over most of the time. By maximizing the sleep time, the converter operating no load input current gets closer to the 18 µA value. To optimize the performance at light loads, the current flowing through the feedback resistors and the reverse current through the freewheeling diode must be minimized, as they are seen as load currents. It is recommended that the feedback resistors be in the order of tens of kΩ in range and that the freewheeling diode reverse current be less than 1 µA at room temperature.

8.9 PCB Layout Information

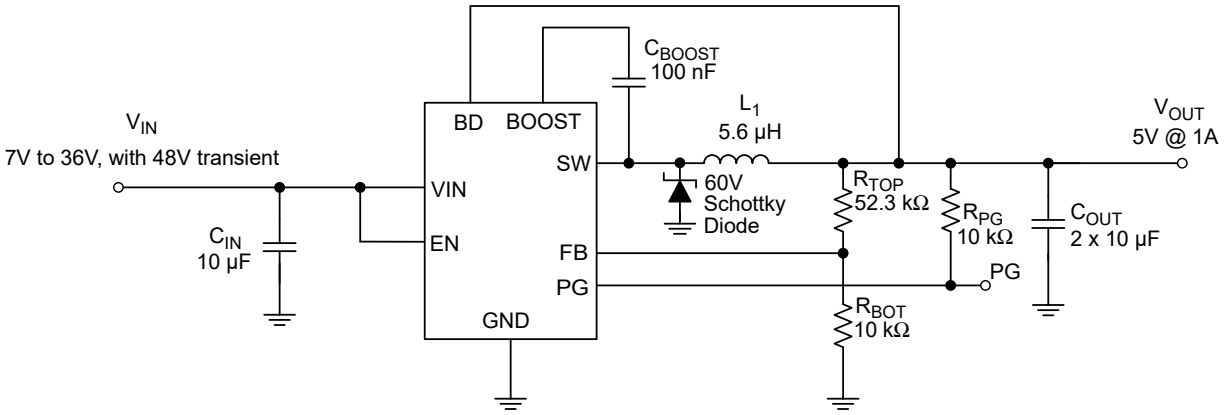
Good printed circuit board layout techniques are important to any switching circuitry, and switch mode power supplies are no different. When wiring the switching high-current paths, short and wide traces must be used. Therefore, it is important that the input and output capacitors be placed as close as possible to the MCP16364/5/6 to minimize the loop area.

The feedback resistors and feedback signal must be routed away from the switching node and the switching current loop. When possible, using ground planes and traces is recommended to help shield the feedback signal and minimize noise and magnetic interference.

A good MCP16364/5/6 layout starts with C_{IN} placement. C_{IN} supplies current to the input of the circuit when the switch is turned on. In addition to supplying high-frequency switch current, C_{IN} also provides a stable voltage source for the internal MCP16364/5/6 circuitry. Unstable PWM operation can result if there are excessive transients or ringing on the VIN pin of the MCP16364/5/6 device. A ground plane on the bottom of the board provides a low resistive and inductive path for the return current. The next priority in placement is the freewheeling current loop formed by the Schottky Diode, C_{OUT} and L, while strategically placing the C_{OUT} return close to ther C_{IN} return. Next, the bootstrap capacitor must be placed between the boost pin and the switch node pin, SW. R_{TOP} and R_{BOT} are routed away from the switch node, so noise is not coupled into the high-impedance FB input.

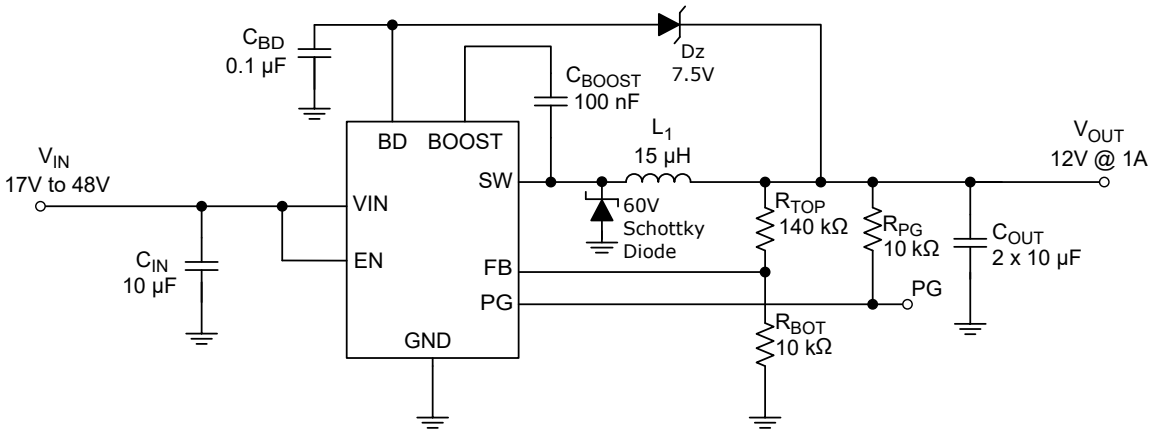
9. Typical Application Circuits

Figure 9-1. Typical Application 7V - 36V V_{IN} (Transient up to 48V) to 5V V_{OUT}.



Component	Value	Manufacturer	Part Number	Comment
C_{IN}	10 µF	TDK Corporation	C5750X7S2A106M	Ceramic Capacitor, 10 µF, 100V, X7S, 2220
C_{OUT}	2 x 10 µF	TDK Corporation	C3216X7R1C106M160AC	Ceramic Capacitor, 10 µF, X7R, 16V, 1206
L_1	5.6 µH	Würth Elektronik	7440700056	5.6 µH, 2.6A, 56 mΩ Shielded Tiny Power Inductor
FW Diode	PMEG6010ER	NXP Semiconductors	PMEG6010ER	Schottky Diode, 60V, 1A, SOD-323
C_{BOOST}	100 nF	KEMET	C0603X104K4RACTU	Ceramic Capacitor, 0.1 µF, 16V, 10%, X7R, SMD, 0603

Figure 9-2. Typical Application 17V - 48V V_{IN} to 12V V_{OUT} with Boost Drive Derived from Output.

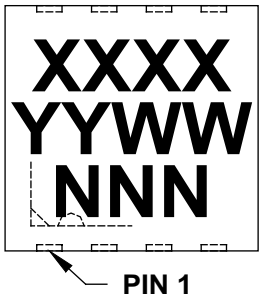


Component	Value	Manufacturer	Part Number	Comment
C_{IN}	10 µF	TDK Corporation	C5750X7S2A106M	Ceramic Capacitor, 10 µF, 100V, X7S, 2220
C_{OUT}	2 x 10 µF	TDK Corporation	C3216X7R1E106M160AB	Ceramic Capacitor, 10 µF, 25V, X7R, 1206
L_1	15 µH	Würth Elektronik	744071150	15 µH, 2.8A, 55 mΩ Shielded Tiny Power Inductor
FW Diode	PMEG6010ER	NXP Semiconductors	PMEG6010ER	Schottky Diode, 60V, 1A, SOD-323
C_{BOOST}	100 nF	KEMET	C0603X104K4RACTU	Ceramic Capacitor, 0.1 µF, 16V, 10%, X7R, SMD, 0603
D_Z	7.5V Zener	Diodes Incorporated®	MMSZ5236BS-7-F	Zener Diode, 7.5V, 200 mW, SOD-323
C_{BD}	0.1 µF	TDK Corporation	C1608X7R1H104K080AA	Ceramic Capacitor, 0.1 µF, 50V, X7R, 0603

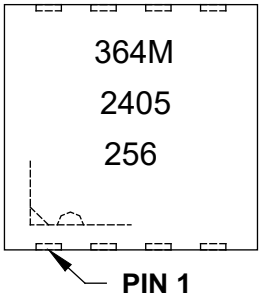
10. Packaging Information

Package Marking Information

8-Lead VDFN (3x3x1 mm)



Example

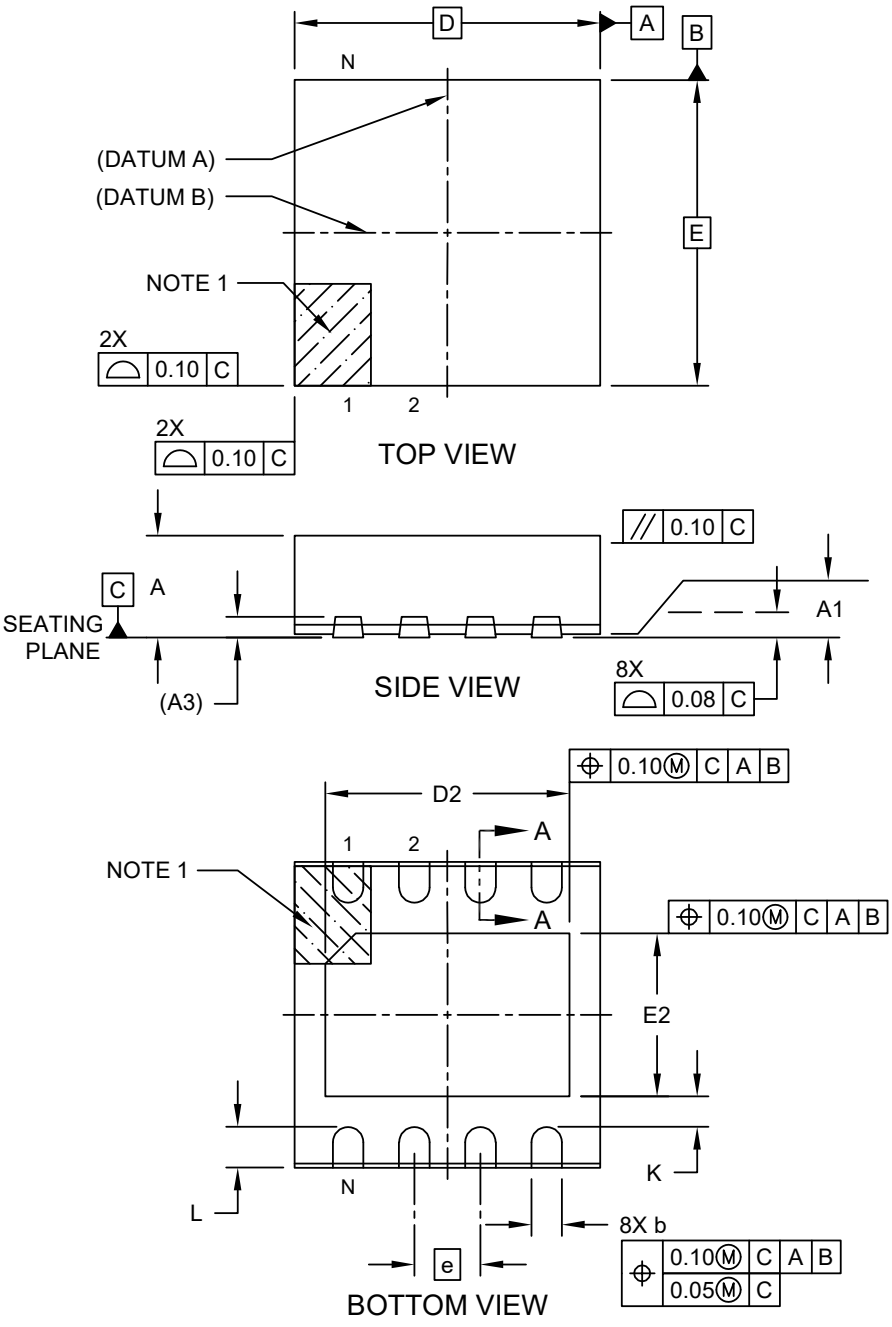


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

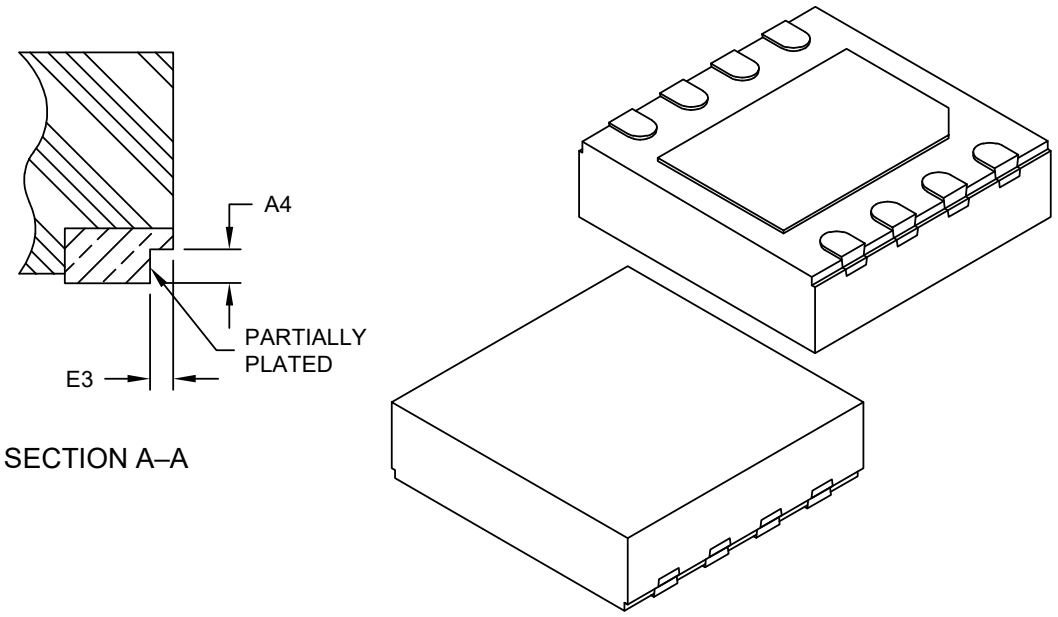
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21358 Rev D Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	-	0.19
Wettable Flank Step Cut Width	E3	-	-	0.085

Notes:

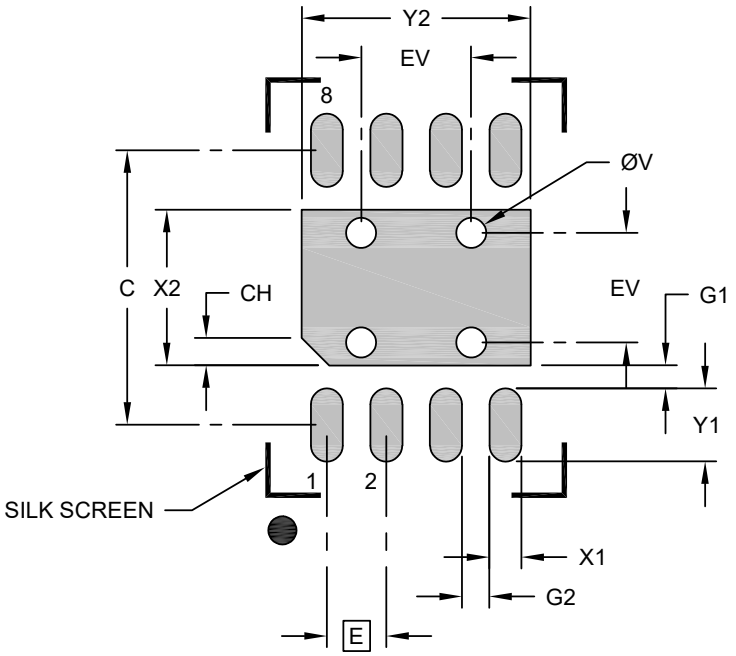
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev D Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev D

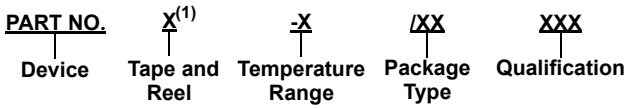
11. Revision History

Revision A (February 2025)

Initial release of this document

12. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device*:	MCP16364/5/6	48V Input, 1A Output, 2.2 MHz Switching Frequency, Integrated Switch Step-Down Regulator Device
Tape and Reel Option [1]:	(Blank)	= Standard Packing (Tube) — 120/Tube
	T	= Tape and Reel — 6000/Reel
Temperature:	E	= -40°C to +125°C (Extended)
Package Type:	Q8B	= 8-Lead 3 mm x 3 mm x 1 mm VDFN
Qualification:	(Blank)	= Standard Part
	VAO	= AEC-Q100 Automotive Qualified
	VXX	= AEC-Q100 Automotive Qualified, custom device, additional terms or conditions may apply
*Device Options:	MCP16364	= PFM/PWM, Fixed 2.2 MHz Switching Frequency
	MCP16365	= PWM Only, Fixed 2.2 MHz Switching Frequency
	MCP16366	= PWM Only, 2.2 MHz +10% Frequency Dithering

- MCP16364T-E/Q8B: PFM/PWM, Fixed 2.2 MHz Switching Frequency, Tape and Reel, Extended Temperature, 8-Lead VDFN Package
- MCP16365T-E/Q8B: PWM Only, Fixed 2.2 MHz Switching Frequency, Tape and Reel, Extended Temperature, 8-Lead VDFN Package
- MCP16366T-E/Q8B: PWM Only, 2.2 MHz +10% Frequency Dithering, Tape and Reel, Extended Temperature, 8-Lead VDFN Package
- MCP16364-E/Q8BVAO: 48V Input, 1 A Output, PFM/PWM, Fixed 2.2 MHz Switching Frequency, Tube, Extended Temperature Range, 8-Lead VDFN Package, AEC-Q100 Automotive Qualified
- MCP16365-E/Q8BVAO: 48V Input, 1 A Output, PWM Only, Fixed 2.2 MHz Switching Frequency, Tube, Extended Temperature Range, 8-Lead VDFN Package, AEC-Q100 Automotive Qualified
- MCP16366T-E/Q8BVAO: 48V Input, 1 A Output, PWM Only, 2.2 MHz +10% Frequency Dithering, Tape and Reel, Extended Temperature Range, 8-Lead VDFN Package, AEC-Q100 Automotive Qualified

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

13. Product Change Notification Service

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