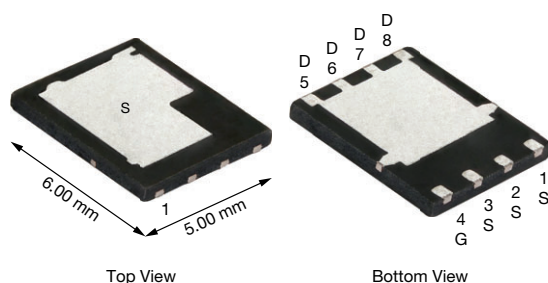


N-Channel 20 V (D-S) MOSFET

PowerPAK® SO-8DC


Top View

Bottom View

PRODUCT SUMMARY

V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00041
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0005
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.00120
Q_g typ. (nC)	95
I_D (A)	467 ^a
Configuration	Single

FEATURES

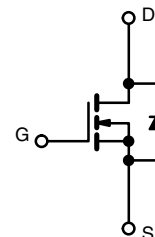
- TrenchFET® power MOSFET
- Top side cooling feature provides additional venue for thermal transfer
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing
- Power supplies
- Motor drive control
- Battery and load switch



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR178DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	-8 / +12	V
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	467
		$T_C = 70$ °C	373
		$T_A = 25$ °C	104 ^{b, c}
		$T_A = 70$ °C	8.3 ^{b, c}
Pulsed drain current ($V_{GS} = 10$ V, $t = 100$ μ s)	I_{DM}	500	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	113
		$T_A = 25$ °C	5.6 ^{b, c}
Single pulse avalanche current	I_{AS}	80	
Single pulse avalanche energy	E_{AS}	320	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	125
		$T_C = 70$ °C	80
		$T_A = 25$ °C	6.25 ^{b, c}
		$T_A = 70$ °C	4 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.8	1	
Maximum junction-to-case (source)	R_{thJC}	1.1	1.4	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	14	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-4.4	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6	-	1.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = -8 V / +12 V	-	-	± 150	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} =10 V	20	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A	-	0.00033	0.00041	Ω
		V _{GS} = 4.5 V, I _D = 30 A	-	0.00041	0.0005	
		V _{GS} = 2.5 V, I _D = 30 A	-	0.00090	0.0012	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 50 A	-	295	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	12 430	-	pF
Output capacitance	C _{oss}		-	4070	-	
Reverse transfer capacitance	C _{rss}		-	740	-	
Total gate charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 20 A	-	207	310	nC
Gate-source charge	Q _{gs}	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 20 A	-	95	143	
Gate-drain charge	Q _{gd}		-	26.6	-	
Output charge	Q _{oss}		-	18.219	-	
Gate resistance	R _g	V _{DS} = 10 V, V _{GS} = 0 V	-	62	-	Ω
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.2	0.94	1.9	
Rise time	t _r	V _{DD} = 10 V, R _L = 1 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	17	40	
Turn-off delay time	t _{d(off)}		-	10	20	
Fall time	t _f		-	83	170	
Turn-on delay time	t _{d(on)}		-	14	30	
Rise time	t _r	V _{DD} = 10 V, R _L = 1 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	44	90	
Turn-off delay time	t _{d(off)}		-	100	130	
Fall time	t _f		-	128	260	
			-	39	80	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	113	A
Pulse diode forward current	I _{SM}		-	-	500	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	-	60	90	ns
Body diode reverse recovery charge	Q _{rr}		-	90	110	nC
Reverse recovery fall time	t _a		-	27	-	ns
Reverse recovery rise time	t _b		-	19	-	

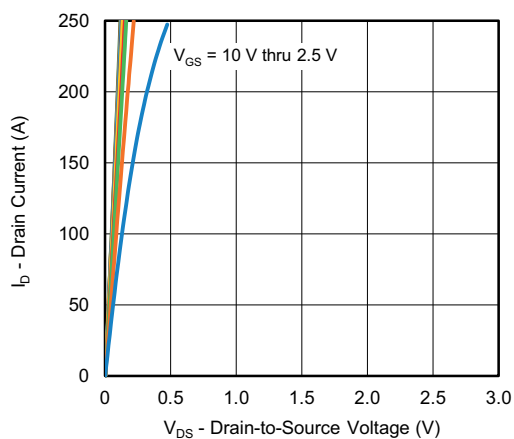
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

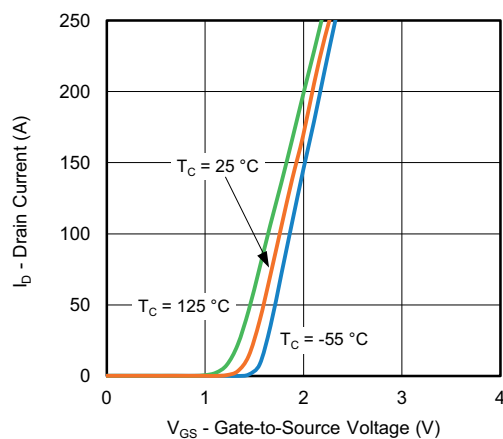
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



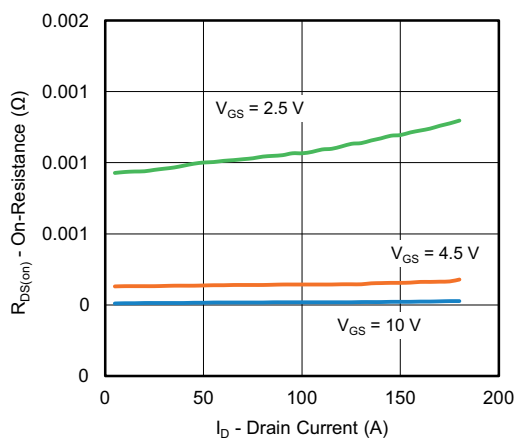
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



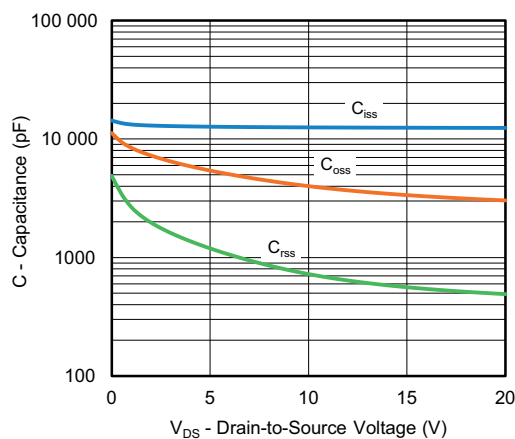
Output Characteristics



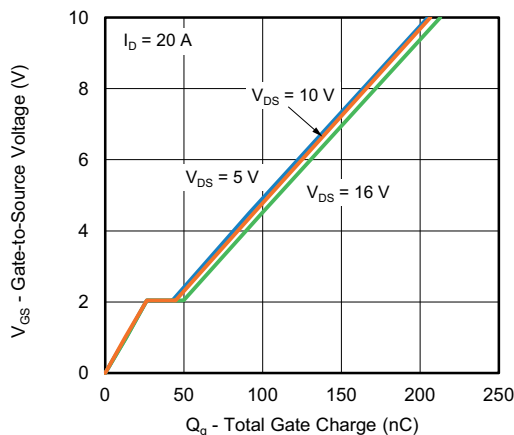
Transfer Characteristics



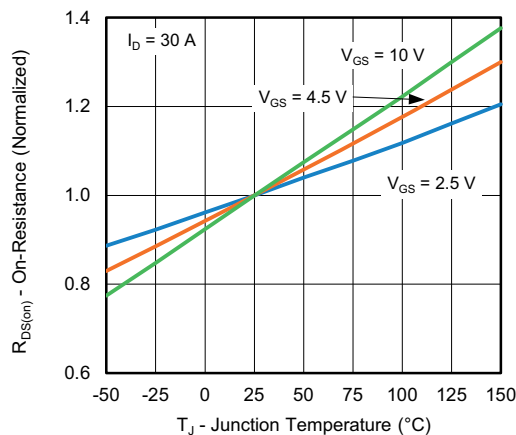
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



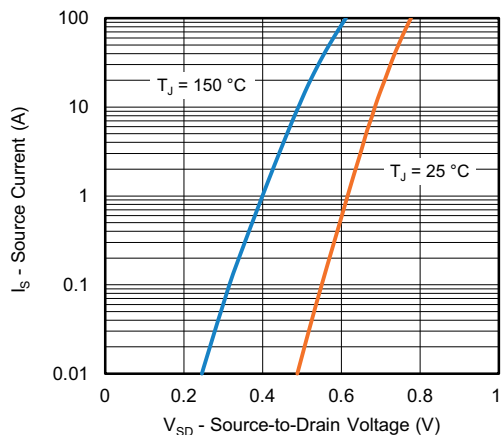
Gate Charge



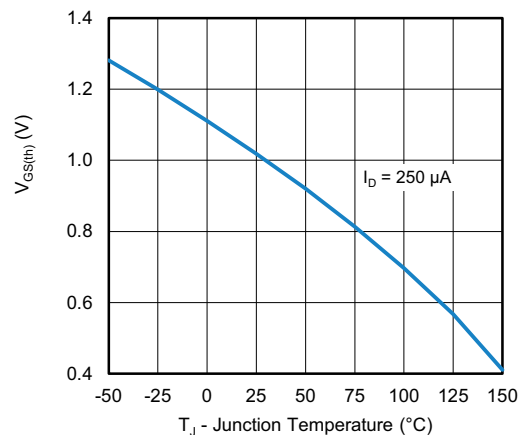
On-Resistance vs. Junction Temperature



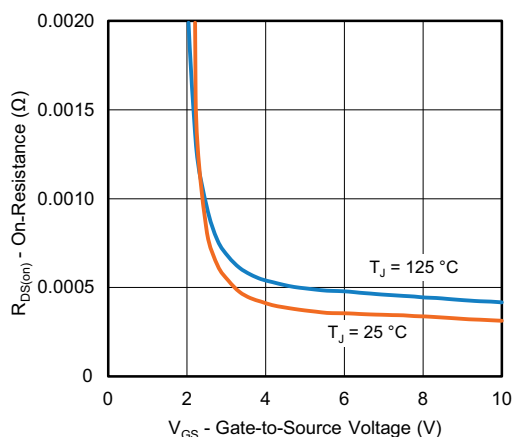
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



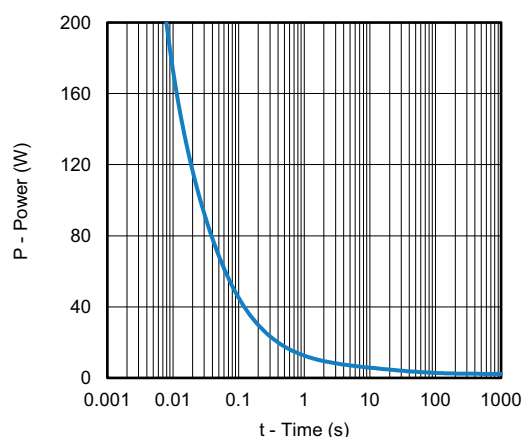
Source-Drain Diode Forward Voltage



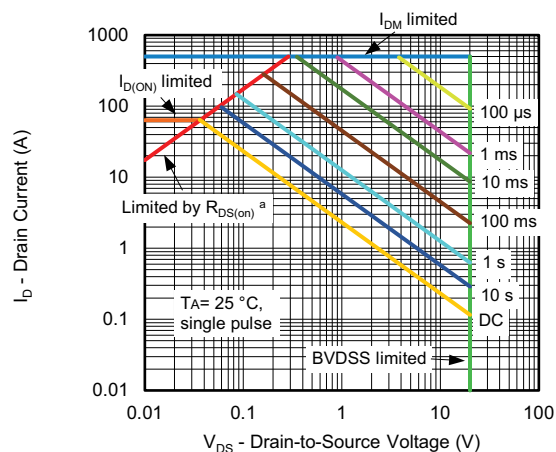
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



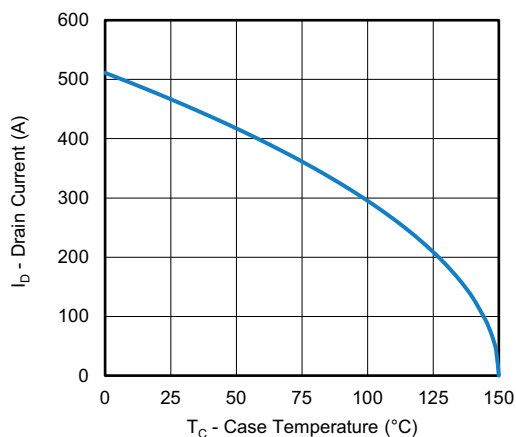
Safe Operating Area, Junction-to-Ambient

Note

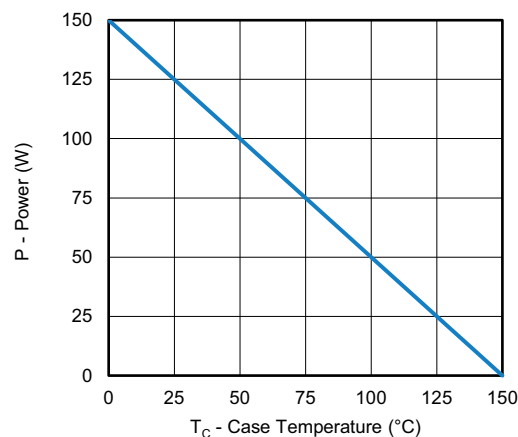
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



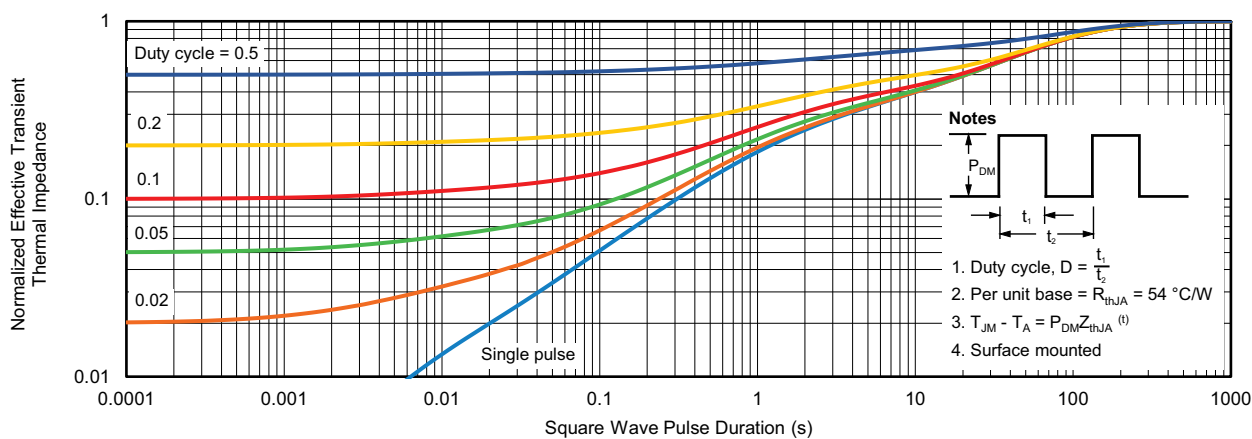
Current Derating ^a



Power, Junction-to-Case

Note

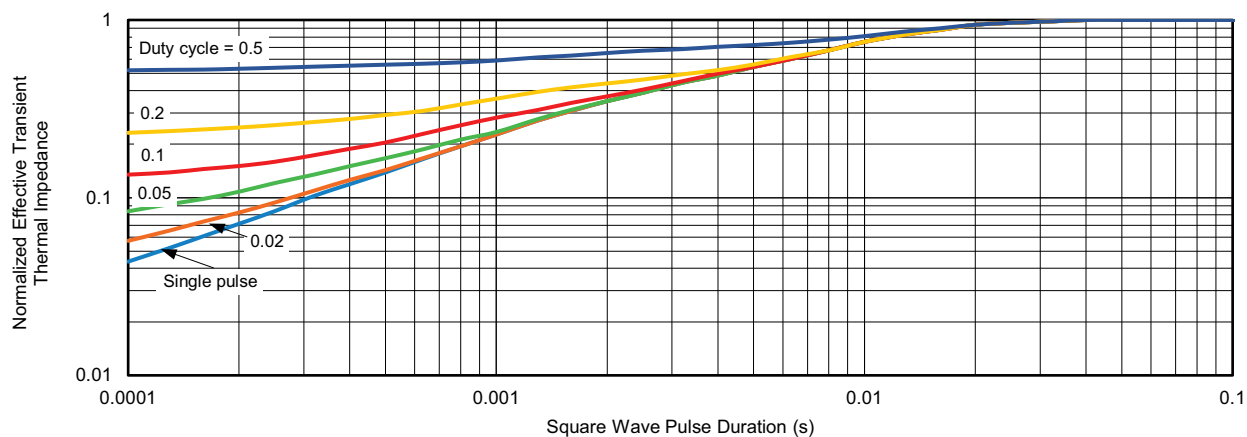
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



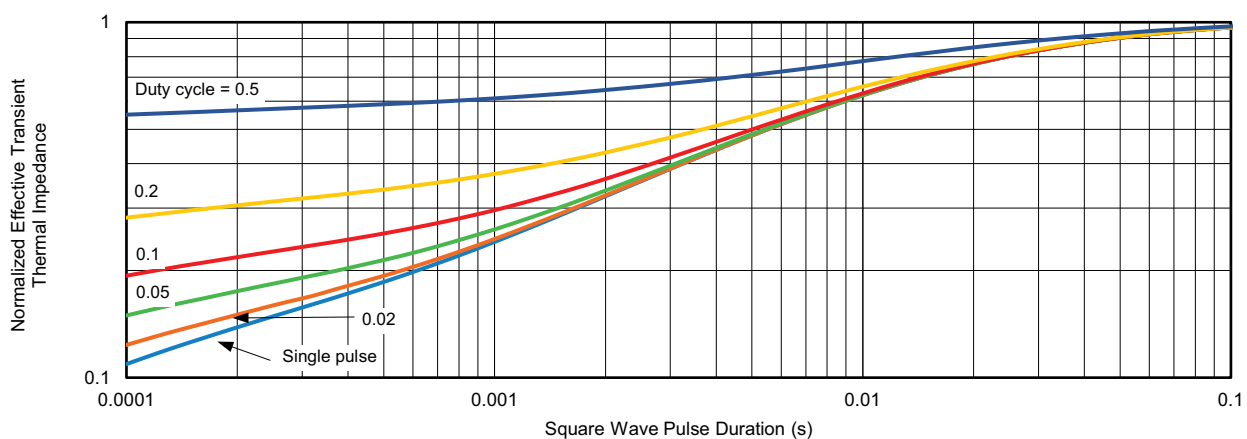
Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



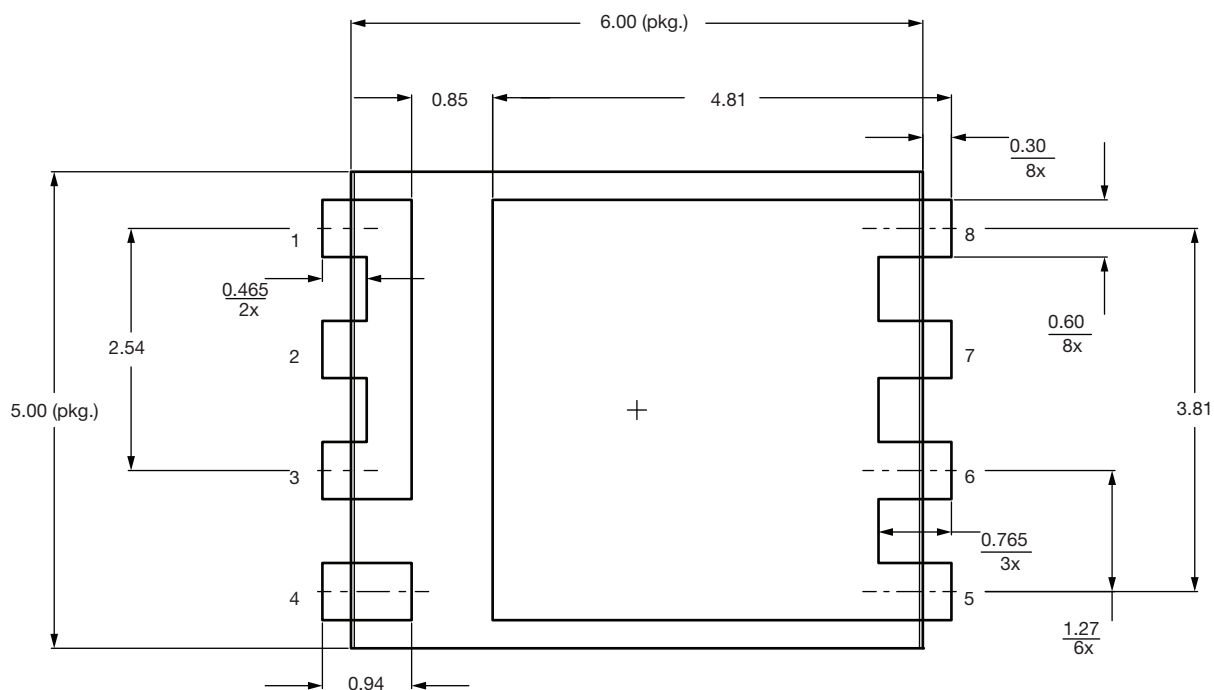
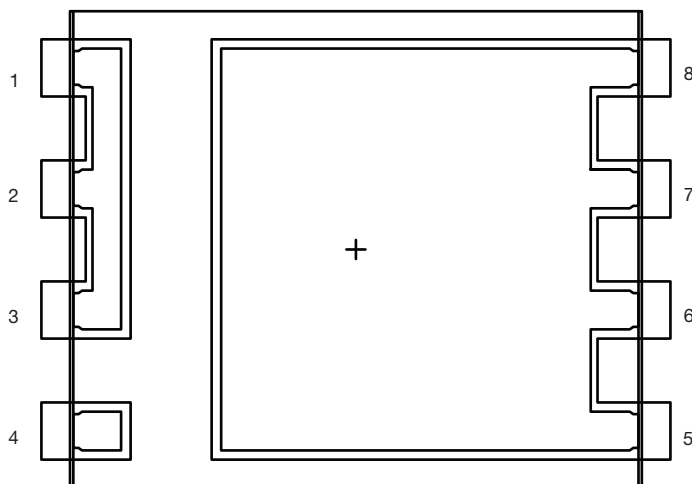
Normalized Thermal Transient Impedance, Junction-to-Case (Drain)



Normalized Thermal Transient Impedance, Junction-to-Case (Source)

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Recommended Land Pattern PowerPAK® SO-8SW (PKSO8SWSCL)



Note

- Dimensions in mm

ECN: C24-0483-Rev. A, 20-May-2024
DWG: 3027



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