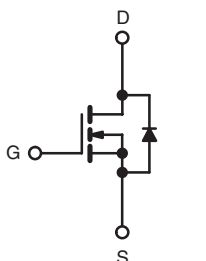
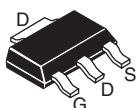


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.20
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	3.1	
Q_{gd} (nC)	5.8	
Configuration	Single	

SOT-223


N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION

Package	SOT-223	SOT-223
Lead (Pb)-free and Halogen-free	SiHFL014-GE3	SiHFL014TR-GE3 ^a
Lead (Pb)-free	IRFL014PbF	IRFL014TRPbF ^a
	SiHFL014-E3	SiHFL014T-E3 ^a
SnPb	IRFL014	IRFL014TR ^a
	SiHFL014	SiHFL014T ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	22	
Linear Derating Factor		0.025	W/ $^\circ\text{C}$
Linear Derating Factor (PCB Mount) ^e		0.017	
Single Pulse Avalanche Energy ^b	E_{AS}	100	mJ
Maximum Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25\text{ }^\circ\text{C}$	
Peak Diode Recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 16\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.7\text{ A}$ (see fig. 12).
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

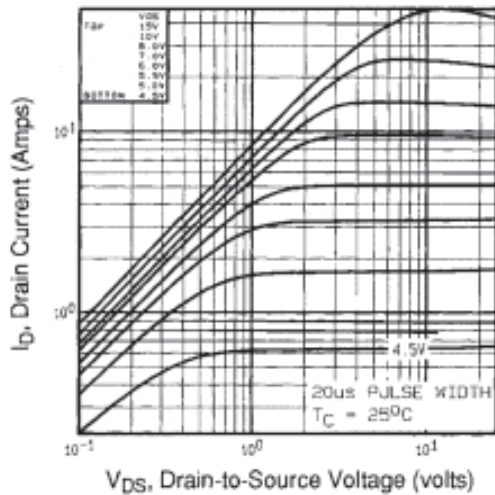
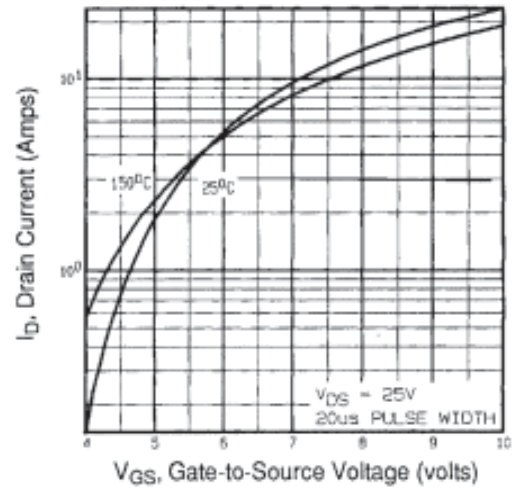
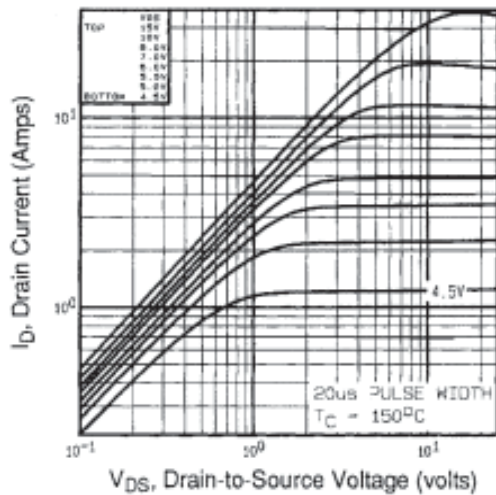
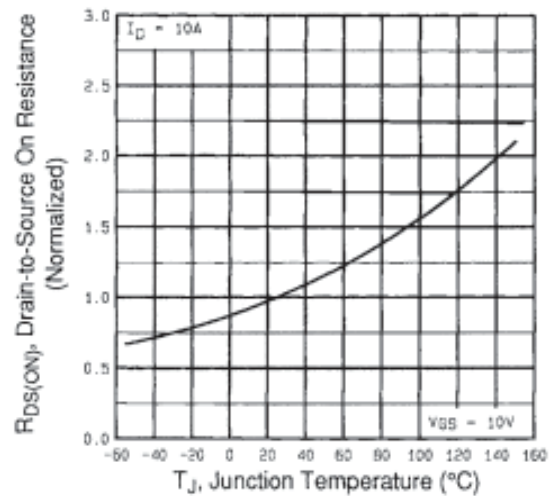
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.068	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.6 A ^b	-	-	0.20	Ω
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 1.6 A		1.9	-	-	S
Dynamic							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	300	-	pF
Output Capacitance	C _{OSS}			-	160	-	
Reverse Transfer Capacitance	C _{rss}			-	29	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 10 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	11	nC
Gate-Source Charge	Q _{gs}			-	-	3.1	
Gate-Drain Charge	Q _{gd}			-	-	5.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 10 A, R _g = 24 Ω, R _D = 2.7 Ω, see fig. 10 ^b		-	10	-	ns
Rise Time	t _r			-	50	-	
Turn-Off Delay Time	t _{d(off)}			-	13	-	
Fall Time	t _f			-	19	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.7	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	22	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 2.7 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 10 A, dI/dt = 100 A/μs ^b		-	70	140	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.20	0.40	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

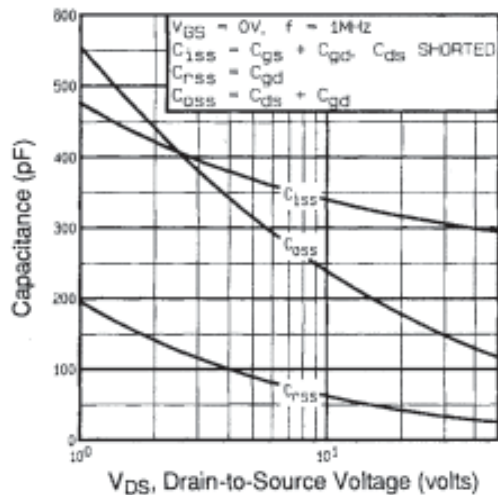


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

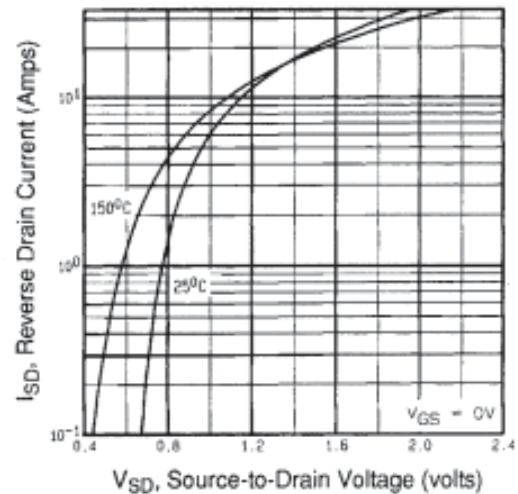


Fig. 7 - Typical Source-Drain Diode Forward Voltage

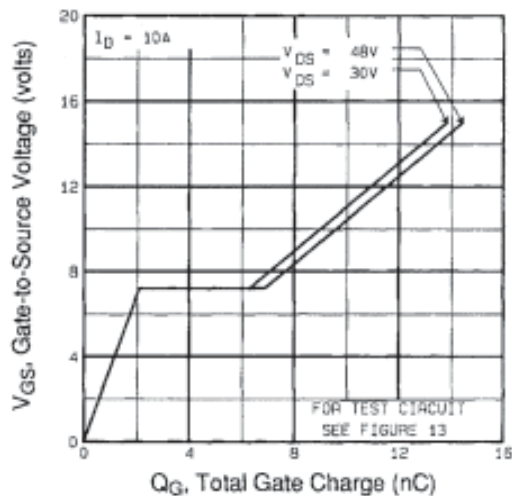


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

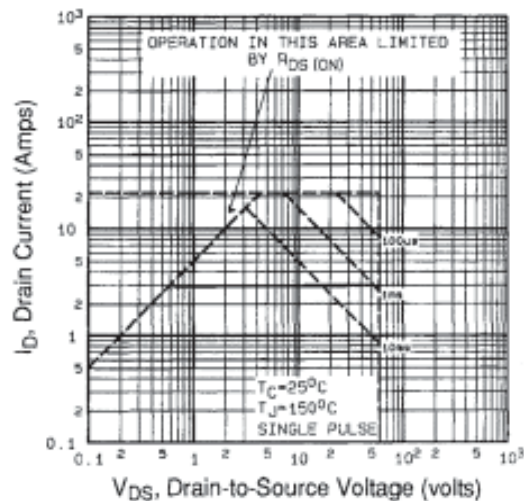


Fig. 8 - Maximum Safe Operating Area

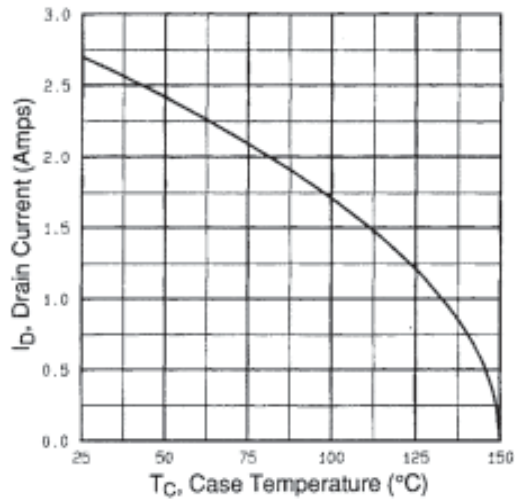


Fig. 9 - Maximum Drain Current vs. Case Temperature

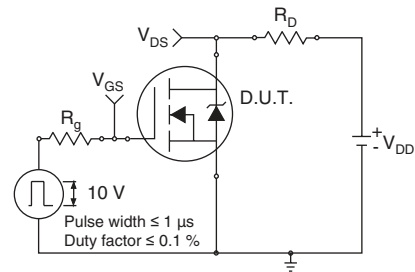


Fig. 10a - Switching Time Test Circuit

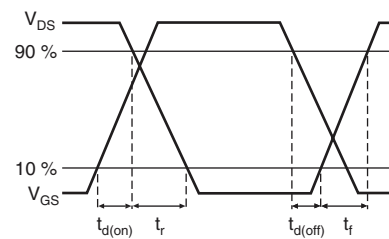


Fig. 10b - Switching Time Waveforms

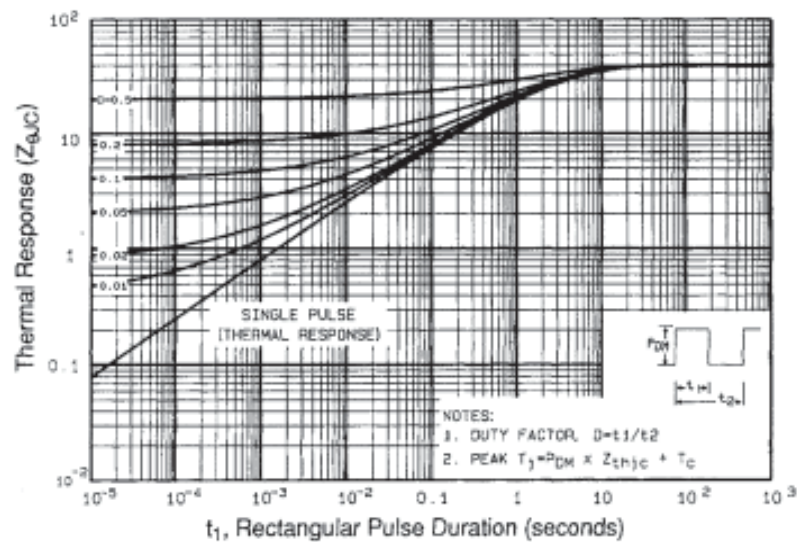


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

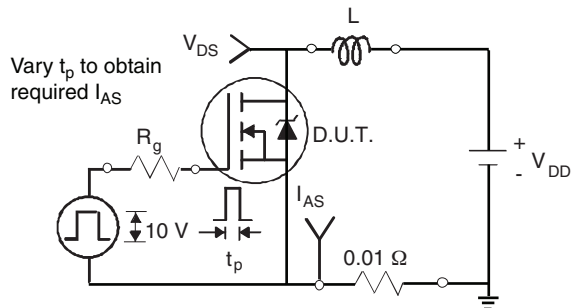


Fig. 12a - Unclamped Inductive Test Circuit

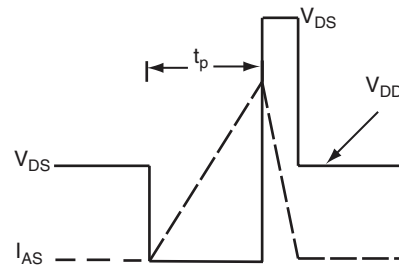


Fig. 12b - Unclamped Inductive Waveforms

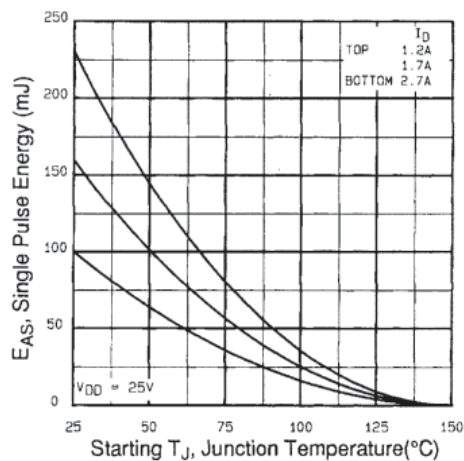


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

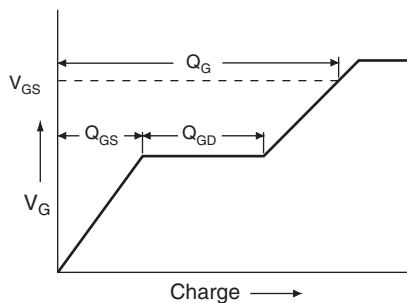


Fig. 13a - Basic Gate Charge Waveform

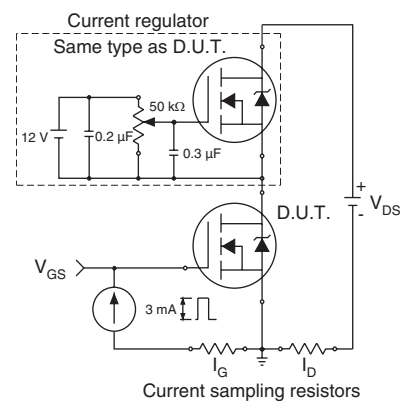
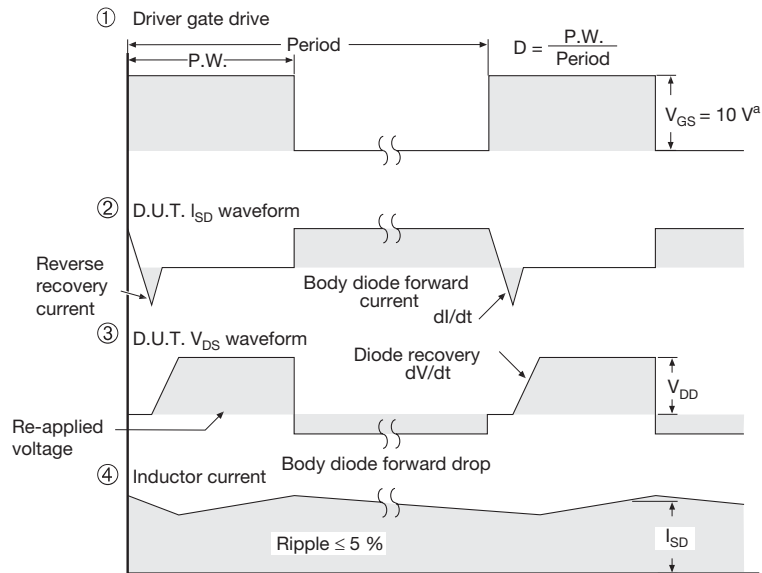
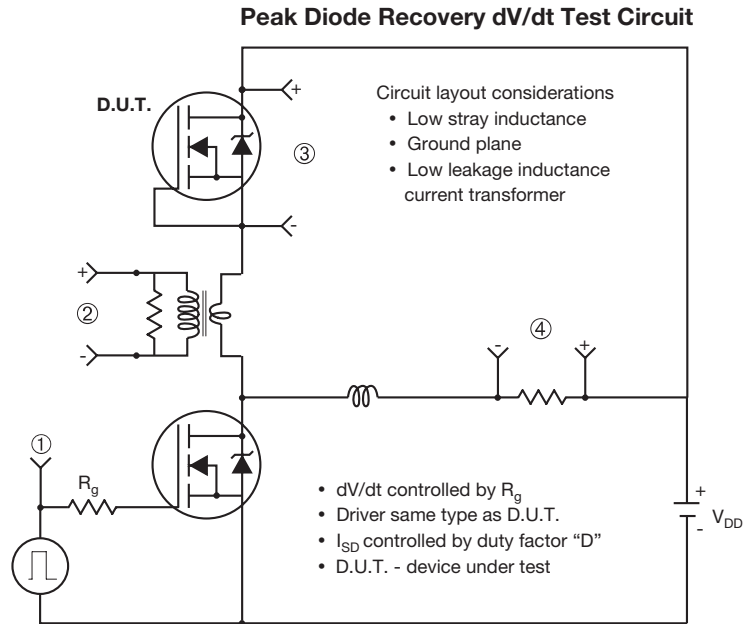


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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