Register DIMM

DDR5 5600

Datasheet

Products

TS4GAR80V6E3

Product Description

32GB DDR5 5600 REG-DIMM 2Rx8 2Gx8 CL46 1.1V

Datasheet version

1.0

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Revision History

Revision No.	History	Released Date	Editor by
1.0	First version	2024/11/22	PM

Transcend Features

Part Name	Capacity	Organization	Rank	Height	DIMM type	Note
TS4GAR80V6E3	32GB	2Gx8	2	31.25mm	RDIMM	

FEATURES

- Operating Temperature : 0°C to +95°C
- RoHS compliant products.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%))
- VPP = 1.8V(1.746V(-3%) ~ 1.908V(+6%))
- Clock Freq: 2800MHz for 5600Mb/s/Pin.
- Programmable CAS Latency: 22,26,28,30,32,36,40,42,46,50
- 16n bit pre-fetch
- Burst Length: 16 by default
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- Multi-purpose command (MPC)
- On-Die ECC
- SPD Hub with Thermal Sensor
- hPPR and sPPR are supported
- 30 u" PCB golden finger thickness
- Embedded Anti-sulfur resistor

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1. Introduction

1.1 General Feature Information

Hardware Feature

- Operating Temperature : 0°C to +95°C
- RoHS compliant products.
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- On-Die ECC
- SPD Hub with Thermal Sensor
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- 30 u" PCB golden finger thickness
- Embedded Anti-sulfur resistor

1.2 Product List

DIMM Type	Part Name	Capacity
Register Long-DIMM	TS4GAR80V6E3	32GB

1.3 Ordering Information

T	S	4	G	A	R	8	0	V	6	E	3
1		2		3		4		5	6	7	8

1 – Transcend
2 – DRAM module capacity = 4GB x 8
3 – Register DIMM
4 – Module memory bus width
5 – Operation voltage 1.1V
6 – 5600
7 – 2Gx8
8 – Micron

2. Product Specifications

2.1 Interface and Compliance

- DDR5 5600 Register Long DIMM with 80 Bits data width
- ECC Function
- RoHS Compliance
- CE, and UKCA Compliance

2.2 Supply Voltage

[Table 1] Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1)
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1)
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1)
Storage temperature	T_{STG}	-55~+100	°C	1), 2)

Note:

1. Stresses greater than those listed in this table may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device.For the measurement conditions, refer to JESD51-2 standard.

[Table 2] Recommended AC & DC Operating Conditions

Parameter	Symbol	Rating			Unit	Note
		Min	Typ.	Max		
Device Supply Voltage	VDD	1.067(-3%)	1.1	1.166(+6%)	V	1), 2), 3)
Supply Voltage for I/O	VDDQ	1.067(-3%)	1.1	1.166(+6%)	V	1), 2), 3)
Core Power Voltage	VPP	1.746(-3%)	1.8	1.908(+6%)	V	3)

Note:

1. VDD must be within 66mV of VDDQ.
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball

2.3 IDD Specification Parameters and Table

[Table 3] IDD Specification Parameters –32GB, 4G x 80 Module (2 Rank x 8)

Parameters	Symbol	IDD Max.	IDDQ Max.	IPP Max.	Unit
Operating One Bank Active-Precharge Current	/DD0	1020	1440	160	mA
Precharge Standby Current	/DD2N	980	1460	140	mA
Precharge Power-Down Current	/DD2P	940	1160	140	mA
Active Standby Current	/DD3N	1820	1400	160	mA
Active Power-Down Current	/DD3P	1800	1100	160	mA
Operating Burst Read Current	/DD4R	2670	2910	170	mA
Operating Burst Write Current	/DD4W	2900	3440	300	mA
Burst Refresh Current	/DD5B	4260	1490	400	mA
Self Refresh Current	/DD6N	3720	1000	400	mA
Operating Bank Interleave Read Current	/DD7	3730	2910	310	mA

Note:

1. IDD values are for full operating range of Voltage and Temperature
2. Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

2.4 Timing Parameters and Specifications

[Table 4] Timing Parameters and Specifications

Speed		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX		
Read command to first data	tAA	16	22.222	ns	
Activate to Read or Write command delay time	tRCD	16	-	ns	
Row Precharge Time	tRP	16	-	ns	
Activate to Precharge command period	tRAS	32	5x tREFI	ns	
Activate to Activate or Refresh command period	tRC	48	-	ns	
Clock Timing					
Average Clock Period	tCK(avg)	0.357	<0.384	ns	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(8nCK, 5ns)		nCK	
WRITE CAS_n to WRITE CAS_n com- mand delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)		ns	

WRITE CAS_n to WRITE CAS_n com- mand delay for same bank group, sec- ond write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)		nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)		nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)		nCK	
Four activate window for 2KB page size	tFAW_2K	Max(40nCK, 16.640ns)		ns	
Four activate window for 1KB page size	tFAW_1K	Max(32nCK, 13.312ns)		ns	
Delay from start of internal write trans- action to internal read command for dif- ferent bank group	tWTR_S	Max(4nCK, 2.5ns)		ns	
Delay from start of internal write trans- action to internal read command for same bank group	tWTR_L	Max(16nCK, 10ns)		ns	
Delay from start of internal write trans- action to internal read with auto pre- charge command for same bank	tWTRA	tWR-tRTP		ns	
Internal READ Command to PRE- CHARGE Command delay	tRTP	Max(12nCK, 7.5ns)		ns	
PRECHARGE (PRE) to PRECHARGE(PRE) delay	tPPD	2		nCK(avg)	
WRITE recovery time	tWR	30	-	ns	

2.5 Serial Presence Detect Specification

[Table 5] Serial Presence Detect Specification

TS4GAR80V6E3 Serial Presence Detect		
Byte No.	**Description**	**Hex Value**
0	Number of Bytes in SPD Device	30
1	SPD Revision	10
2	Host Bus Command Protocol Type	12
3	Module Type	01
4	First SDRAM Density and Package	04
5	First SDRAM Addressing	00
6	First SDRAM I/O Width	20
7	First SDRAM Bank Groups & Banks Per Bank Group	62
8	Second SDRAM Density and Package	00
9	Second SDRAM Addressing	00
10	Secondary SDRAM I/O Width	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	00
12	SDRAM BL32 & Post Package Repair	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	02
14	SDRAM Fault Handling and Temperature Sense	00
15	Reserved	00
16	SDRAM Nominal Voltage, VDD	00
17	SDRAM Nominal Voltage, VDDQ	00
18	SDRAM Nominal Voltage, VPP	00
19	SDRAM Timing	65
20	SDRAM Minimum Cycle Time(LSB)	A0
21	SDRAM Minimum Cycle Time(MSB)	01
22	SDRAM Maximum Cycle Time(LSB)	F2
23	SDRAM Maximum Cycle Time(MSB)	03
24	SDRAM CAS Latencies Supported	7A
25		AD
26		00
27		00
28		00
29	Reserved	00
30-31	SDRAM Minimum CAS Latency Time (tAAmin)	80
		3E
32-33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin)	80
		3E
34-35	SDRAM Minimum Row Precharge Delay Time (tRPmin)	80
		3E
36-37	SDRAM Minimum Active to Precharge Delay Time (tRASmin)	00

		7D
38-39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin)	80
		BB
40-41	SDRAM Minimum Write Recovery Time (tWRmin)	30
		75
42-43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min)	27
		01
44-45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min)	A0
		00
46-47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin)	82
		00
48-49	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFC1min)	00
		00
50-51	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFC2min)	00
		00
52-53	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFCsbmin)	00
		00
54	SDRAM Refresh Management, First Byte, First SDRAM 1	00
55	SDRAM Refresh Management, Second Byte, First SDRAM 1	00
56	SDRAM Refresh Management, First Byte, Second SDRAM 1	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM 1	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM 1	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM 1	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM 1	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM 1	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM 1	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM 1	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM 1	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM 1	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM 1	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM 1	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM 1	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM 1	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (tRRD_Lmin)	88
71		13
72		08
73	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group	88
74		13

75	(tCCD_Lmin)	08
76	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group (tCCD_L_WRmin)	20
77		4E
78		20
79	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group (tCCD_L_WR2min)	10
80		27
81		10
82	SDRAM Minimum Four Activate Window (tFAWmin)	A4
83		2C
84		20
85	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group (tCCD_L_WTRmin)	10
86		27
87		10
88	SDRAM Minimum Write to Read Command Delay Time, Different Bank Group(tCCD_S_WTRmin)	C4
89		09
90		04
91	SDRAM Minimum Read to Precharge Command Delay Time, (tRTPmin)	4C
92		1D
93		0C
94-127	Base Configuration Section	00
128-191	Reserved for future use	00
192	SPD Revision for SPD bytes 192~447	10
193	Hashing Sequence	00
194	SPD Manufacturer ID Code, First Byte	Variable
195	SPD Manufacturer ID Code, Second Byte	Variable
196	SPD Device Type	Variable
197	SPD Device Revision Number	Variable
198	PMIC 0 Manufacturer ID Code, First Byte	Variable
199	PMIC 0 Manufacturer ID Code, Second Byte	Variable
200	PMIC 0 Device Type	Variable
201	PMIC 0 Revision Number	Variable
202	PMIC 1 Manufacturer ID Code, First Byte	Variable
203	PMIC 1 Manufacturer ID Code, Second Byte	Variable
204	PMIC 1 Device Type	Variable
205	PMIC 1 Revision Number	Variable
206	PMIC 2 Manufacturer ID Code, First Byte	Variable
207	PMIC 2 Manufacturer ID Code, Second Byte	Variable
208	PMIC 2 Device Type	Variable
209	PMIC 2 Revision Number	Variable
210	Thermal Sensor Manufacturer ID Code, First Byte	Variable
211	Thermal Sensor Manufacturer ID Code, Second Byte	Variable
212	Thermal Sensor Device Type	Variable
213	Thermal Sensor Revision Number	Variable
214-229	Reserved	00
230	Module Nominal Height	11
231	Module Maximum Thickness	21
232	Reference Raw Card Used	04
233	DIMM Attributes	81

234	Module Organization	08
235	Memory Channel Bus Width	32
236-239	Reserved	00
240	Registering Clock Driver Manufacturer ID Code, First Byte	Variable
241	Registering Clock Driver Manufacturer ID Code, Second Byte	Variable
242	Register Device Type	Variable
243	Register Revision Number	Variable
244	Data Buffer Manufacturer ID Code, First Byte	00
245	Data Buffer Manufacturer ID Code, Second Byte	00
246	Data Buffer Device Type	00
247	Data Buffer Revision Number	00
248	RCD-RW08 Clock Driver Enable	2A
249	RCD-RW09 Output Address and Control Enable	0A
250	RCD-RW0A QCK Driver Characteristics	55
251	RCD-RW0B	00
252	RCD-RW0C QxCA and QxCS_n Driver Characteristics	11
253	RCD-RW0D Data Buffer Interface Driver Characteristics	00
254	RCD-RW0E QCK, QCA and QCS Output Slew Rate	00
255	RCD-RW0F BCK, BCOM, and BCS Output Slew Rate	00
256	DB-RW86 DQS RTT Park Termination	00
257-447	Reserved	00
448-509	Reserved for future use	00
510-511	CRC for bytes 0-509	Variable
512	Manufacturing Information	01
513		4F
514	Module Manufacturing Location	54
515	Module Manufacturing Date	Variable
516		Variable
517-520	Module Serial Number	Variable
521-550	Module Part Number	Note 1
551	Module Revision Code	00
552	DRAM Manufacturer ID Code	Variable
553		Variable
554	DRAM Stepping	Variable
555-639	Manufacturer's Specific Data	Variable
640-1023	End User Programmable	Variable

Note:

1. The detail Model Part Number is listed as below.

Byte	521	522	523	524	525	526	527	528	529	530	531	532	533	534
PN	T	S	4	G	A	R	8	0	V	6	E	3		
Hex	54	53	34	47	41	52	38	30	56	36	45	33	20	20

Byte	535	536	537	538	539	540	541	542	543	544	545	546	547	548
PN														
Hex	20	20	20	20	20	20	20	20	20	20	20	20	20	20

Byte	549	550
PN		
Hex	20	20

2.6 Hub Device Address

[Table 6] Hub Device Address

	Local Device Type ID (LID)					Host ID (HID)	HSA Pin connection
	PMIC	SPD Hub	RCD	TS0	TS1		
DIMM 0	1001	1010	1011	0010	0110	000	10.0 KΩ to GND
DIMM 1	1001	1010	1011	0010	0110	001	15.4 KΩ to GND
DIMM 2	1001	1010	1011	0010	0110	010	23.2 KΩ to GND
DIMM 3	1001	1010	1011	0010	0110	011	35.7 KΩ to GND
DIMM 4	1001	1010	1011	0010	0110	100	54.9 KΩ to GND
DIMM 5	1001	1010	1011	0010	0110	101	84.5 KΩ to GND
DIMM 6	1001	1010	1011	0010	0110	110	127 KΩ to GND
DIMM 7	1001	1010	1011	0010	0110	111	196 KΩ to GND

2.7 SPD HUB & PMIC Operating Conditions

[Table 7] SPD HUB operating conditions

Parameter	Symbol	Min	Typ	Max	Units
Input Supply Voltage	V_{DDSPD}	1.7	1.8	1.98	V
Input Supply Voltage	V_{DDIO}	0.95	1	1.05	V
Case operating temperature	T_{CASE}	-40		125	°C
Case temperature range for NVM Write operation Data writes outside this range may not meet retention requirements.	$T_{WRITEOK}$	-40		95	°C

[Table 8] PMIC operating conditions

Parameter	Symbol	Min	Typ	Max	Units	note
Bulk Input Supply Voltage	VIN_Bulk	4.25	12.0	15	V	
Host Supply Voltage	VIN_MGMT	3.0	3.3	3.6	V	

2.8 Environment Specifications

[Table 9] Operating Temperature condition

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	DRAM Operating Temperature	0 to 95	°C	1),2),3)
T_{STG}	Storage Temperature	-55 to 100	°C	4)

Note:

1. Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values. See JESD402-1 for details.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. Average Refresh Period 3.9us at lower than Tcase 85°C , 1.95us at 85°C < Tcase ≤ 95°C. For more details, please refer to JESD79-5.
4. Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

2.9 System Reliability

[Table 10] Telcordia SR332 issue 4 MTBF Specifications

Parameter	TS4GAR80V6E3
MTBF	> 2,000,000 hours

Note:

1. The calculation is based on 25°C.

[Table 11] Warranty

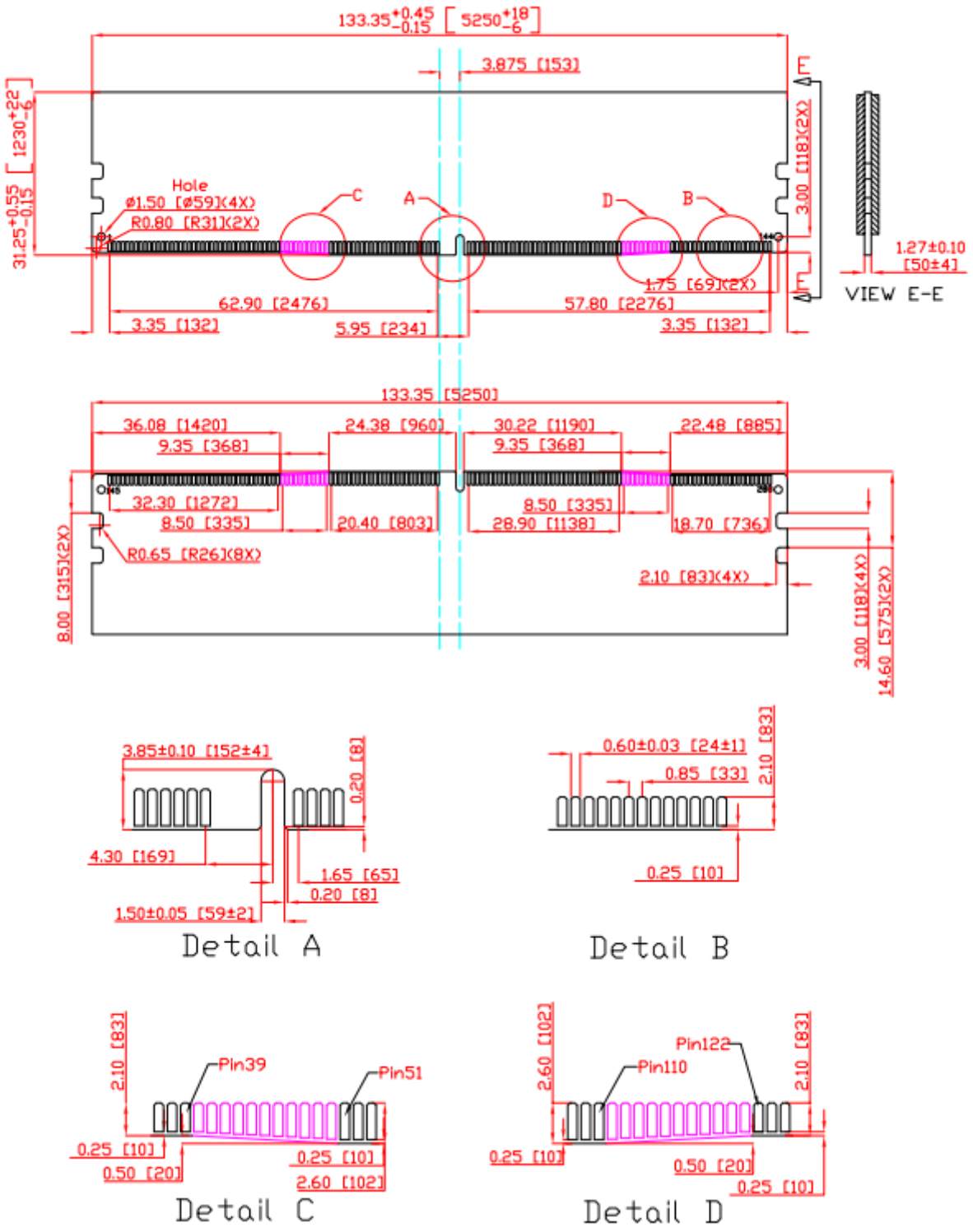
Parameter	TS4GAR80V6E3
Warranty	Limited Lifetime Warranty

3. Mechanical Specification

The figure below illustrates the Transcend DDR5 Register Long DIMM.

[Table 12] Physical Dimensions and Weight

Model	Thickness (mm)	Width (mm)		Length (mm)		Weight (gram)
TS4GAR80V6E3	Max 5.57	133.35	+0.45 -0.15	31.25	+0.55 -0.15	NA



Note : All dimensions are in millimeters[mils] and should be kept within a tolerance of ±0.15[6], unless otherwise specified.

4. Pin Assignments

4.1 Pin Assignments

[Table 13] Pin Assignments

Pin	Front Side	Pin	Back side	Pin	Front Side	Pin	Back side
1	VIN_BULK	145	VIN_BULK	74	PAR_A	218	CK_c
2	RFU	146	VIN_BULK	75	VSS	219	VSS
3	VIN_MGMT	147	PCAMP	Key			
4	HSCL	148	HSA				
5	HSDA	149	RFU	76	CA0_B	220	RFU
6	VSS	150	RFU	77	VSS	221	CA1_B
7	DQ0_A	151	VSS	78	CA2_B	222	VSS
8	VSS	152	DQ2_A	79	VSS	223	CA3_B
9	DQ1_A	153	VSS	80	CA4_B	224	VSS
10	VSS	154	DQ3_A	81	VSS	225	CA5_B
11	DQS0_A_t	155	VSS	82	CA6_B	226	VSS
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	83	VSS	227	PAR_B
13	VSS	157	DQS5_A_t, TDQS5_A_t	84	CS0_B_n	228	VSS
14	DQ4_A	158	VSS	85	VSS	229	CS1_B_n
15	VSS	159	DQ6_A	86	DLBDQ	230	VSS
16	DQ5_A	160	VSS	87	DLBDQS	231	RFU
17	VSS	161	DQ7_A	88	VSS	232	RFU
18	DQ8_A	162	VSS	89	CB4_B	233	VSS
19	VSS	163	DQ10_A	90	VSS	234	CB6_B
20	DQ9_A	164	VSS	91	CB5_B	235	VSS
21	VSS	165	DQ11_A	92	VSS	236	CB7_B
22	DQS1_A_t	166	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS
23	DQS1_A_c	167	DQS6_A_c, TDQS6_A_c	94	DQS9_B_c, TDQS9_B_c	238	DQS4_B_c
24	VSS	168	DQS6_A_t, TDQS6_A_t	95	VSS	239	DQS4_B_t
25	DQ12_A	169	VSS	96	CB0_B	240	VSS
26	VSS	170	DQ14_A	97	VSS	241	CB2_B
27	DQ13_A	171	VSS	98	CB1_B	242	VSS
28	VSS	172	DQ15_A	99	VSS	243	CB3_B
29	DQ16_A	173	VSS	100	DQ0_B	244	VSS
30	VSS	174	DQ18_A	101	VSS	245	DQ2_B
31	DQ17_A	175	VSS	102	DQ1_B	246	VSS
32	VSS	176	DQ19_A	103	VSS	247	DQ3_B
33	DQS2_A_t	177	VSS	104	DQS0_B_t	248	VSS
34	DQS2_A_c	178	DQS7_A_c, TDQS7_A_c	105	DQS0_B_c	249	DQS5_B_c, TDQS5_B_c
35	VSS	179	DQS7_A_t, TDQS7_A_t	106	VSS	250	DQS5_B_t, TDQS5_B_t

36	DQ20_A	180	VSS	107	DQ4_B	251	VSS
37	VSS	181	DQ22_A	108	VSS	252	DQ6_B
38	DQ21_A	182	VSS	109	DQ5_B	253	VSS
39	VSS	183	DQ23_A	110	VSS	254	DQ7_B
40	DQ24_A	184	VSS	111	DQ8_B	255	VSS
41	VSS	185	DQ26_A	112	VSS	256	DQ10_B
42	DQ25_A	186	VSS	113	DQ9_B	257	VSS
43	VSS	187	DQ27_A	114	VSS	258	DQ11_B
44	DQS3_A_t	188	VSS	115	DQS1_B_t	259	VSS
45	DQS3_A_c	189	DQS8_A_c, TDQS8_A_c	116	DQS1_B_c	260	DQS6_B_c, TDQS6_B_c
46	VSS	190	DQS8_A_t, TDQS8_A_t	117	VSS	261	DQS6_B_t, TDQS6_B_t
47	DQ28_A	191	VSS	118	DQ12_B	262	VSS
48	VSS	192	DQ30_A	119	VSS	263	DQ14_B
49	DQ29_A	193	VSS	120	DQ13_B	264	VSS
50	VSS	194	DQ31_A	121	VSS	265	DQ15_B
51	CB0_A	195	VSS	122	DQ16_B	266	VSS
52	VSS	196	CB2_A	123	VSS	267	DQ18_B
53	CB1_A	197	VSS	124	DQ17_B	268	VSS
54	VSS	198	CB3_A	125	VSS	269	DQ19_B
55	DQS4_A_t	199	VSS	126	DQS2_B_t	270	VSS
56	DQS4_A_c	200	DQS9_A_c, TDQS9_A_c	127	DQS2_B_c	271	DQS7_B_c, TDQS7_B_c
57	VSS	201	DQS9_A_t, TDQS9_A_t	128	VSS	272	DQS7_B_t, TDQS7_B_t
58	CB4_A	202	VSS	129	DQ20_B	273	VSS
59	VSS	203	CB6_A	130	VSS	274	DQ22_B
60	CB5_A	204	VSS	131	DQ21_B	275	VSS
61	VSS	205	CB7_A	132	VSS	276	DQ23_B
62	ALERT_n	206	VSS	133	DQ24_B	277	VSS
63	VSS	207	RESET_n	134	VSS	278	DQ26_B
64	CS0_A_n	208	VSS	135	DQ25_B	279	VSS
65	VSS	209	CS1_A_n	136	VSS	280	DQ27_B
66	CA0_A	210	VSS	137	DQS3_B_t	281	VSS
67	VSS	211	CA1_A	138	DQS3_B_c	282	DQS8_B_c, TDQS8_B_c
68	CA2_A	212	VSS	139	VSS	283	DQS8_B_t, TDQS8_B_t
69	VSS	213	CA3_A	140	DQ28_B	284	VSS
70	CA4_A	214	VSS	141	VSS	285	DQ30_B
71	VSS	215	CA5_A	142	DQ29_B	286	VSS
72	CA6_A	216	VSS	143	VSS	287	DQ31_B
73	VSS	217	CK_t	144	RFU	288	VSS

4.2 Pin Description

[Table 14] Pin Description

Pin Name	Description	Pin Name	Description
CA[6:0]_A **CA[6:0]_B**	Address and Command Bus	**DQ[31:0]_A** **DQ[31:0]_B**	DIMM memory Data bus channel A & B
CS[1:0]_A **CS[1:0]_B**	Chip Select	**CB[7:0]_A** **CB[7:0]_B**	DIMM ECC Checkbits (CB) channel A & B
PAR_A **PAR_B**	Parity input	**DQS[9:0]_A_t** **DQS[9:0]_B_t**	Data Strobes (positive line of differential pair)
CK_t	Clocks (positive)	**DQS[9:0]_A_c** **DQS[9:0]_B_c**	Data Strobes (negative line of differential pair)
CK_c	Clocks (negative)	**TDQS[9:5]_A_t** **TDQS[9:5]_B_t**	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error	**TDQS[9:5]_A_c** **TDQS[9:5]_B_c**	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	**VIN_BULK**	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	**VIN_MGMT**	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	**VSS**	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	**RFU**	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	**LBDQS**	Loopback Data strobe output
LBDQ	Loopback Data output:		
Note: TDQSx and DQSx_t share a pin.			

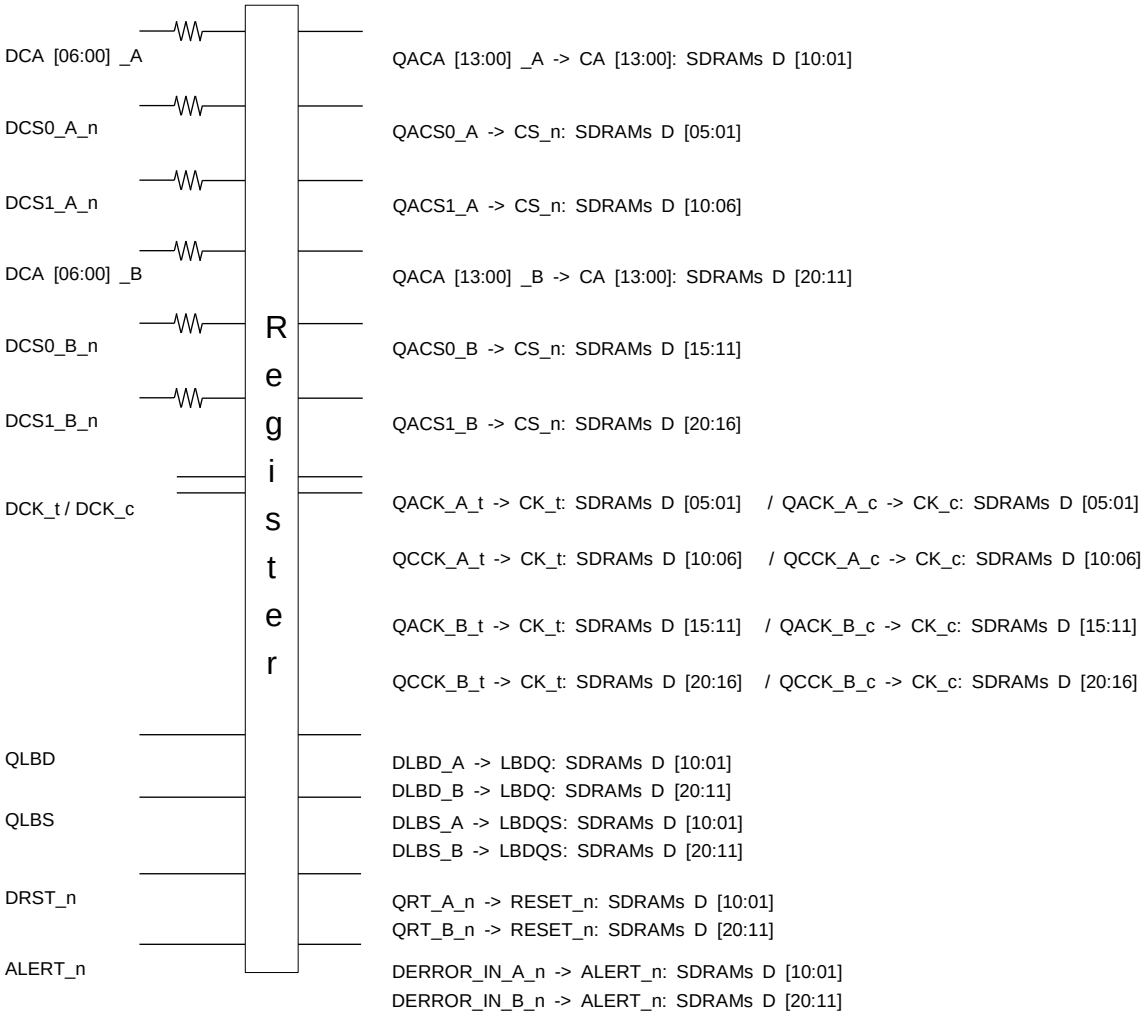
Symbol	Type	I/O Level	Function
CK_t, CK_c,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A **CA[6:0]_B**	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.
CS[1:0]_A **CS[1:0]_B**	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A **PAR_B**	Input	VDD	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
ALERT_n	Output	VDD	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Input Output	3.6V (max)	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).

Symbol	Type	I/O Level	Function
HSCL	Input	VOUT_1.0V	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.0V	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Input	2.1V max	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
DQ[31:0]_A **DQ[31:0]_B**	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A **CB[7:0]_B**	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating
DQS[9:0]_A_t **DQS[9:0]_B_t** **DQS[9:0]_A_c** **DQS[9:0]_B_c**	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
TDQS[9:5]_A_t **TDQS[9:5]_B_t** **TDQS[9:5]_A_c** **TDQS[9:5]_B_c**	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
DLBDQ	Output	VDDQ	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36: OP[2:0].
DLBDQS	Output	VDDQ	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].
RFU			Reserved for Future Use: No on DIMM electrical connection is present.
VIN_BULK	Supply		External power supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply		External power supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Supply		Ground

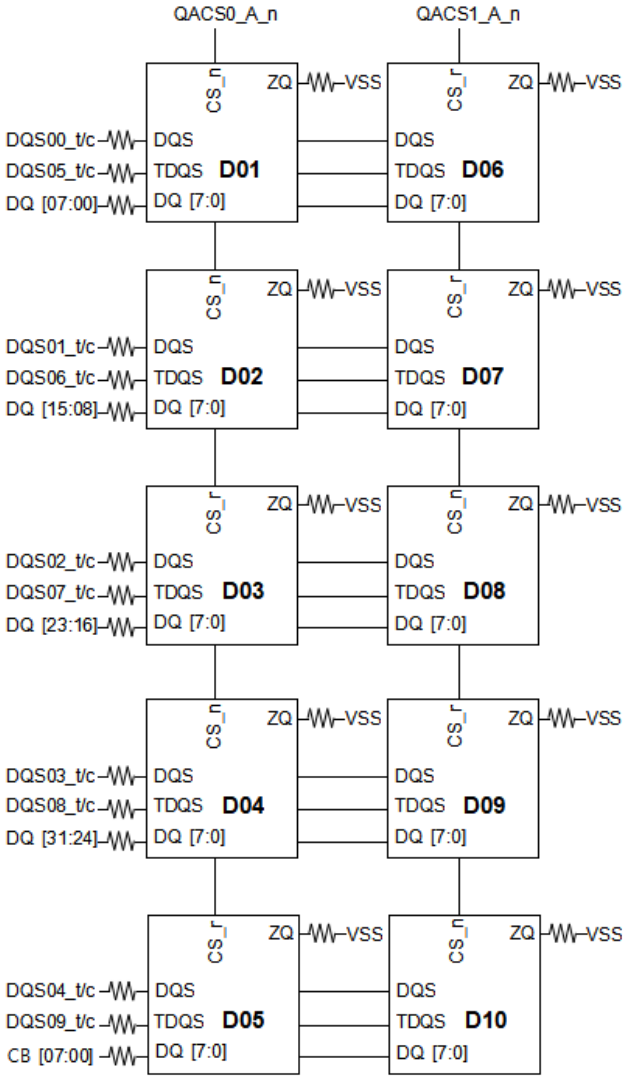
5. Block Diagram

5.1 Block Diagram

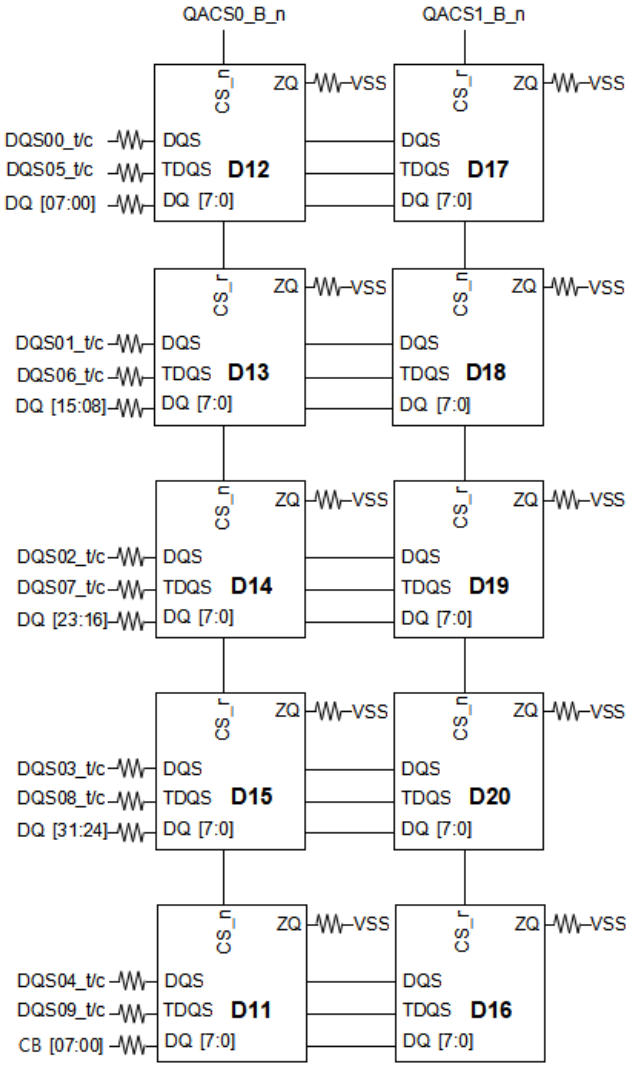
32GB, 4G x 80 Module (2 Rank x 8) TS4GAR80V6E3

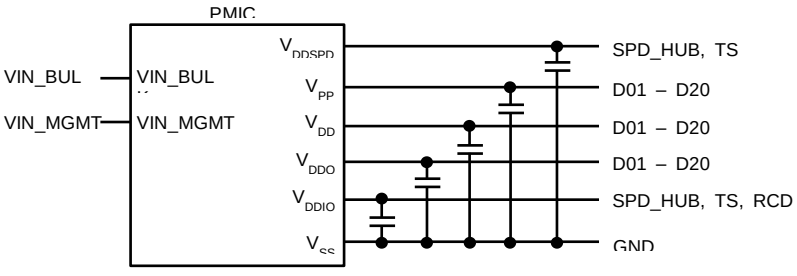


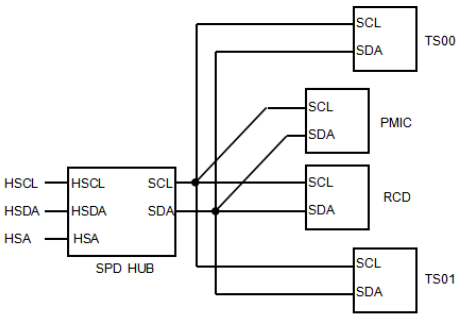
Channel A



Channel B







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