X67BCD321.L12(-1)

1 General information

EtherNet/IP is an Ethernet-based fieldbus. EtherNet/IP was developed by Allen-Bradley (Rockwell Automation) and later transferred to the Open DeviceNet Vendor Association (ODVA) as an open standard. In 1998, a working group at ControlNet International developed a procedure for setting the published Common Industrial Protocol to Ethernet. EtherNet/IP was published in March 2000 as an open industrial automation standard based on this procedure.

This bus controller makes it possible to connect X2X Link I/O nodes to EtherNet/IP. The bus controller can be operated via interface module X20IF10D1-1 or by 3rd-party systems with EtherNet/IP scanner functionality.

Additional X2X Link I/O nodes (X67 modules or other modules based on X2X Link) can be connected using the integrated X2X Link connection.

- Fieldbus: EtherNet/IP
- Integrated 3-port switch (1 internal port) for efficient cabling
- Auto-configuration of I/O modules
- Can be configured by the scanner using configuration assembly
- Web interface
- DHCP-capable
- 16 digital channels, configurable as inputs or outputs
- M12 connection type
- Integrated connection to local expansions via X2X Link for 252 additional modules
- Configurable I/O cycle (0.5 to 4 ms)
- Minimum fieldbus cycle time (also requested packet interval or RPI): 1 ms

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

Automation Studio V4.3 or later can be used to easily create configuration files (e.g. EDS files, binary files). All other function models are also supported by transferring configuration data to the bus controller (e.g. using the scanner via a "configuration assembly").

Automation Studio can be downloaded at no cost from the B&R website www.br-automation.com. The evaluation license is permitted to be used to create complete configurations for fieldbus bus controllers at no cost.

2 Order data

Model number	Short description	Figure
	Bus controller modules	
X67BCD321.L12	X67 bus controller, 1 EtherNet/IP interface, X2X Link power supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	
X67BCD321.L12-1	X67 bus controller, 1 EtherNet/IP interface, X2X Link supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, pinning variant, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	

Table 1: X67BCD321.L12, X67BCD321.L12-1 - Order data

Required accessories
See "Required cables and connectors" on page 8. For a general overview, see section "Accessories - General overview" of the X67 system user's manual.

3 Technical data

Model number	X67BCD321.L12	X67BCD321.L12-1
Short description		
Bus controller	EtherNet/IP Adapter (slave)	
General information		
Inputs/Outputs	16 digital channels, configurable as inputs or outputs using Automation Studio or data point, inputs with additional functions	
Isolation voltage between channel and bus	500 V_{Eff}	
Nominal voltage	24 VDC	
B&R ID code		
Bus controller	0xACF7	0xDABF
Internal I/O module	0xB1E7	0xDACE
Sensor/Actuator power supply	0.5 A summation current	
Status indicators	I/O function for each channel, supply voltage, bus function	
Diagnostics		
Outputs	Yes, using status LED and software	
I/O power supply	Yes, using status LED and software	
Connection type		
Fieldbus	M12 D-keyed	
X2X Link	M12, B-keyed	
Inputs/Outputs	8x M12, A-keyed	
I/O power supply	M8, 4-pin	
Power output	15 W X2X Link supply for I/O modules	
Power consumption		
Fieldbus	2.5 W	
Internal I/O	3.3 W	
X2X Link power supply	20.5 W at maximum power output for connected I/O modules	
Certifications		
CE	Yes	
KC	Yes	-
EAC	Yes	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - Max. 60°C TÜV 05 ATEX 7201X	
Interfaces		
Fieldbus	EtherNet/IP Adapter (slave)	
Variant	Internal 3x switch, male M12 circular connector, 2 female connectors on the module	
Line length	Max. 100 m between 2 stations (segment length)	
Transfer rate	10/100 Mbit/s	

Table 2: X67BCD321.L12, X67BCD321.L12-1 - Technical data

Model number	X67BCD321.L12	X67BCD321.L12-1
Transfer		
Physical layer	10BASE-T/100BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Min. cycle time [1]		
Fieldbus	1 ms	
X2X Link	500 µs	
Synchronization between bus systems possible	No	
I/O power supply		
Nominal voltage	24 VDC	
Voltage range	18 to 30 VDC	
Integrated protection	Reverse polarity protection	
Power consumption		
Sensor/Actuator power supply	Max. 12 W [2]	
Sensor/Actuator power supply		
Voltage	I/O power supply minus voltage drop for short circuit protection	
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC	
Summation current	Max. 0.5 A	
Short-circuit proof	Yes	
Digital inputs		
Input voltage	18 to 30 VDC	
Input current at 24 VDC	Typ. 4 mA	
Input characteristics per EN 61131-2	Type 1	
Input filter		
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 8)	
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Input circuit	Sink	
Additional functions	50 kHz event counting, gate measurement	
Input resistance	Typ. 6 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Event counter		
Quantity	2	
Signal form	Square wave pulse	
Evaluation	Each falling edge, cyclic counter	
Input frequency	Max. 50 kHz	
Counter 1	Input 1	
Counter 2	Input 3	
Counter frequency	Max. 50 kHz	
Counter size	16-bit	
Gate measurement		
Quantity	1	
Signal form	Square wave pulse	
Evaluation	Rising edge - Falling edge	
Counter frequency		
Internal	48 MHz, 3 MHz, 187.5 kHz	
Counter size	16-bit	
Length of pause between pulses	≥100 µs	
Pulse length	≥20 µs	
Supported inputs	Input 2 or input 4	
Digital outputs		
Variant	FET positive switching	
Switching voltage	I/O power supply minus residual voltage	
Nominal output current	0.5 A	
Total nominal current	8 A	
Output circuit	Source	
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output power supply	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)	
Residual voltage	<0.3 V at 0.5 A rated current	
Peak short-circuit current	<12 A	
Switching delay		
0 → 1	<400 µs	
1 → 0	<400 µs	
Switching frequency		
Resistive load	Max. 100 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	50 VDC	

Table 2: X67BCD321.L12, X67BCD321.L12-1 - Technical data

Model number	X67BCD321.L12	X67BCD321.L12-1
Electrical properties		
Electrical isolation	Channel isolated from bus EtherNet/IP not isolated from bus and channel not isolated from channel	
Operating conditions		
Mounting orientation		
Any	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP67	
Ambient conditions		
Temperature		
Operation	-25 to 60°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Mechanical properties		
Dimensions		
Width	53 mm	
Height	155 mm	
Depth	42 mm	
Weight	355 g	
Torque for connections		
M8	Max. 0.4 Nm	
M12	Max. 0.6 Nm	

Table 2: X67BCD321.L12, X67BCD321.L12-1 - Technical data

1) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

4 LED status indicators

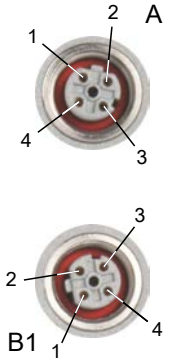
Figure	LED	Color	Status	Description
Status indicator 1: Left: Module status, Right: Network status  Status indicator 2: Left: Green, Right: Red	**Status indicator 1**: Status indicator for module and network function			
	Mod status[1]	Green	On	Indicates that there is at least one client connection
			Blinking	Bus controller not yet configured.
		Red	On	Major unrecoverable fault.
			Blinking	Minor recoverable fault
		Green/Red	Blinking	Initialization/Self-test
	Net status[2]	Green	On	Indicates at least one established active scanner connection
			Blinking	Indicates no established active scanner connection
			Off	Indicates no IP address has been assigned
		Red	On	Indicates an IP address has been used more than once
			Blinking	Indicates a timeout on at least one connection
		Green/Red	Blinking	Initialization/Self-test
	I/O LEDs			
	1-1 to 8-2	Orange	-	Input/Output status of the corresponding channel
	Status indicator 2: Status indicator for module functionality			
	Left	Green	Off	No power to module
			Single flash	Mode RESET
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	Right	Red	Off	No power to module or everything OK
			On	Error or reset state
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not in the valid range

1) LED "Mod status" is a green/red dual LED. The LED blinks red several times immediately after startup. However, this is a boot message, not an error (see EtherNet/IP user's manual).
2) LED "Net status" is a greed/red dual LED.

5 Operating and connection elements

6 Fieldbus interfaces

The module is connected to the network using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout		
	Pin	Name	
	1	TXD	Transmit data
	2	RXD	Receive data
	3	TXD\	Transmit data\
	4	RXD\	Receive data\
	Shield connection made via threaded insert in the module A → D-keyed (female), input B1 → D-keyed (female), output		

Information:

The color of the wires used in field-assembled cables for connecting to the fieldbus interface may deviate from the standard.

It is extremely important to make sure that the pinout is correct (see X67 section "Accessories - POWERLINK cables" in the X67 user's manual).

6.1 Cabling guidelines for bus controllers with Ethernet cables

Some X67 system bus controllers are based on Ethernet technology. POWERLINK cables supplied by B&R can be used for wiring.

Model number	Connection type
X67CA0E41.xxxx	Attachment cables - RJ45 to M12
X67CA0E61.xxxx	Connection cables - M12 to M12

The following cabling guidelines must be observed:

- Use Cat 5 SFTP cables.
- Observe the minimum cable bend radius (see data sheet for the cable).

Information:

Using POWERLINK cables supplied by B&R (X67CA0E61.xxxx and X67CA0E41.xxxx) satisfies product standard EN 61131-2.

The customer must implement additional measures in the event of further requirements.

6.2 EtherNet/IP address switch position

Switch position	Description
0x00	The IP address saved in flash memory is used. The adapter is started via DHCP if attribute 3 (configuration control) of the TCP/IP interface object was set to DHCP.
0x01 to 0x7F	The last position of the IP address saved in flash memory is changed to the address switch value. The IP address saved in flash memory is not changed. All other adapter parameters are read from flash memory and used without being changed.
0x80 to 0xEF	Sets the bus controller to DHCP mode for this range. The DNS server is informed of the current hostname. A hostname is generated according to how the network address switches are set. Example: The generated hostname is made up of three elements: "br" + "eip" + Address switch position (three decimal places) This means, for example, that the following hostname is generated for address switch position 0xD7 (dec. 215): "breip215".
0xF0 to 0xFD	Reserved (same function as position 0xFF).
0xFE	Initializes all bus controller parameters with default values during booting. No values are read from flash memory. The communication parameters correspond to the values assigned with switch setting 0xFF.
0xFF	Initializes all communication parameters with default values. All other bus controller parameters are read from flash memory. Default parameters: • IP address: 192.168.100.1 • Subnet mask: 255.255.255.0 • Gateway: 192,168,100,254 • Primary NetBIOS name: "br" + MAC address • Secondary NetBIOS name: "br" + "eip" + address switch number (decimal) • X2X Link configuration: 1 ms cycle time • X2X Link cable length: 0 m

6.2.1 Setting the IP address (default value)

Changes to the network address switch are only applied after a restart (power cycle). If the bus controller is restarted with the address switch value 0xFF, it is initialized with IP address 192.168.100.1. This address is also the factory default setting.
This IP address can be used to establish a connection to the bus controller. The internationally unique MAC address is listed on the housing side of the bus controller. The combination of "br" and the MAC address results in a unique name (primary NetBIOS name) that also makes it possible to access the bus controller.

Example of the primary NetBIOS name:

MAC address: 00-60-65-00-49-02
Resulting NetBIOS name: br006065004902

This means that, without additional parameter changes, either the default IP address 192.168.100.1 or the NetBIOS name "br+MAC" can be used to communicate with the controller.

Since NetBIOS is being used, the bus controller can only be accessed via this name if there are no intermediary routers or gateways in the way.

6.2.2 Automatic IP assignment by a DHCP server

If a address switch position between 0x80 and 0xEF is configured, the bus controller will attempt to request an IP address from the DHCP server. The assigned IP address can be queried with a "ping" command together with the hostname. The bus controller registers this hostname on the DHCP server, which should forward it to a DNS server.

Example: The hostname (DNS name) is made up of three elements:
"br" + "eip" + Address switch value (three decimal places).
This means, for example, that the following hostname is generated for address switch setting 0xD7 (dec. 215): "breip215".

If DNS service is not available on the network, the bus controller's two NetBIOS names can also be used for access. The secondary NetBIOS name is identical to the hostname; at address switch value 0x00, it is identical with the primary NetBIOS name. The bus controller can only be reached via its NetBIOS name if no other routers or gateways are in the way.

6.2.3 Changing the IP address with the network address switches

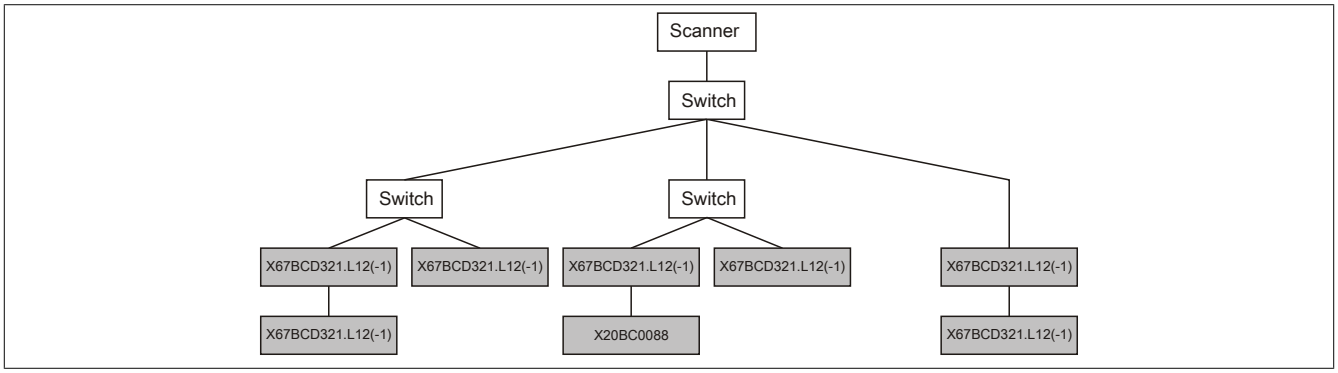
The address switches can be used to change the last byte in the IP address configured on the bus controller. The IP address saved in flash memory is not changed. If the address switches are set to 0x00, the bus controller applies the IP address last saved to flash memory. Switch positions between 0x01 and 0x7F cause the last position of the IP address (the lowest byte) to be overwritten by the value of the address switch. This provides the user a quick and easy way to address a large number of bus controllers. In short, an IP address between 192.168.100.1 and 192.168.100.127 can be selected for a bus controller using the address switches without requiring any additional software configuration.

6.2.4 Saving an IP address to flash memory

The IP parameters in the flash memory can be changed via the EtherNet/IP protocol or using the Telnet interface (see EtherNet/IP in the user's manual). If the IP address should be set via the TCP/IP object (class 0xF5), then the new address will only be saved to flash if instance attribute 3 (configuration control) of the TCP/IP object is set to 0 (see CIP specification).

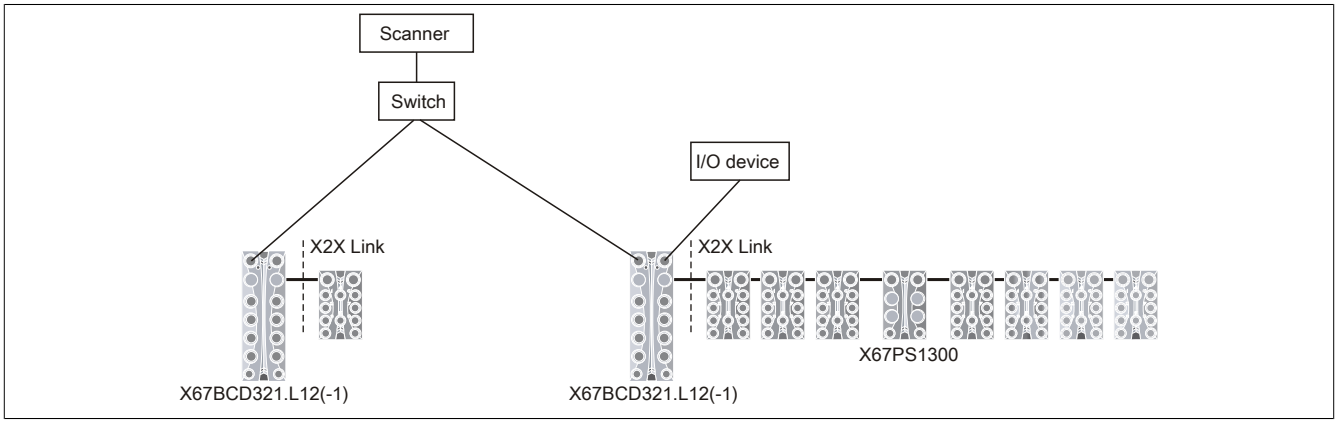
6.3 Integration into an EtherNet/IP network

This bus controller can be used in a tree or line topology as follows:



6.4 System configuration

A digital mixed module is already integrated in the bus controller. Up to 252 I/O modules can be connected to the bus controller.

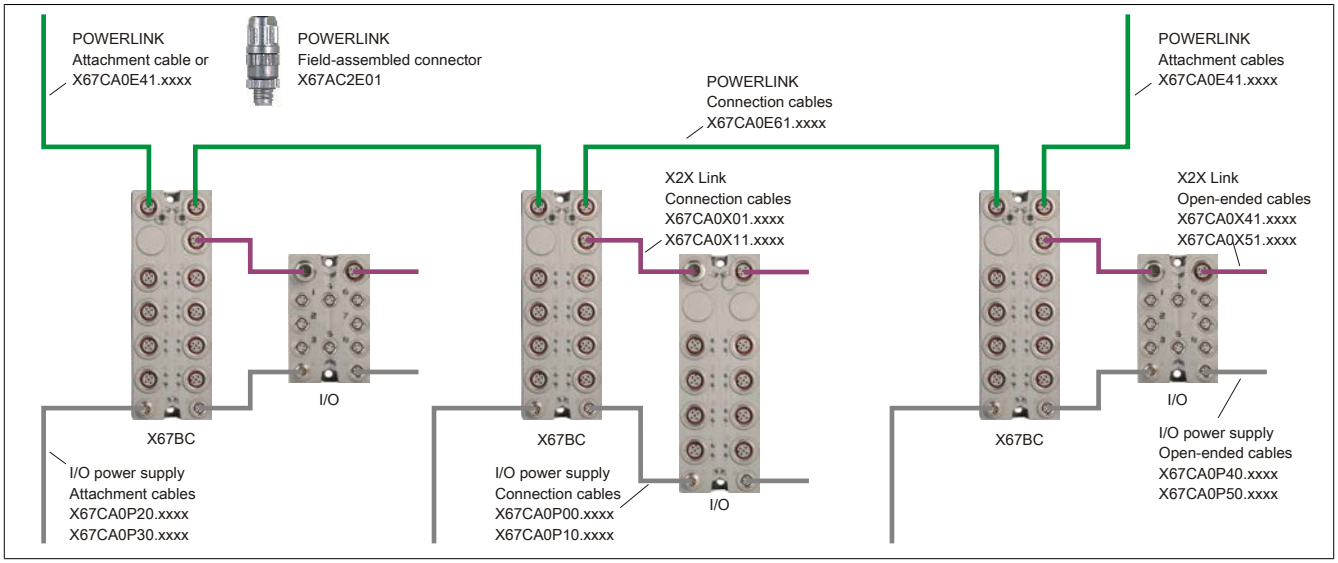


Information:

15 W are provided by the bus controller for additional X67 modules or other X2X Link-based modules.

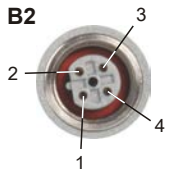
System supply module X67PS1300 is needed for additional power. This system supply module provides 15 W for additional modules. Each one should be mounted in the middle of the modules that are to be supplied with power.

6.5 Required cables and connectors



7 X2X Link

Additional modules can be connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using an M12 circular connector.

Connection	Pinout	
	Pin	**Name**
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield connection made via threaded insert in the module	
	B2 → B-keyed (female), output	

8 24 VDC I/O power supply

The I/O power supply is connected via M8 connectors C and D. The power supply is connected via connection C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

Information:

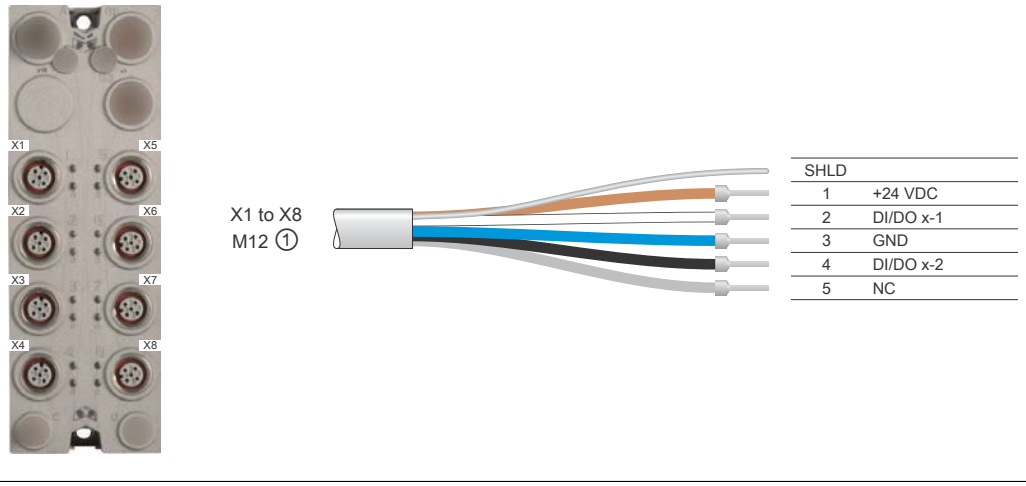
The maximum permissible current for the I/O power supply is 8 A (4 A per pin).

Connection	Pinout		
	Pin	**Connector C (male)**	**Connector D (female)**
	1	24 VDC fieldbus / X2X Link	24 VDC I/O
	2	24 VDC I/O	24 VDC I/O
	3	GND	GND
	4	GND	GND
	C → Connector (male) in module, feed for I/O power supply D → Connector (female) in module, routing of I/O power supply		

9 Integrated digital mixed module

1 additional mixed module can be saved by the digital mixed module integrated in the bus controller.

9.1 Pinout

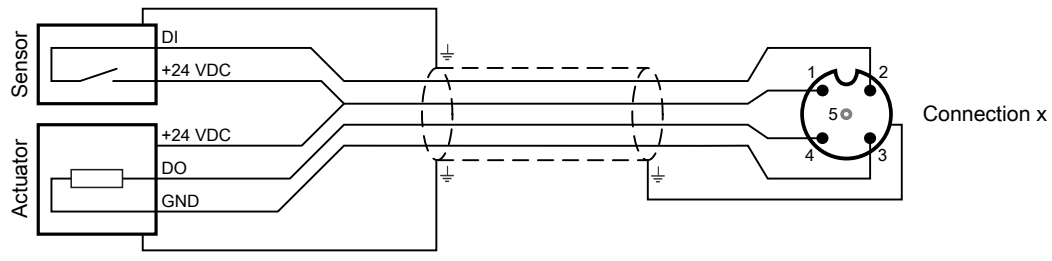


① X67CA0A41.xxxx: M12 sensor cable, straight
X67CA0A51.xxxx: M12 sensor cable, angled

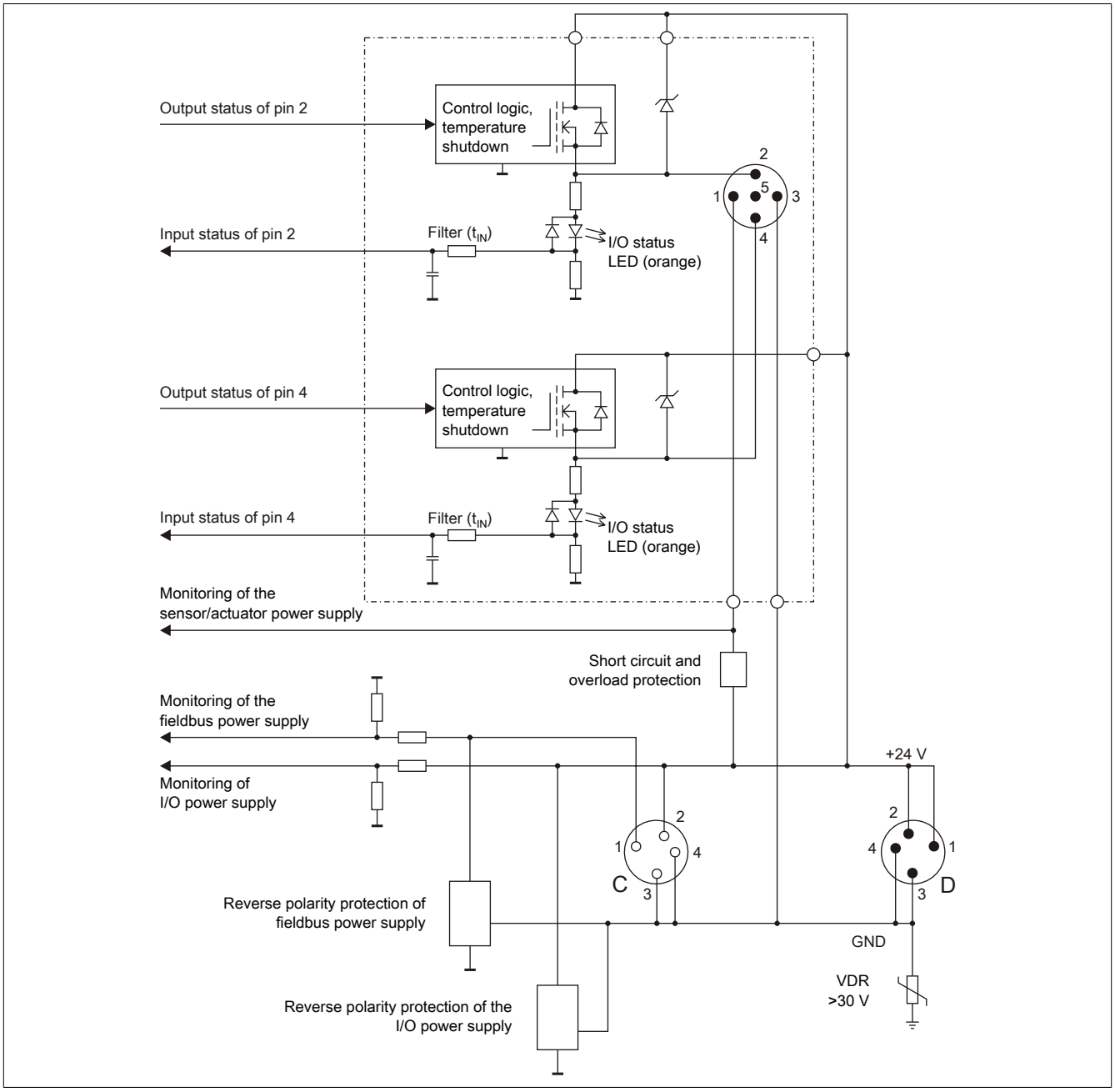
9.2 Connection X1 to X8

M12, 5-pin	Pinout		
Connection 1 to 4	Pin	Name	
		xxx.L12	xxx.L12-1
	1	24 VDC sensor/actuator power supply[1)]	
	2	Input/Output x-1	Input/Output x-2
	3	GND	
	4	Input/Output x-2	Input/Output x-1
	5	NC	
	Shield connection made via threaded insert in the module. 1) Sensors/Actuators are not permitted to be supplied externally. X1 to X8 → A-keyed (female), input/output		
Connection 5 to 8			

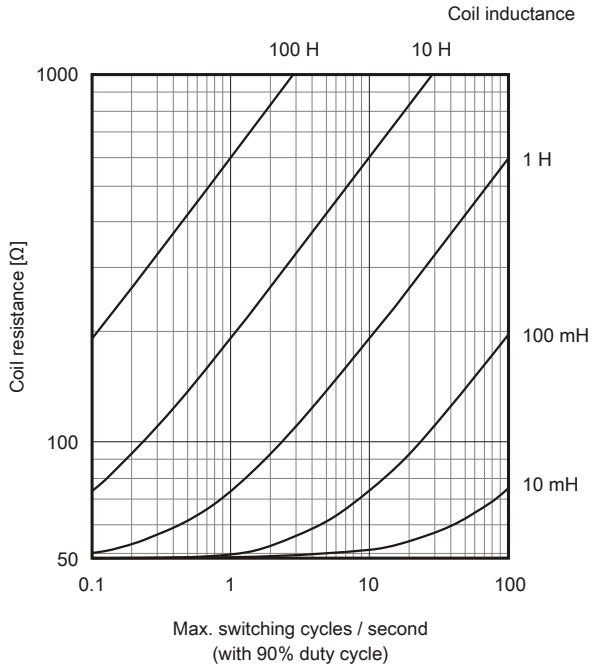
9.3 Connection example



9.4 Input/Output circuit diagram



9.5 Switching inductive loads



10 Register description

10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

These general data points are listed in section "Additional information - General data points" of the X67 system user's manual.

10.2 Function model 2 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

10.3 Function model 1 - Counter

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
20	ConfigOutput01 (counter channel 1)	USINT				•
22	ConfigOutput02 (counter channel 2)	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Reset counter 1	USINT			•	
	ResetCounter01	Bit 5				
22	Reset counter 2	USINT			•	
	ResetCounter02	Bit 5				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

10.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigIOMask01	USINT				•
17	-	ConfigIOMask02	USINT				•
20	-	ConfigOutput01 (counter channel 1)	USINT				•
22	-	ConfigOutput02 (counter channel 2)	USINT				•
18	-	ConfigOutput03 (input filter)	USINT				•
Communication							
0	0	Input state of digital inputs 1 to 16	UINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput16	Bit 15				
2	2	Switching state of digital outputs 1 to 16	UINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput16	Bit 15				
30	-	Status of digital outputs 1 to 16	UINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 15				
26	-	Input latch - Rising edges 1 to 8	USINT	•			
		InputLatch01	Bit 0				
		...	...				
		InputLatch08	Bit 7				
27	-	Input latch - Rising edges 9 to 16	USINT	•			
		InputLatch09	Bit 0				
		...	...				
		InputLatch16	Bit 7				
28	-	Acknowledgment - Input latch 1 to 8	USINT			•	
		QuitInputLatch01	Bit 0				
		...	...				
		QuitInputLatch08	Bit 7				
29	-	Acknowledgment - Input latch 9 to 16	USINT			•	
		QuitInputLatch09	Bit 0				
		...	...				
		QuitInputLatch16	Bit 7				
4	-	Counter01	UINT		•		
6	-	Counter02	UINT		•		
20	-	Reset counter 1	USINT			•	
		ResetCounter01	Bit 5				
22	-	Reset counter 2	USINT			•	
		ResetCounter02	Bit 5				
8192	-	asy_ModulID	UINT		•		
8196	-	asy_SupplyStatus	USINT		•		
8208	-	asy_SupplyInput	USINT		•		
8210	-	asy_SupplyOutput	USINT		•		

1) The offset specifies the position of the register within the CAN object.

10.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X67 user's manual (version 3.30 or later).

10.4.2 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN I/O.

10.5 Configuration

10.5.1 I/O mask 1 to 8

Name:
ConfigIOMask01

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

> **Information:**
>
> **In counter operation, channels 1 to 4 can only be configured as inputs.**

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 8 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

10.5.2 I/O mask 9 to 16

Name:
ConfigIOMask02

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

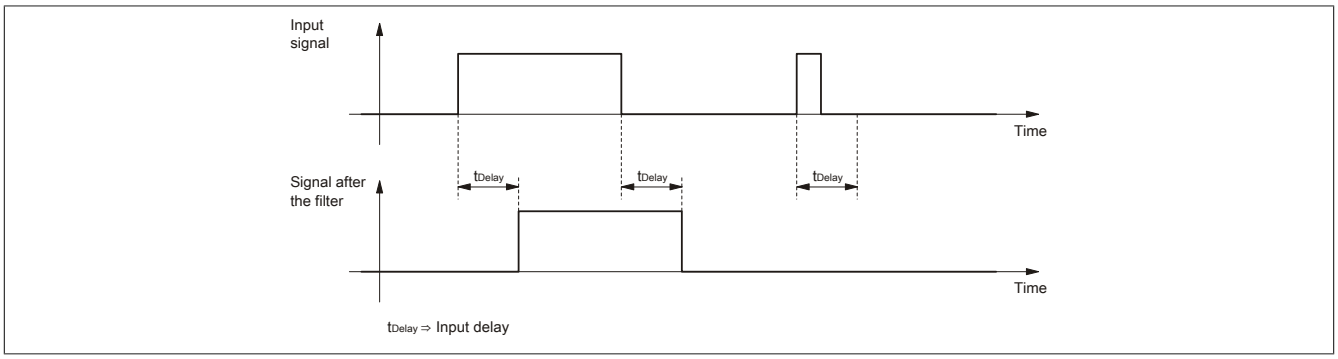
Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 9 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 16 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

10.5.3 Input filter

An input filter is available for each input. The input delay can be set using register "ConfigOutput03" on page 16. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



10.5.3.1 Digital input filter

Name:
ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

10.5.4 Configuration of Counter Channels 1 and 2

Name:
ConfigOutput01 to ConfigOutput02
ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Configuration of the counter frequency (only with gate measurement)	000	Counter frequency = 48 MHz (bus controller default setting)
		001	Counter frequency = 3 MHz
		010	Counter frequency = 187.5 kHz
		011 to 111	Reserved
3 - 4	Reserved	0	
5	ResetCounter0x	0	No affect on counter (bus controller default setting)
		1	Delete counter
6 - 7	Configuration of the operating mode	0	Event counter operation (Bus controller default setting)
		1	Gate measurement

Event counter operation

The falling edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

> **Information:**
>
> **Only one of the counter channels at a time can be used for gate measurement.**

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

10.6 Communication

10.6.1 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

10.6.1.1 Input state of digital inputs 1 to 16

Name:
DigitalInput01 to DigitalInput16

This register indicates the input state of digital inputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
15	DigitalInput16	0 or 1	Input state - Digital input 16

10.6.2 Digital outputs

The output status is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

10.6.2.1 Switching state of digital outputs 1 to 16

Name:
DigitalOutput01 to DigitalOutput16

This register is used to store the switching state of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
15	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

10.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

10.6.3.1 Status of digital outputs 1 to 16

Name:
StatusDigitalOutput01 to StatusDigitalOutput16

This register is used to indicate the status of digital outputs 1 to 16.

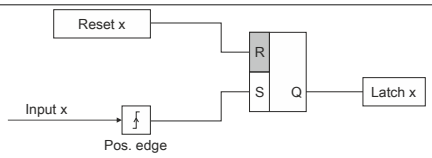
Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
15	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

10.6.4 Input latch

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	State
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

10.6.4.1 Input latch - Rising edges 1 to 8

Name:
InputLatch01 to InputLatch08

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatch0x" on page 19.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch01	0	Do not latch input 1
		1	Latch input 1
...		...	
7	InputLatch08	0	Do not latch input 8
		1	Latch input 8

10.6.4.2 Input latch - Rising edges 9 to 16

Name:
InputLatch09 to InputLatch16

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatchxx" on page 19.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch09	0	Do not latch input 9
		1	Latch input 9
...		...	
7	InputLatch16	0	Do not latch input 16
		1	Latch input 16

10.6.4.3 Acknowledgment - Input latch 1 to 8

Name:
QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch01	0	Do not reset input 1
		1	Reset input 1
...		...	
7	QuitInputLatch08	0	Do not reset input 8
		1	Reset input 8

10.6.4.4 Acknowledgment - Input latch 9 to 16

Name:
QuitInputLatch09 to QuitInputLatch16

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch09	0	Do not reset input 9
		1	Reset input 9
...		...	
7	QuitInputLatch16	0	Do not reset input 16
		1	Reset input 16

10.6.5 Event counter / Gate measurement

Name:
Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

Data type	Values
UINT	0 to 65535

10.6.6 Reading the module ID

Name:
asy_ModulID

This register offers the possibility to read the module ID.

Data type	Values
UINT	Module ID

10.6.7 Operating limit status registers

Name:
asy_SupplyStatus

This register can be used to read the status of the operating limits.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
1	Reserved	0	
2	Output supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
3 - 7	Reserved	0	

10.6.8 I/O supply voltage

Name:
asy_SupplyInput

This register contains the I/O supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

10.6.9 Output supply voltage

Name:
asy_SupplyOutput

This register contains the output supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs

10.8 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs