

CPU Unit Specifications

Item	CQM1-CPU11-E/21-E	CQM1-CPU41-E	CQM1-CPU42-E	CQM1-CPU43-E /44-E
Control method	Stored program method			
I/O control method	Cyclic scan with direct output; immediate interrupt processing			
Programming language	Ladder diagram			
Instruction length	1 step per instruction, 1 to 4 words per instruction			
Types of instructions	117 instructions (14 basic types)	137 instructions (14 basic types)		
Execution time	Basic instructions: 0.50 to 1.50 μ s Special instructions: 24 μ s (MOV instruction)			
Program capacity	3.2K words	7.2K words		
Input bits	00000 to 01115	I/O total within 128 points (8 words)	I/O total within 192 points (12 words)	
Output bits	10000 to 11115	Bits not used as I/O bits can be used as work bits.		
Work bits	2720 bits min. 01200 to 09515 11200 to 19515 21600 to 21915 22400 to 22915			
Function expansion bits	20000 to 21515: Used as work bits.			
	22000 to 22315: Used as work bits.		Analog SV area	Used as work bits.
	23200 to 23515: Used as work bits.			High-speed Counter 1,2 PV
	23600 to 23915: Used as work bits.			Pulse output 1, 2 volume (CPU43-E only)
	24000 to 24315: Used as work bits.			
MACRO instruction bits	Inputs: 64 bits (IR 09600 to IR 09915) Outputs: 64 bits (IR 19600 to IR 19915)			
High-speed Counter 0 PV	32 bits (IR 23000 to IR 23115)			
Special bits (SR area)	192 bits (IR 24400 to IR 25515)			
Temporary bits (TR area)	8 bits (TR0 to TR7)			
Holding bits (HR area)	1,600 bits (HR 0000 to HR 9915)			
Auxiliary bits (AR area)	448 bits (AR0000 to AR 2715)			
Link bits (LR area)	1,024 bits (LR 0000 to LR6315)			
Timers/counters	512 timers/counters (TIM/CNT 000 to TIM/CNT 511). Interrupt refreshing possible for TIM 000 to TIM 015 (high-speed timer only). Interval timers 0 to 2 (interval timer 2 is used with the high-speed counter 0). High-speed counter input.			In addition to the specifications on the left, high-speed counter 1, 2 inputs (2 pts.)
Data memory	1,024 words (DM 0000 to DM 1023) plus DM 6144 to DM 6655 (read-only)	6,144 words (DM 0000 to DM 6143) plus DM 6144 to DM 6655 (read-only)		
Interrupt processing	External interrupts: 4 Scheduled interrupts: 3 (one of which can be used as a high-speed counter interrupt and one of which can be used as pulse output)			In addition to the specifications on the left, high-speed counter 1, 2 interrupts (2 pts.)

Item	CQM1-CPU11-E/21-E	CQM1-CPU41-E	CQM1-CPU42-E	CQM1-CPU43-E /44-E
Memory protection	HR, AR, and DM area contents; counter values; and clock (RTC) values maintained during power interruptions.			
Memory backup	Battery life is 5 years regardless of presence or absence of clock (RTC).Backup time varies with ambient temperature.If BAT ERR indicator lights, replace the battery with a new one within 1 week.Connect new battery within 5 min of removing battery.			
Self-diagnostic functions	CPU Unit failure (watchdog timer), I/O bus error, memory failure, battery error, and host link error			
Program checks	No END instruction, programming errors (continuously checked during operation)			