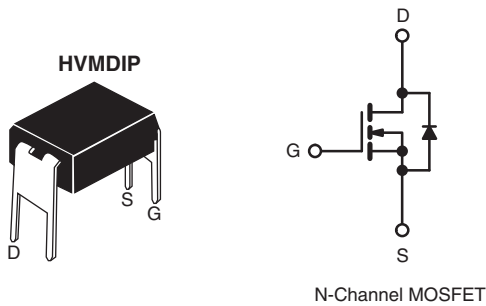


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V   0.10
$Q_g$ (Max.) (nC)	18
$Q_{gs}$ (nC)	4.5
$Q_{gd}$ (nC)	12
Configuration	Single



### FEATURES

- Dynamic dV/dt Rating
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4$  V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertible case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain servers as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRLD024PbF
	SiHLD024-E3
SnPb	IRLD024
	SiHLD024

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 10$		
Continuous Drain Current	$V_{GS}$ at 5.0 V	$T_A = 25$ °C	2.5	A
		$T_A = 100$ °C	1.8	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	20	
Linear Derating Factor			0.0083	W/°C
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	91	mJ
Maximum Power Dissipation	$T_A = 25$ °C	$P_D$	1.3	W
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 16$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.5$  A (see fig. 12).
- $I_{SD} \leq 17$  A,  $di/dt \leq 140$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W		
SPECIFICATIONS ( $T_J = 25\text{ °C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ °C}, I_D = 1\text{ mA}$	-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}, I_D = 1.5\text{ A}^b$	-	-	0.10	$\Omega$
		$V_{GS} = 4.0\text{ V}, I_D = 1.3\text{ A}^b$	-	-	0.14	
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 1.5\text{ A}^b$	3.7	-	-	S
Dynamic						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$ , see fig. 5	-	870	-	pF
Output Capacitance	$C_{oss}$		-	360	-	
Reverse Transfer Capacitance	$C_{rss}$		-	53	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$ $I_D = 17\text{ A}, V_{DS} = 48\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	18	nC
Gate-Source Charge	$Q_{gs}$		-	-	4.5	
Gate-Drain Charge	$Q_{gd}$		-	-	12	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 17\text{ A}$ $R_g = 9.0\text{ }\Omega, R_D = 1.7\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	11	-	ns
Rise Time	$t_r$		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Fall Time	$t_f$		-	41	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.0	-	nH
Internal Source Inductance	$L_S$		-	6.0	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode	-	-	2.5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	20	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 2.5\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	110	260	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.49	1.5	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

## Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

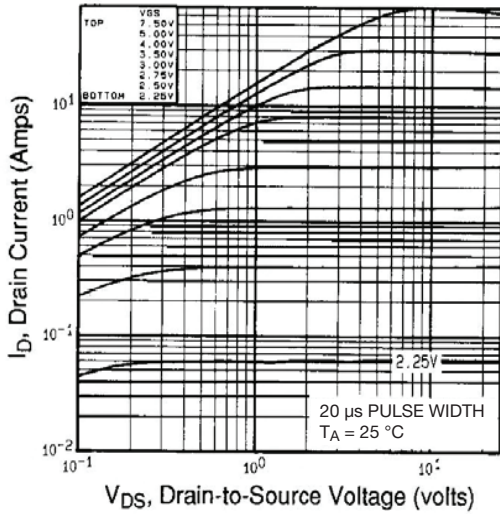


Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ °C}$

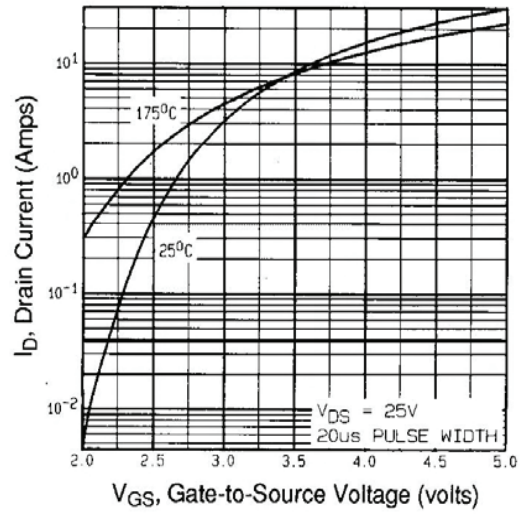


Fig. 3 - Typical Transfer Characteristics

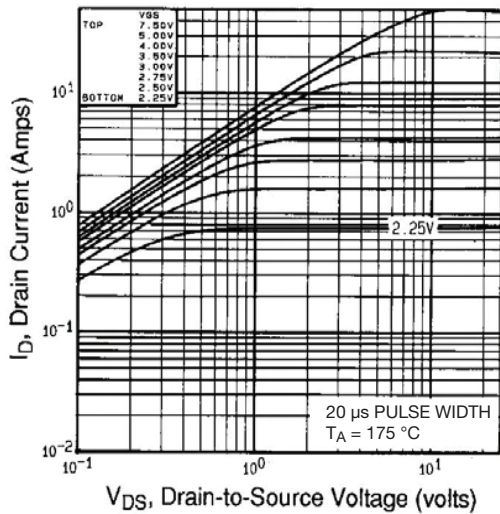


Fig. 2 - Typical Output Characteristics,  $T_A = 175\text{ °C}$

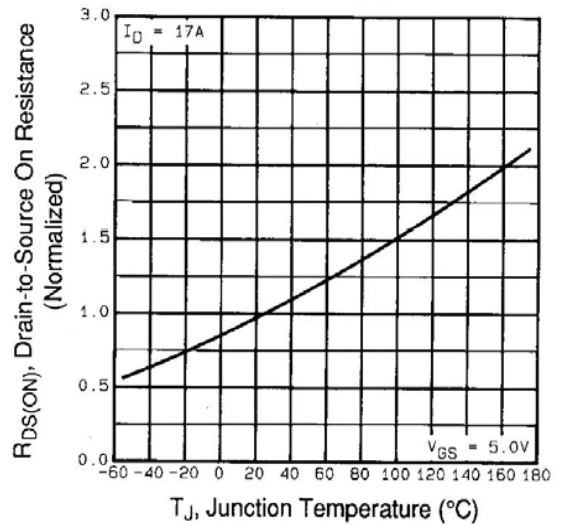


Fig. 4 - Normalized On-Resistance vs. Temperature

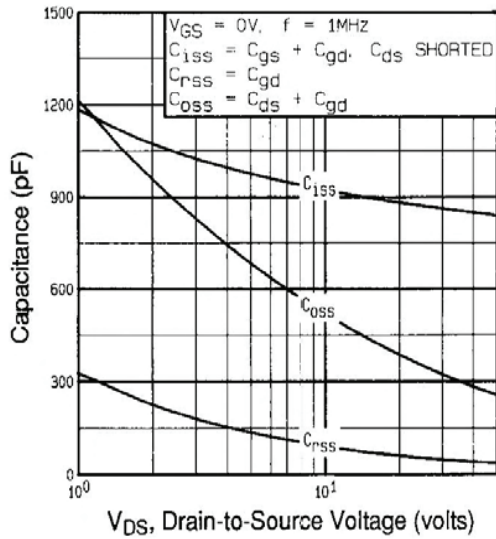


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

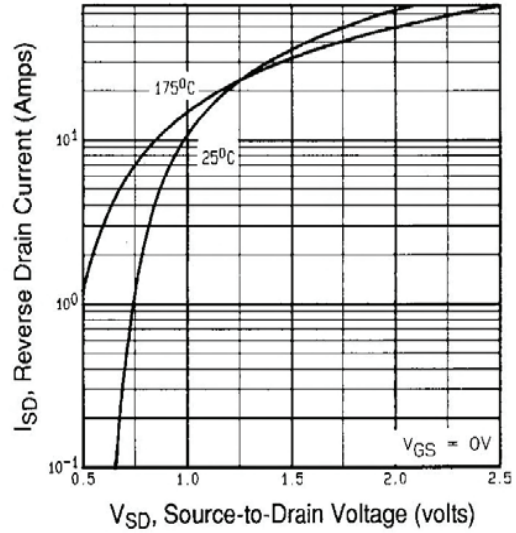


Fig. 7 - Typical Source-Drain Diode Forward Voltage

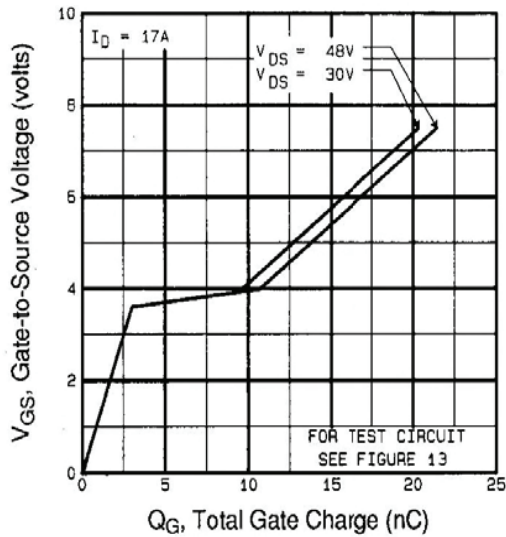


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

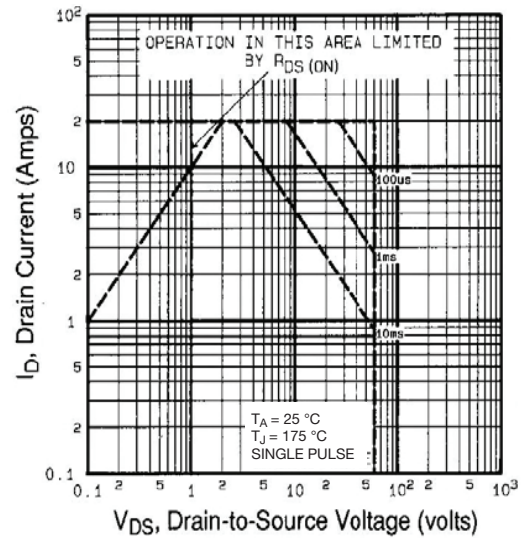


Fig. 8 - Maximum Safe Operating Area

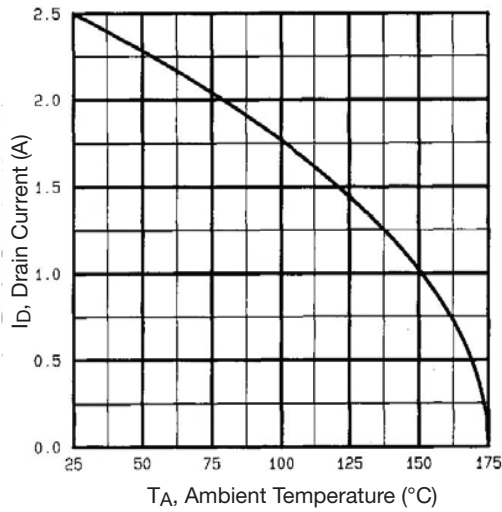


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

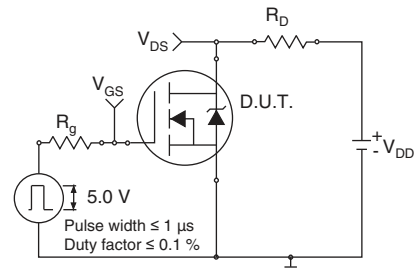


Fig. 10a - Switching Time Test Circuit

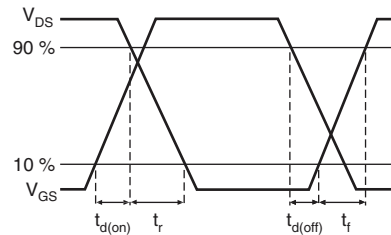


Fig. 10b - Switching Time Waveforms

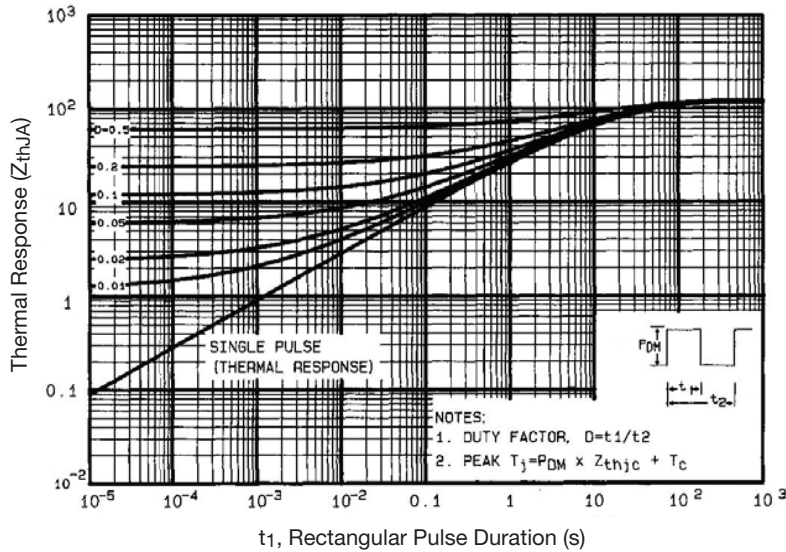


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

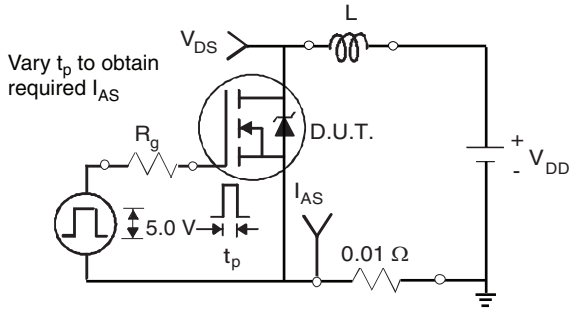


Fig. 12a - Unclamped Inductive Test Circuit

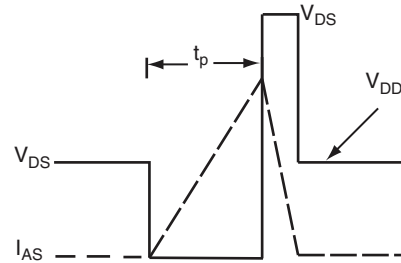


Fig. 12b - Unclamped Inductive Waveforms

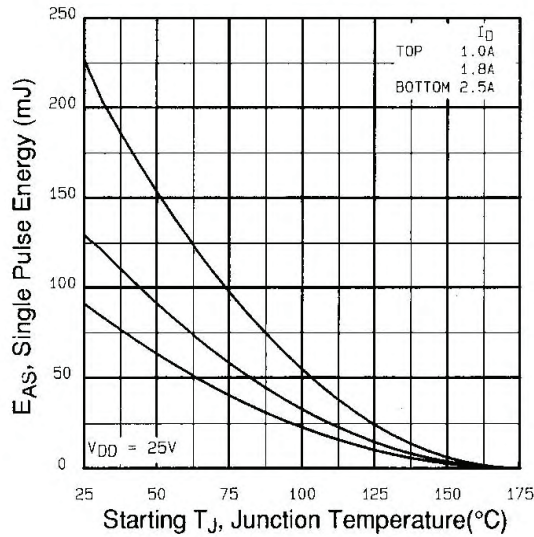


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

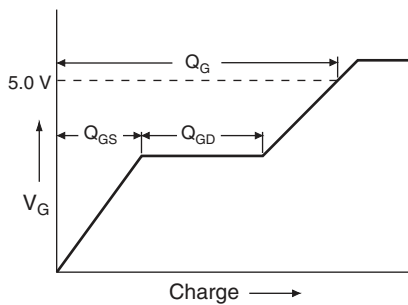


Fig. 13a - Basic Gate Charge Waveform

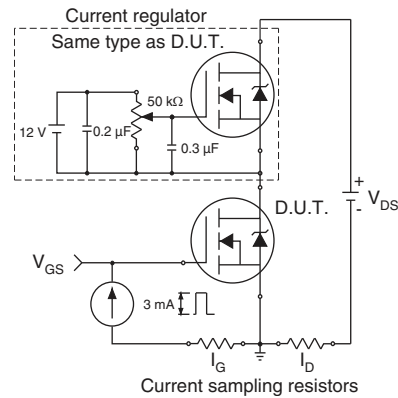
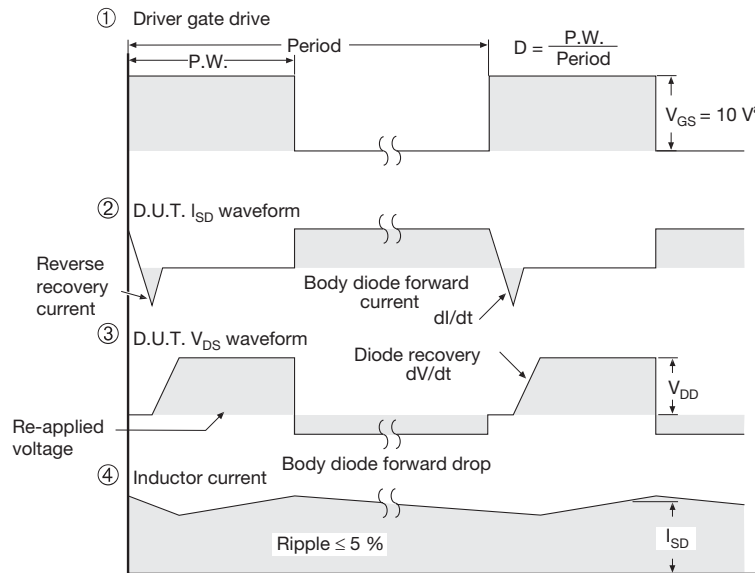
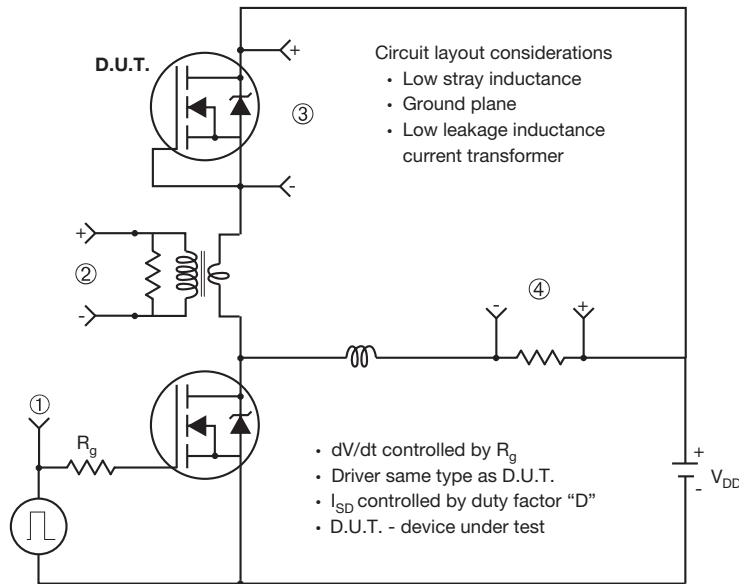


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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## HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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