High-performance, High-accuracy PMIC for High-end MPU and FPGA Power Solutions

MCP16701

General Description

The MCP16701 is a 2.7V-5.5V input Power Management Integrated Circuit (PMIC) dedicated to FPGA and high-end MPU applications. The MCP16701 supports commercial and industrial applications.

It can be configured in-circuit directly by the end user to support a very large number of FPGA use cases. The programming interface is I^2C, supporting clock rates up to 3.4 MHz.

The MCP16701 integrates 13 power channels distributed as eight parallelable 1.5A Buck regulators, four 300 mA LDOs, and one low-input/low-output voltage LDO Controller using an external MOSFET.

The eight 1.5A Buck regulators can be operated either independently or in parallel to support higher currents, in groups of up to four. The paralleling technique relies on the matching of the power switches' resistances and does not require the complication of an additional current-sharing loop. The part count and solution footprint are also reduced since all paralleled channels share the same inductor, while the required magnetic volume is the same as in equivalent multiphase architectures.

As a result of the pin arrangement, paralleling up to 4 channels allows for a total of 6A output current with the recommended layout.

The switching frequency of the Buck channels defaults to 2 MHz, and the switching phases can be also programmed. Furthermore, the switching frequency can be synchronized to an external clock within the 3-5 MHz range. The frequency synchronization technique can achieve zero phase error (after synchronization) between the incoming synchronization clock and the Buck converters' turn-on switching, such that the timing of the switching events can be accurately established.

The buck output voltage setting spans from 0.6V to 1.6V in 12.5 mV increments and from 1.6V to 3.8V in 25 mV increments, and can be as accurate as ±0.8% (V_{FB} ≥ 1V) over temperature. Feedback resistors are internal, thus improving total accuracy (due to superior matching in integrated form) and further reducing part count and solution space.

The four 300 mA high-accuracy (±1% over temp), high-PSRR LDOs can also be cascaded (in groups of two) to the output of a DC-DC channel, thus improving overall conversion efficiency. LDOs are typically dedicated to sensitive analog loads such as PLL supply rails.

LDOs' output voltages are also programmable from 0.6V to 1.6V in 12.5 mV increments and from 1.6V to 3.8V in 25 mV increments.

The MCP16701 additionally integrates one low-input/low-output high-accuracy LDO Controller, using an inexpensive and small external N-channel MOSFET as a pass device. This solution is intended to provide a clean supply voltage to SERDES lanes. It can do so while maintaining high PSRR, low noise, fast load transient performance, and achieving scalability for different applications.

The LDO Controller typically post-regulates the output of one (or more, if paralleled) Buck channels to a slightly lower regulated voltage. Protection features are provided by the upstream Buck stage. The output voltage of the LDO Controller is programmable from 0.6V to 1.6V in 12.5 mV increments.

The programming and communication interface is I^2C (High-speed mode i.e. up to 3.4 MHz) with optional support of Packet Error Checking (PEC). An open-drain interrupt pin (nINTO) allows signaling of anomalies to either the FPGA/FPGA SoC or to a host MCU/MPU.

For Buck channels, either main or replica, the default power-up voltage values, as well as all the sequencing among power channels, associated delays, and many other settings, are written by the user in an embedded EEPROM memory (which is protected against accidental write operations) so that different use cases can be addressed without the need for dedicated product variants from the factory. This step may be done during prototyping and also at board manufacturing, prior to FPGA programming, and takes a negligible amount of time in the production flow. Nevertheless, preprogrammed customized parts can be ordered from Microchip to support large-volume applications.

The MCP16701 features two different reset outputs:

- nRSTO_A: the nRSTO_A signal is deasserted (with a user-programmable delay) after all enabled channels have reached their regulation voltage. The nRSTO_A signal is meant to flag to a system supervisor (e.g. housekeeping MCU) that the whole application has started correctly.
- nRSTO_P: the nRSTO_P signal is deasserted (with a user-programmable delay) after a user-defined subset of all enabled channels have reached their regulation voltage. The nRSTO_P signal is meant to drive the DEVRST_N input of PolarFire FPGAs/SoCs.

The MCP16701 power management settings allow for the implementation of low-power modes commanded by a GPIO pin (MODE input of MCP16701). Any channel can also be selectively and permanently set in AutoPFM or FPWM, or even turned on/off based on the MODE input.

A programmable, windowed Watchdog Timer with uncommitted open-drain output (nWDO) is also available.

The MCP16701 is available in a 64-pin, 8 mm x 8 mm VQFN package with an operating junction temperature range from –40°C to +105°C.

Features

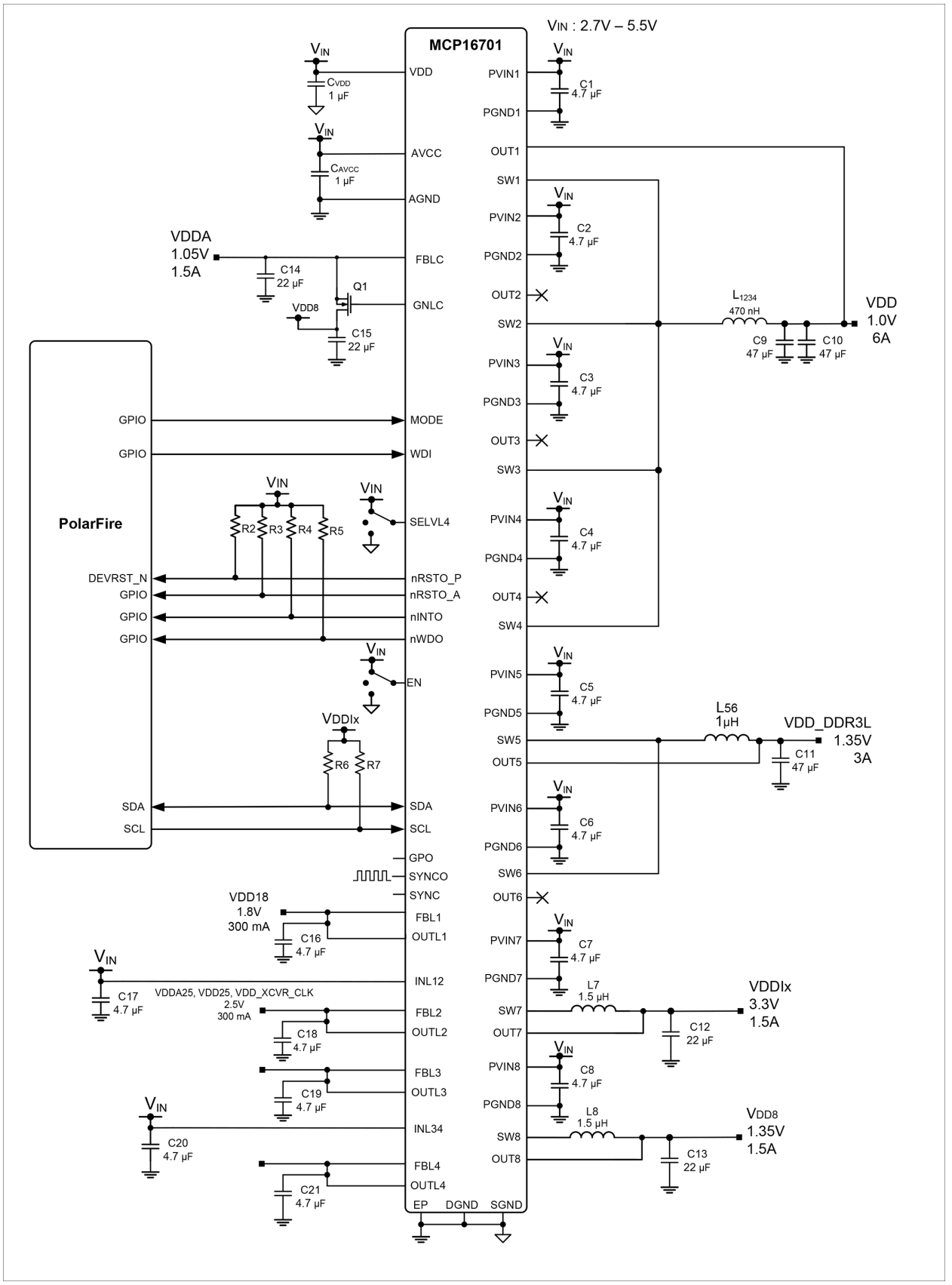
- Input Voltage: 2.7V to 5.5V
- Eight 1.5A Buck DC-DC Channels
- Four 300 mA High-accuracy LDOs
- One High-accuracy, High-PSRR LDO Controller Using External N-channel MOSFET (SERDES Lanes Supply)
- ±0.8% Output Voltage Accuracy for Bucks (VDD), for $V_{FB} \geq 1V$
- -1.5%/+1% Output Voltage Accuracy for the LDO Controller, for $V_{FB} \geq 0.9V$
- ±1% Output Voltage Accuracy for LDOs, for $V_{FB} \geq 1.8V$
- Directly Parallelable Buck Channels Power Stages – up to 4 – for a Combined Current Capability up to 6A
- Tight Rds(ON) Matching of Parallelable Channels for Good Current Sharing
- Minimum Number of Inductors: Paralleled Buck Channels Share the Same Inductor
- Programmable Output Voltage for all Buck and LDO Channels 0.6V to 3.8V – No External Feedback Resistors Required
- 100% Duty Cycle Capability of Buck Channels
- LDO Controller Output Voltage 0.6V to 1.6V/12.5 mV Steps
- Reference Ground (REFGND) Can be Remotely Routed to the Load Ground (Pseudo Remote Sensing)
- Low-Noise Forced-PWM and Light-load High-efficiency Mode Available (Pin-selectable or Bit Control)
- External Synchronization of Switching Frequency, with Accurate Switching-events Time Positioning
- Selectable Phase (0°, 90°, 180° or 270°) for Buck Channels
- Global RESET (nRSTO_A) with Programmable Deassertion Delay
- User-defined RESET (nRSTO_P) with Programmable Deassertion Delay – Ideal for PolarFire FPGA DEVRST_N Interfacing
- 3.4 MHz I^2C Interface

- In-circuit Programmable: On-board Embedded EEPROM for Default Power-up Configuration Programming
- EEPROM Write Password Protection
- Dedicated VDD Supply Pin for EEPROM and Interface Allows Programming Without Powering up the Application
- Reconfigurable During Run Time
- Hiccup-mode Current Limit for Buck Channels (Can be Disabled)
- Programmable Thermal Early Warning and Thermal Shutdown Protection
- nINTO Pin (Interrupt Flag) with Selectable Interrupt Masking for Each Channel
- 64-Pin VQFN Package, 8 mm x 8 mm
- –40°C to +105°C Junction Temperature Range

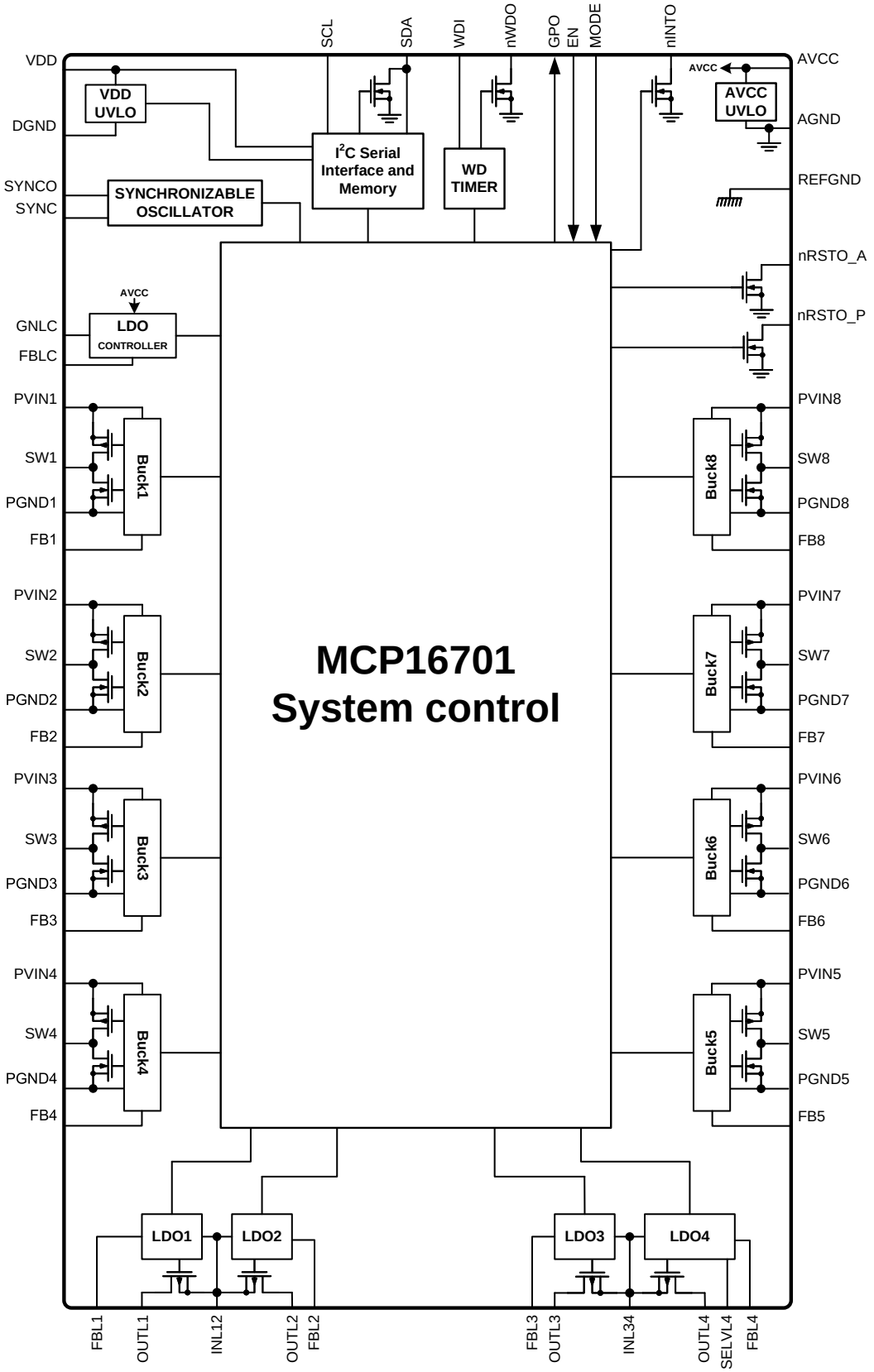
Applications

- High-Performance MPUs Power Supply Solutions
- µC/µP, FPGA, and DSP Power

Polarfire FPGA Typical Application



Functional Block Diagram



1. Pin Description

Pin Number	Pin Name	Description
1	FB1	Buck1 feedback. Connect to VOUT1 for output sensing for Buck Channel 1. Buck1 is always a main channel.
2	PVIN1	Power Input Voltage of Buck Channel 1.
3	SW1	Switch Node of Buck Channel 1. Internal power MOSFET switches and external inductor connection.
4	PGND1	Power Ground of Buck Channel 1.
5	PGND2	Power Ground of Buck Channel 2.
6	SW2	Switch Node of Buck Channel 2. Internal power MOSFET switches and external inductor connection.
7	PVIN2	Power Input Voltage of Buck Channel 2.
8	FB2	Buck2 feedback. Connect to VOUT2 for output sensing of Buck Channel 2 in main operation. Connect to PVIN2, ground or leave floating when Buck2 is defined as a replica and paralleled to Buck1.
9	FB3	Buck3 feedback. Connect to VOUT3 for output sensing of Buck Channel 3 in main operation. Connect to PVIN3, ground or leave floating when Buck3 is defined a as replica and paralleled to Buck2.
10	PVIN3	Power Input Voltage of Buck Channel 3.
11	SW3	Switch Node of Buck Channel 3. Internal power MOSFET switches and external inductor connection.
12	PGND3	Power Ground of Buck Channel 3.
13	PGND4	Power Ground of Buck Channel 4.
14	SW4	Switch Node of Buck Channel 4. Internal power MOSFET switches and external inductor connection.
15	PVIN4	Power Input Voltage of Buck Channel 4.
16	FB4	Buck4 feedback. Connect to VOUT4 for output sensing of Buck Channel 4 in main operation. Connect to PVIN4, ground or leave floating when Buck4 is defined as a replica and paralleled to Buck3.
17	NC	Not connected. Leave floating.
18	FBL1	LDO1 feedback. Connect to the point of regulation of the load of LDO1, fed by pin OUTL1.
19	OUTL1	LDO1 output. Decouple OUTL1 to ground with a 2.2 µF (minimum) ceramic capacitor.
20	INL12	Input voltage for LDO1 and LDO2. Decouple INL12 to ground with a 2.2 µF (minimum) ceramic capacitor.
21	OUTL2	LDO2 output. Decouple OUTL2 to ground with a 2.2 µF (minimum) ceramic capacitor.
22	FBL2	LDO2 feedback. Connect to the point of regulation of the load of LDO2, fed by pin OUTL2.
23	nINTO	Interrupt output (open-drain).
24	nRSTO_P	Programmable reset open-drain output. nRSTO_P will be deasserted (high-Z), with a default or user-defined delay, after a user-defined subset of all enabled regulators (which are part of the start-up sequence) have reached their POK thresholds. Typically interfaced to the DEVRST_N pin of PolarFire FPGAs.
25	nRSTO_A	Global reset open-drain output (default). nRSTO_A will be deasserted (high-Z), with a default or user-defined delay, after all enabled regulators (which are part of the start-up sequence) have reached their POK thresholds.
26	NC	Not connected. Leave floating.
27	FBL3	LDO3 feedback. Connect to the point of regulation of the load of LDO3, fed by pin OUTL3.
28	OUTL3	LDO3 output. Decouple OUTL3 to ground with a 2.2 µF (minimum) ceramic capacitor.
29	INL34	Input voltage for LDO3 and LDO4. Decouple INL34 to ground with a 2.2 µF (minimum) ceramic capacitor.
30	OUTL4	LDO4 output. Decouple OUTL4 to ground with a 2.2 µF (minimum) ceramic capacitor.

Pin Description (continued)

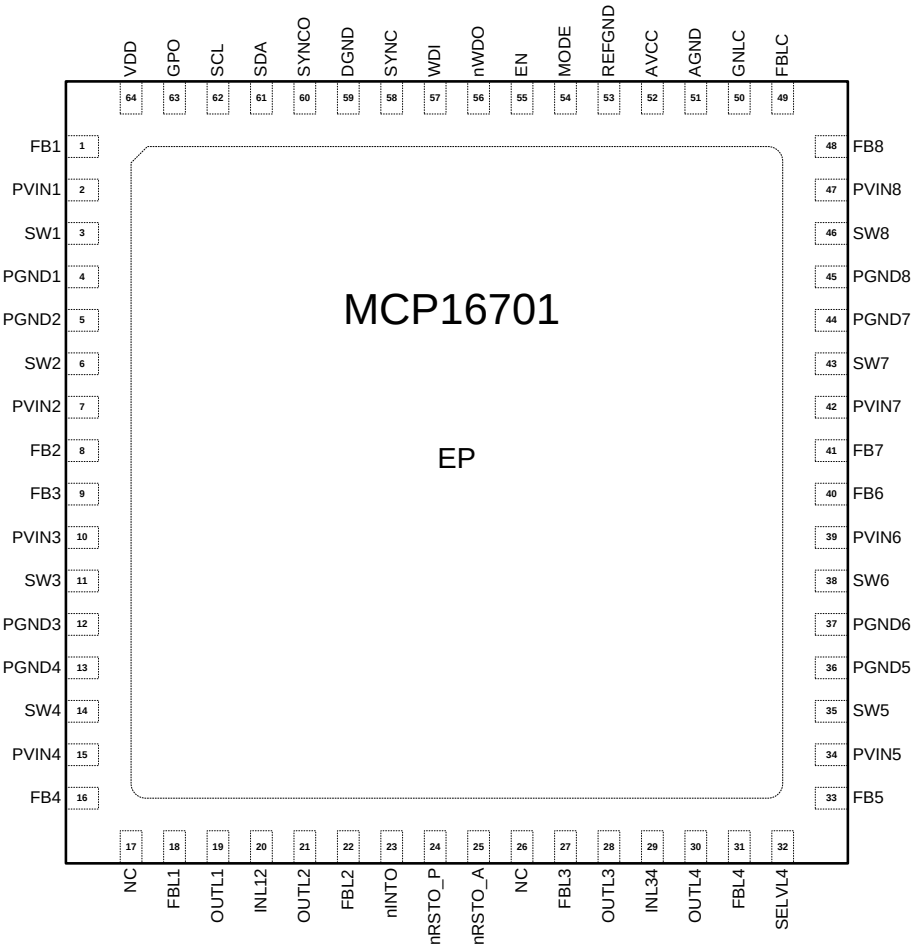
Pin Number	Pin Name	Description
31	FBL4	LDO4 feedback. Connect to the point of regulation of the load of LDO4, fed by pin OUTL4.
32	SELVL4	LDO4 Voltage Selection Pin. If configured appropriately, this pin selects between 1.8V and 3.3V on LDO4. Used for dual-voltage SD Card support. **Do not leave floating.**
33	FB5	Buck5 feedback. Connect to VOUT5 for output sensing of Buck Channel 5. Buck5 is always a main channel.
34	PVIN5	Power Input Voltage of Buck Channel 5.
35	SW5	Switch Node of Buck Channel 5. Internal power MOSFET switches and external inductor connection.
36	PGND5	Power Ground of Buck Channel 5.
37	PGND6	Power Ground of Buck Channel 6.
38	SW6	Switch Node of Buck Channel 6. Internal power MOSFET switches and external inductor connection.
39	PVIN6	Power Input Voltage of Buck Channel 6.
40	FB6	Buck6 feedback. Connect to VOUT6 for output sensing of Buck Channel 6 in main operation. Connect to PVIN6, ground or leave floating when Buck6 is defined as a replica and paralleled to Buck5.
41	FB7	Buck7 feedback. Connect to VOUT7 for output sensing of Buck Channel 7 in main operation. Connect to PVIN7, ground or leave floating when Buck7 is defined as replica and paralleled to Buck6.
42	PVIN7	Power Input Voltage of Buck Channel 7.
43	SW7	Switch Node of Buck Channel 7. Internal power MOSFET switches and external inductor connection.
44	PGND7	Power Ground of Buck Channel 7.
45	PGND8	Power Ground of Buck Channel 8.
46	SW8	Switch Node of Buck Channel 8. Internal power MOSFET switches and external inductor connection.
47	PVIN8	Power Input Voltage of Buck Channel 8.
48	FB8	Buck8 feedback. Connect to VOUT8 for output sensing of Buck Channel 8 in main operation. Connect to PVIN8, ground or leave floating when Buck8 is defined as a replica and paralleled to Buck7.
49	FBLC	LDO Controller feedback. Connect to the point of regulation of the load, which is connected to the source of the external N-channel MOSFET. The typical load of the LDO Controller will be the SERDES lanes core rail of the FPGA.
50	GNLC	LDO Controller gate. Connect to the gate of the external N-channel MOSFET.
51	AGND	Analog ground for control section. AGND is also the return for the LDO Controller.
52	AVCC	Analog supply voltage for control section (2.7V to 5.5V). Locally decouple pin AVCC to pins AGND and REFGND with a 1 µF (minimum) ceramic capacitor. AVCC is also the supply voltage for the gate drive of the LDO Controller.
53	REFGND	All reference voltages are returned to this pin. For best regulation accuracy, route REFGND free from any parasitic voltage drops up to the grounding point of the load.
54	MODE	Buck channels high-efficiency light-load mode selection pin. Drive this pin HIGH to force FPWM operation. Leave floating or connect to ground to enable AutoPFM. MODE is internally pulled down through a 100 kΩ resistor.
55	EN	Enable input. Set EN to HIGH to turn on the power channels. Set to LOW to turn power channels off.
56	nWDO	Watchdog Output (open drain).
57	WDI	Watchdog Input.
58	SYNC	External synchronization pin. A reference clock frequency can be provided externally to the SYNC pin, resulting in the switching frequency of the Buck regulators being ½ of the SYNC frequency. Feeding SYNC with an external clock will also cause the Buck channels to operate in CCM mode (aka FPWM), regardless of the MODE selection pin (unless masked by configuration). SYNC is internally pulled down to DGND through a 100 kΩ resistor.

Pin Description (continued)

Pin Number	Pin Name	Description
59	DGND	Digital Ground. Return for I^2C interface.
60	SYNCO	Programmable SYNChronization Output pin. When enabled, this pin provides a square wave that can be used to synchronize other DC-DC converters in the system.
61	SDA	I^2C interface Serial Data.
62	SCL	I^2C interface Serial Clock.
63	GPO	General Purpose Output.
64	VDD	Digital supply voltage for EEPROM memory, I^2C interface, and volatile registers. VDD can be applied independently from all other supply rails. Decouple VDD to DGND with a 1 µF (minimum) ceramic capacitor.
—	EP	Exposed pad. Connect to a ground plane with vias to ensure good thermal properties.

1.1 Package Type

Figure 1-1. 64-Lead 8x8x0.9 mm VQFN (KCX) – Top View.



2. Functional Description

2.1 Buck Channels and Related External Components

The MCP16701 Buck channels are based on peak-current-mode control architecture and have internal frequency compensation for the voltage regulation loop. The slope compensation is optimized for inductors in the 1 µH to 2.2 µH range. A minimum output capacitor of 22µF is required for stable operation. Output capacitance can be increased if necessary, however, the maximum output capacitance value should be limited to avoid engaging hiccup-mode overcurrent protection during the initial soft-start ramp and during DVS operation.

The recommended input decoupling capacitance on each Buck channel is 4.7 µF.

The Buck channels can operate either in Forced PWM mode (Continuous Inductor Current mode), where the inductor current is allowed to go negative, or in Automatic PFM mode, where the inductor current is not allowed to go negative through Zero-Current Detection (ZCD) and diode emulation of the low-side MOSFET.

The switching frequency in Forced PWM mode is nominally 2 MHz and can be displaced through I^2C by ±16.5% to prevent interference with other sensitive system blocks.

For the MCP16701, parallel operation is constrained to Buck channels placed on the same edge of the device. Buck channels placed on opposite edges cannot be connected in parallel. Therefore, the two separate parallel groups are Buck1-to-Buck4 and Buck5-to-Buck8. Buck1 and Buck5 are always either independent or MAIN.

2.2 LDO Channels with Forced Bypass Mode and Related External Components

The MCP16701 integrates four 300 mA high-accuracy (±1% over temperature, for $V_{FB} \geq 1.8V$), high-PSRR LDOs. The LDOs can also be cascaded (in groups of two) to the output of a DC-DC channel, thus improving overall conversion efficiency. LDOs are typically dedicated to sensitive analog loads such as PLL supply rails.

LDOs' output voltages are also programmable from 0.6V to 1.6V in 12.5 mV increments and from 1.6V to 3.8V in 25 mV increments.

2.2.1 LDO Mode Operation

The MCP16701 LDOs are designed for operation with low-ESR ceramic output capacitors of 2.2 µF (minimum value) for loads up to 150 mA, and of 4.7 µF (minimum value) for loads up to 300 mA. The total output capacitance should not exceed 20 µF.

The LDOs can be used with an input voltage (INL) less than or equal to the voltage at pin AVCC. As such, they can operate as post-regulators cascaded to a buck output, if its output voltage is programmed above 2.7V.

2.2.2 Forced Bypass Mode Operation

The forced bypass operation of LDOs can change the functionality of the LDOs into four additional software-controlled load switches. Forced Bypass mode is enabled by setting bit FBYPM (default is "0" = normal LDO mode).

When the FBYPM is set, the LDO is programmed to deliver a 5.25V output voltage to the load (the LDO will always operate in dropout). However, if for any reason the input voltage INLxx overshoots above 5.25V, the output of the LDO will try to regulate at 5.25V, thus protecting the load from overvoltage.

2.2.3 LDO4 with External Voltage Selection (SELVL4 PIN)

LDO4 features a dedicated pin (SELVL4) to control its output voltage between 1.8V and 3.3V. This is done to implement support of dual-voltage SD Cards.

The SELVL4 can be changed on-the-fly during run time.

The table below summarizes the mode of operation of LDO4 depending on the configuration bits ENSELVL4, POLSELV/FBYPM and the SELVL4 pin logic level.

Table 2-1. LDO4 FUNCTIONALITY VS. NVM_ENSELVL4, POLSELV/FBYPM, SELVL4.

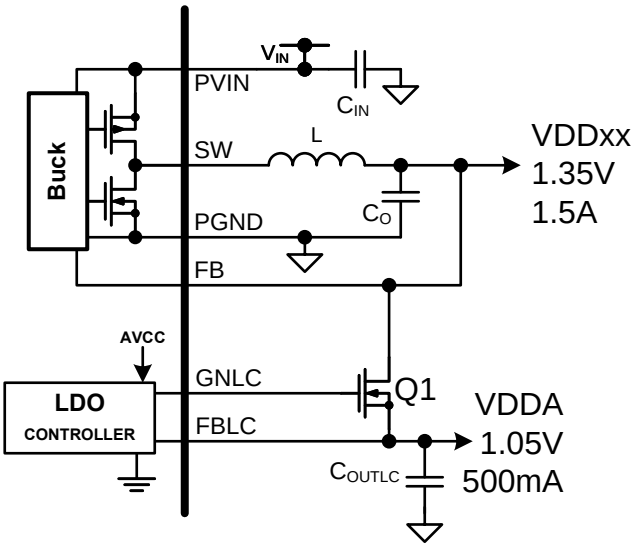
NVM_ENSELVL4	POLSELV/FBYPM	SELVL4 Pin	VOUT LDO4	SELVL4S Status Bit
0	0	Don't care	From VSET[7:0]	0
0	1	Don't care	Forced Bypass Mode	0
1	0	0	3.3V	0
1	0	1	1.8V	1
1	1	0	1.8V	0
1	1	1	3.3V	1

2.3 LDO Controller and Related External Components

The LDO Controller is intended to drive an external N-channel MOSFET (Q1 in the figure below). There is no charge pump for gate overdrive, and the turn-on of the external MOSFET is only based on its gate threshold voltage and the available supply voltage (AVCC).

The LDO Controller output voltage (sensed at FBLC) is programmable from 0.6V to 1.6V in 12.5 mV increments.

Figure 2-1. LDO Controller Concept.



The drain of the external MOSFET Q1 is connected to the output of one of the Buck channels. This can either be a dedicated or a shared output. In the first case, the output voltage of the front-end Buck can be optimized for best efficiency and performance. In the second case, efficiency optimization may not be possible, and the user must ensure that the LDO controller output rail sequencing is compatible with the shared Buck output (i.e. LDO Controller is turned on after the shared Buck output, and turned off before the shared Buck output or at least at the same time).

Possible external MOSFETs Q1 for the LDO Controller are listed in LDO Controller External MOSFET Selection.

Overload protection for the LDO Controller channel is supported by the Buck channel, which powers the input of the LDO Controller (external MOSFET drain). The LDO Controller does not have any autonomous overcurrent protection.

For safety and robustness against short circuits on the LDO Controller output, the hiccup mode protection of the Buck feeding the LDO Controller should never be disabled; otherwise, excessive power dissipation across the external MOSFET may result.

The MCP16701 LDO Controller is designed for operation with low-ESR ceramic output capacitors of 4.7 µF (minimum value) for loads up to 300 mA, and 22 µF (minimum value) for loads up to 1.5A. The total output capacitance should not exceed 120 µF.

2.4 Main Oscillator with External Synchronization

The MCP16701 dedicated synchronizable oscillator generates the switching frequencies and phases for all DC-DC channels.

In free-running mode, the oscillator frequency is nominally 8 MHz (supporting selectable 4-phase operation of the Bucks). Each Buck runs at 2 MHz, and its turn-on switching can be programmed to 0°, 90°, 180° or 270° phase-shift.

The oscillator always starts on its own free-running frequency. In the absence of external frequency synchronization fed at SYNC, FSD[1:0] bits may shift the oscillator free-running frequency as soon as the volatile registers become operational. Until then, FSD[1:0] = 00.

The oscillator can be externally synchronized to an external clock fed at pin SYNC. This clock will be typically generated by a GPIO of the FPGA/MPU or the housekeeping MCU and could also be spread-spectrum modulated.

As soon as the SYNC signal is detected, the oscillator frequency is locked to the SYNC frequency. Therefore, the external synchronization used in the MCP16701 falls into the category of PLL-based techniques.

When the SYNC signal disappears, the PLL filter is slowly reset, and the controlling voltage for the oscillator frequency seamlessly decays towards the free-running value.

2.5 Control Signals and Power States

2.5.1 Interfacing Signals

The MCP16701 is interfaced to the system supervisor by means of I^2C interface pins. The I^2C interface supports High-speed mode (Hs-mode) data transfer with a bit rate up to 3.4 Mbit/s, as described in the official I^2C standard, with optional support of Packet Error Checking (PEC). The I^2C interface is always accessible, even in the OFF state, as long as the VDD pin is powered and above its UVLO threshold. AVCC UVLO is irrelevant to I^2C interface operation. Further details about the I^2C interface of the MCP16701 are given in the I^2C section of the data sheet.

2.5.2 nRSTO_A, nRSTO_P, nINTO

The MCP16701 features two different reset outputs:

- nRSTO_A: the nRSTO_A signal is deasserted (with a user-programmable delay) after all enabled channels have reached their regulation voltage. The nRSTO_A signal is meant to flag to a system supervisor (e.g. housekeeping MCU) that the whole application has been correctly started.
- nRSTO_P: the nRSTO_P signal is deasserted (with a user-programmable delay) after a user-defined subset of all enabled channels have reached their regulation voltage. The nRSTO_P signal is meant to drive the DEVRST_N input of PolarFire FPGAs/SoCs.

Pin nINTO is an active-low, open-drain interrupt output pin. The nINTO pin goes low every time a Fault is detected, and the corresponding Interrupt Masking bit is cleared, thus signaling any anomalies to either the FPGA/FPGA SoC or to a host MCU/MPU.

The interrupt is maskable for each channel.

2.5.3 GPO Output

MCP16701 also provide a general-purpose output pin, which can be used in two ways depending on its NVM_ENABLE bit setting:

1. **NVM_ENABLE = '1':** GPO is used as an auxiliary command for an external power stage during turn-on/off sequences.
   In this mode, GPO will be asserted during the start-up sequence and deasserted during the turn-off sequence in a similar way as other power channels.

   In any case, GPO does NOT influence the assertion/deassertion of nRSTO_A/nRSTO_P.

   The assertion polarity (asserted level = HIGH or LOW) can be controlled by the GPOPOL bit. Therefore, it is possible to have the GPO pin starting HIGH or LOW at the beginning of the start-up sequence and to have GPO toggle to the opposite level during start-up (if ENABLE = '1').

   If ENABLE = '1', during the turn-off sequence, the GPO will toggle to the deassertion level at the time programmed by its OFFDLY[5:0] bits.

   In this mode, it is recommended NOT to change ENABLE and/or GPOPOL in the volatile shadow registers during run time, or to restore them to their default values prior to initiating a turn-off sequence.
2. **NVM_ENABLE = '0':** GPO is only activated by the user during run time i.e. after the start-up sequence, through interface commands that overwrite the ENABLE and/or the GPOPOL bits.

The user is responsible for ensuring that ENABLE = '0' at the beginning and during the turn-off sequence to avoid unwanted potential toggling of GPO at the programmed OFFDLY[5:0].

2.5.4 Programmable Watchdog Timer and WDI, nWDO Pins

The Watchdog Timer functionality can be chosen as a basic GPIO-cleared WDI/nWDO Watchdog Timer (NVM_WDMODE = '0', EEPROM only bit) or a more complex, interface-cleared internal Watchdog Timer with WDI transitions count and hardware reset and restart (NVM_WDMODE = '1').

Before the watchdog can run, the NVM_WDEN/WDEN bit must be set. This applies to both modes of operation.

The need for two different modes arises because:

- For **NVM_WDMODE = '0'**, it is assumed that the host does NOT have an embedded watchdog, or the embedded watchdog is redundant. In this case, the WDI pin is driven by a host GPIO, which is toggled intentionally by software. In this scenario, the transition of WDI is a sign of system good health (software is running and periodically toggling WDI). The lack of WDI transition within the programmed time window is a symptom of software being stuck.
- For **NVM_WDMODE = '1',** it is assumed that the host already has an embedded watchdog which can assert a software reset. In this case, WDI will be toggled because of a host watchdog reset assertion. Therefore, in this scenario, the transition of WDI means that the software is not running properly. If WDI is repeatedly triggered, this is a sign of a malfunction that cannot be recovered by only resetting the software, and therefore, a full hardware reset is invoked.

Additional information regarding Watchdog Timer modes can be found in WDI/nWDO Watchdog Timer Modes.

2.5.5 MODE Pin and Low-power/Standby Mode Control

The MODE pin is typically used to switch the MCP16701 between a high-performance mode (Forced PWM) and a low-power mode (AutoPFM).

As a note of caution, when the MODE pin/bit is changed, the output voltage of the regulator may also change (dictated by the VSET0/VSET1 values). Each VSET register corresponds to an imposed mode of operation (VSET0 = AutoPFM,VSET1 = FPWM).

The MODE pin features programmable polarity, which is defined by an EEPROM bit (NVM_INVMODEP, Inversion of MODE Pin). The MODE pin polarity is defined by the hardware configuration and therefore it is only allocated in EEPROM.

It is possible to override the external MODE pin command for every regulator. This is done by setting the MODEPMSK bit. When MODEPMSK is '0', the MODE pin (external command) will have an effect on the corresponding regulator. If MODEPMSK = '1', the external MODE command is disabled, and the operation of the regulator will be determined by the MODEB bit.

This way, it is possible to force some regulators to always operate in a certain mode, regardless of the MODE pin, and/or assign their mode control to software commands only, such that it is possible to activate or suspend external MODE control during run time.

The MODE pin features control interdependency as defined in the following table:

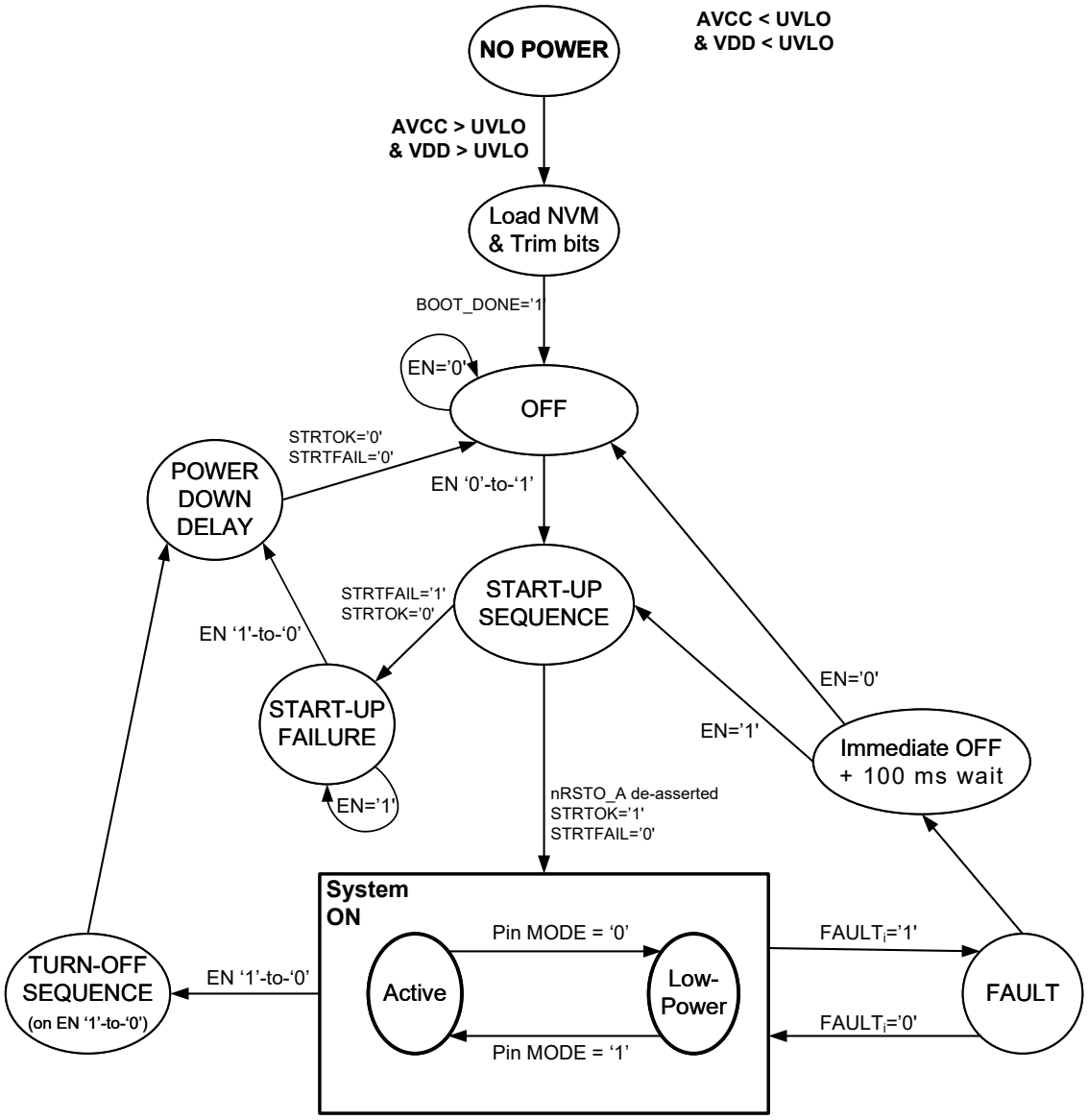
Table 2-2. MODE Pin Configuration

MODE Pin	INVMODEP bit	MODEPMSK bit	MODEB	Output Voltage determined by:	Operation Mode
LOW	0	0	Irrelevant	VSET0[7:0]	AutoPFM
LOW	1	0	Irrelevant	VSET1[7:0]	FPWM
HIGH	0	0	Irrelevant	VSET1[7:0]	FPWM
HIGH	1	0	Irrelevant	VSET0[7:0]	AutoPFM
Irrelevant	Irrelevant	1	0	VSET0[7:0]	AutoPFM
Irrelevant	Irrelevant	1	1	VSET1[7:0]	FPWM

The MODE pin also allows the user to disable desired regulators using DISMODE0 and DISMODE1 bits. By doing so, the power consumption can be further decreased. Please note that when regulators are disabled using the MODE pin, no sequencing or active discharge will be activated, but the start-up of the disabled regulators will be achieved as described by the corresponding ONSR bits.

2.5.6 Power States Definitions

Figure 2-2. Finite State Machine (FSM) States Diagram for MCP16701.

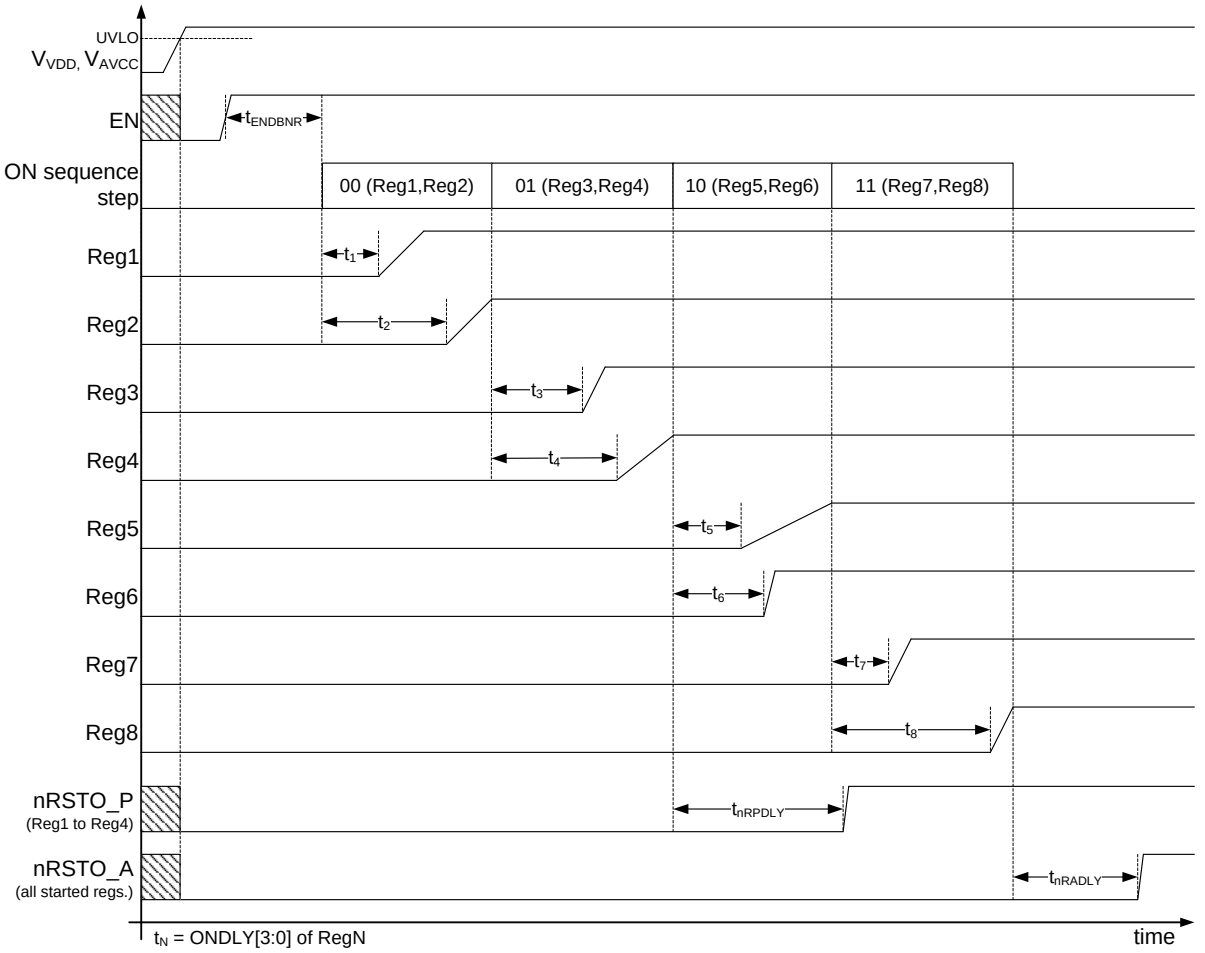


The process by which the MCP16701 exits OFF state and enters the other possible power states is defined as the Power-Up Sequence, which is described in Typical Power-Up Sequence and Timing.

2.6 Power-Up/Power-Down Sequences and Timings

2.6.1 Typical Power-up Sequence and Timing

Figure 2-3. Turn-On Sequence Timing Diagram Example.



Where:

- t_1 to t_8 – are programmable turn-on delays within each sequence step and configured by the ONDLY[3:0] bits
- t_{ENDBNR} – defines the debounce time for the L-to-H (Rising) edge (or initial H status upon AVCC and VDD UVLO release) and is configured by the ENDBNR[2:0] bits
- t_{nRPDLY} – represents the deassertion delays for nRSTO_P and is programmed through the nRPDLY[3:0] bits
- t_{nRADLY} – represents the deassertion delays for nRSTO_A and is programmed through the nRADLY[3:0] bits

For MCP16701, a turn-on (start-up) sequence is typically initiated by the EN pin going HIGH (L-to-H transition).

If EN is connected to VIN and VIN is ramped up, crossing the AVCC and VDD UVLO thresholds, the turn-on sequence will be started.

EN pin transitions (or initial H status upon AVCC and VDD UVLO release) are always deglitched in the analog domain (typically 5-10 µs).

Furthermore, the EN pin transitions (or initial H status upon AVCC and VDD UVLO release) are debounced digitally by an internal programmable timer.

The timing diagram above exemplifies the turn-on sequence.

2.6.2 Power-up Sequence Programming and Flowchart

Figure 2-4. Start-Up Flowchart, Part 1 (ONSEQ[1:0] = '00' and '01').

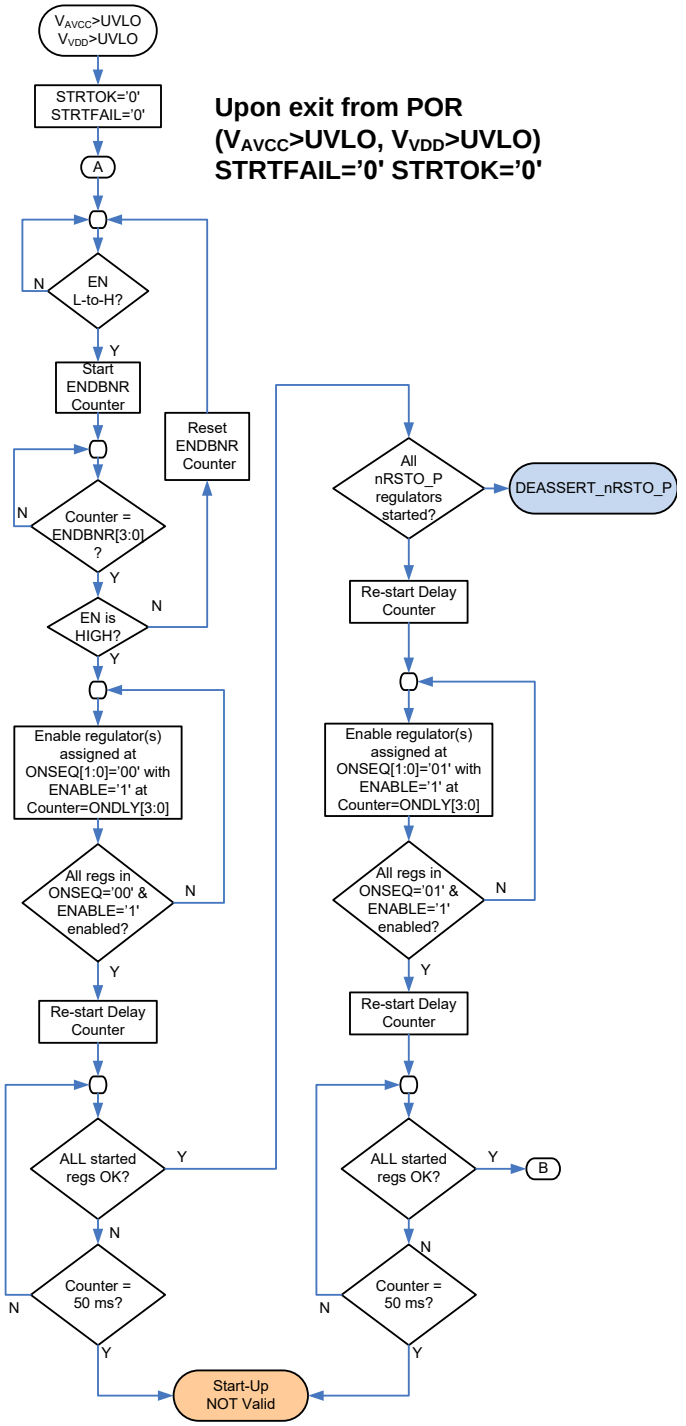
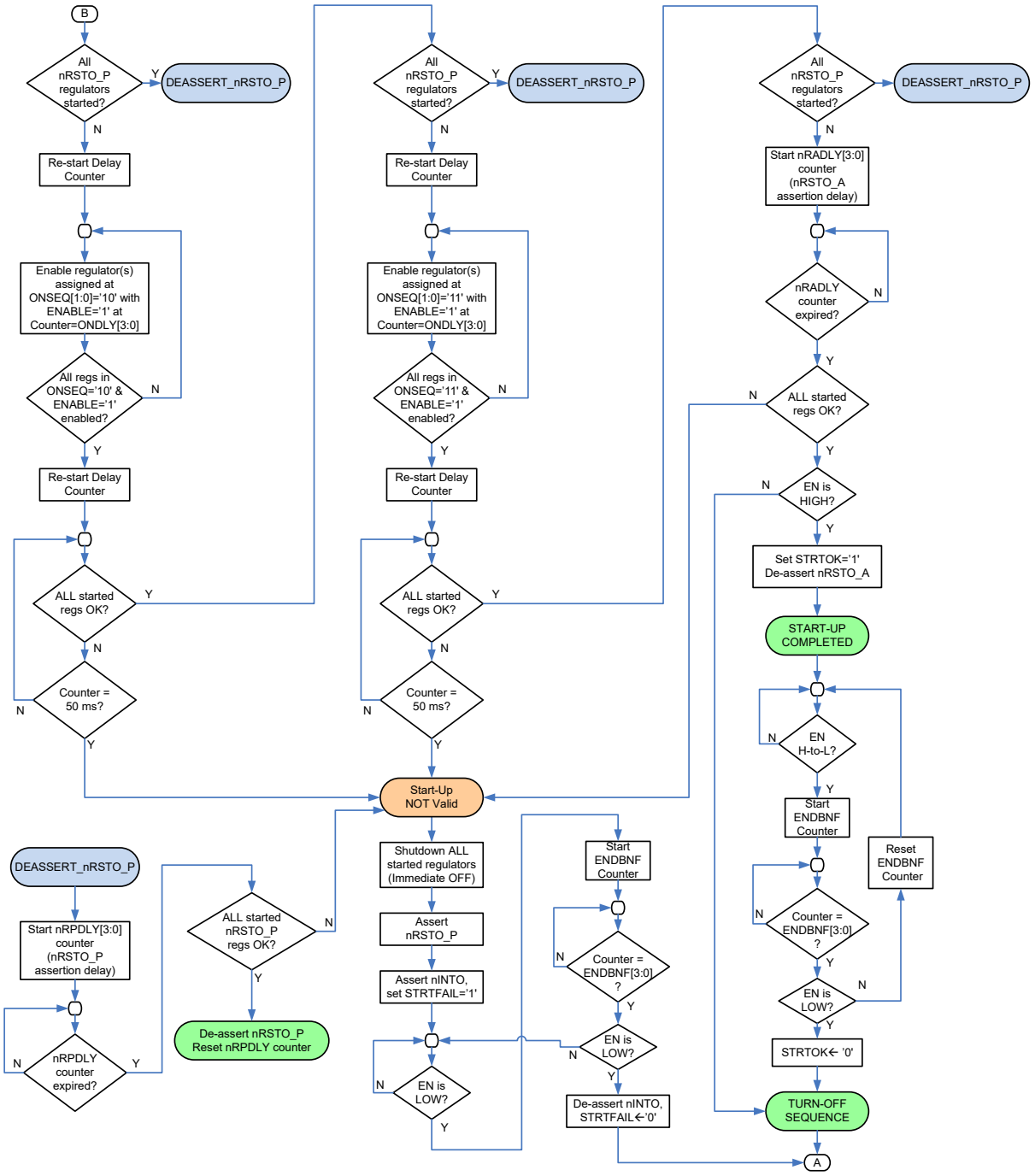


Figure 2-5. Start-Up Flowchart, Part 2 (ONSEQ[1:0] = '10' and '11' – nRSTO_P and nRSTO_A Deassertion).



The MCP16701 supports four different sequence steps and sixteen different delays within each sequence.

This allows for up to 4 x 16 = 64 possible different power channel activation instances.

If a given first output voltage must be fully established before a second output voltage is started, then they should be assigned to different turn-on sequence steps.

Sequence steps are defined by the ONSEQ[1:0] bits. See Table 2-10 for Turn-on Sequence Step Assignment Bit values.

The next sequence step can only be initiated after ALL power channels assigned to the current sequence steps are properly established.

It is recommended to assign power supply rails that have sequencing and relative voltage level requirements - such as the VDD1 and VDD2/VDDQ supply rails of LPDDR2/3/4 memories - to different sequence steps. This ensure that any possible failure of the first channel during start-up will also prevent the subsequent channel from attempting start-up, and the turn-on sequence will be aborted without violating the LPDDRx power supply ramping specifications set by JEDEC standards.

This is especially important when the first channel (powering VDD1) can be exposed to unpredictable loading in the system (despite it is not being recommended to use the LPDDRx VDD1 rail for other purposes).

If different channels are assigned to the same sequence step, their start-up times within the sequence step are purely determined by the turn-on delay (ONDLY[3:0] bits), i.e., the first channel being fully established does NOT condition the start-up of the second channel.

At the conclusion of each sequence step, the proper power-on of ALL regulators previously started is checked. If ALL regulators (including those started in any previous sequence step) have been properly powered-up (POK or bypass POK goes H), then the sequence can continue to the next step.

If ANY of the previously started regulators (including those started in any previous sequence step) have failed to power-up properly (i.e. POK/bypass POK is LOW) after 50 ms since the start of the last regulator in the current sequence step, then the turn-on sequence is immediately aborted, all regulators are shut down through Immediate OFF, nRSTO_P is asserted (if previously deasserted), nINTO output will be asserted, and the STRTFAIL bit will be set.

After the failure of the start-up sequence, even if EN is still H, no further start-up attempts will be made. The MCP16701 expects the host (housekeeping MCU) to detect the failure of the start-up sequence because of the nINTO assertion and STRTFAIL bit readout, and to set EN = L. If EN is set L for the duration determined by ENDBNF[2:0] bits, then nINTO is deasserted and the STRTFAIL bit cleared. Then the turn-on sequencer can accept another EN L-to-H transition.

If EN was connected directly to VIN, power cycling (AVCC and VDD must both fall below the UVLO lower threshold and come back above the UVLO upper threshold) will be the only way to initiate another start-up sequence. This will also reset all status bits (e.g. STRTFAIL) and deassert nINTO.

2.6.3 Typical Power-down Sequencer and Timing Diagram

2.6.3.1 Turn-Off Sequencer

The MCP16701 also supports turn-off sequencing and Immediate OFF.

Unlike turn-on, there are no turn-off sequence steps. All channels are turned off (upon deassertion of EN and debouncing) based solely on their OFFDLY[5:0] bits. The OFFDLY[5:0] delay marks the beginning of the Immediate OFF.

The turn-off sequence is concluded when the last regulator has been turned off through Immediate OFF or the nRSTO_P/_A signals have both been asserted - whichever comes later.

At that point, the PDENDLY[2:0] delay (Power-Down Enable Delay) is started.

During the execution of the turn-off sequence, and for a programmable delay set by the PDENDLY[2:0], the EN pin is masked,and any L-to-H transition will be ignored until the PDENDLY[2:0] delay has expired.

If EN is detected H at the end of PDENDLY, it will be interpreted as a L-to-H transition just after the expiration of PDENDLY, and another start-up sequence will be initiated after validating the EN L-to-H transition through the ENDBNR debounce timer.

2.6.3.2 nRSTO_P/nRSTO_A

Assertion at Turn-Off nRSTO_A and nRSTO_P can be programmed to be asserted at a specific time during the turn-off sequence.

The same table, Turn-off Sequence Step Delay Bits OFFDLY[5:0], also applies to the nRSTO_A/_P assertion.

The choice of the nRSTO_A/P OFFDLY[5:0] bits is entirely up to the user. If OFFDLY[5:0] = '000000', then nRSTO_A/nRSTO_P will be asserted LOW as soon as EN has experienced a valid H-to-L transition (i.e., after ENDBNF delay) during run time.

The STRTOK bit does not have a corresponding OFFDLY[5:0] and will be cleared with no delay when the turn-off sequence is initiated.

2.6.3.3 Turn-off Sequence Timing Diagram

The timing diagram below exemplifies the turn-off sequence. Reg1 to RegN are generic regulators (Buck1-Buck8, LDO1-LDO4, LDO Controller).

All OFF delays (programmed by the OFFDLY[5:0] bits of each regulator and nRSTO_P/_A) are counted starting from the same time instant (tENDBNF after the EN H-to-L edge, which marks the beginning of the turn-off sequence).

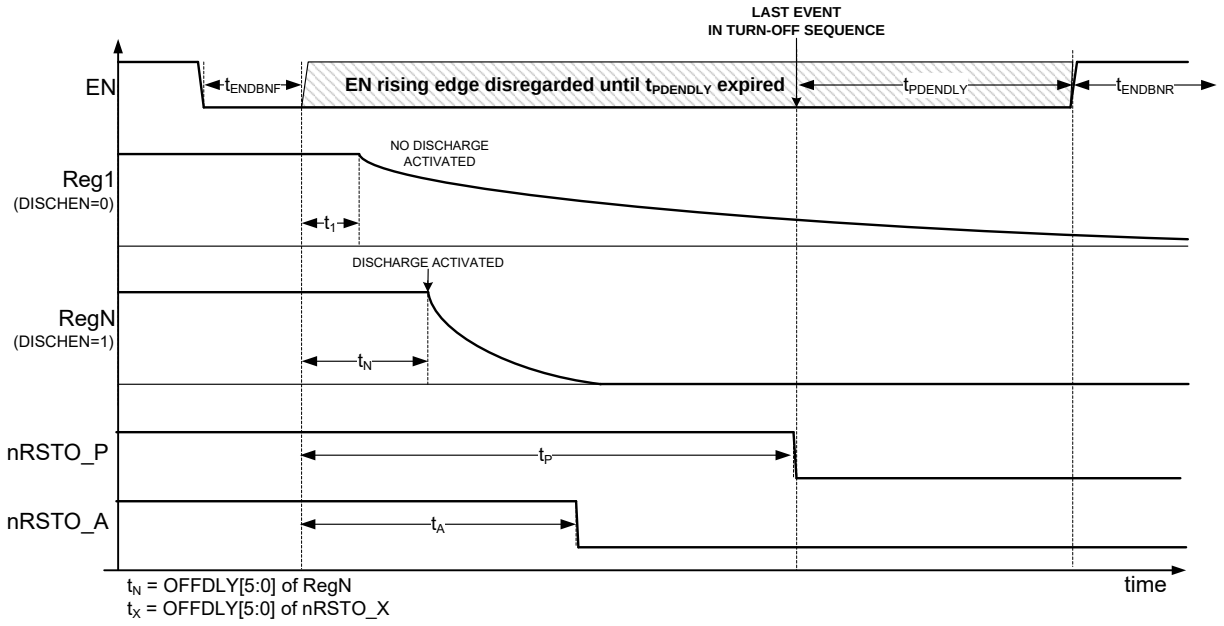
In the example below, the last event in the turn-off sequence is the Immediate OFF of RegN.

Additional information about OFFDLY[5:0] can be found in Turn-Off Sequence Step Delay Bits OFFDLY[5:0].

From the beginning of the turn-off sequence and for the Power-Down Enable Delay tPDENDLY (programmed through the PDENDLY[2:0] bits) after the last event in the turn-off sequence, the EN L-to-H transition is not recognized.

Additional information about PDENDLY[2:0] can be found in Power-Down Delay Programming PDENDLY[2:0].

Figure 2-6. Turn-OFF Sequence Example Timing Diagram.



2.7 Configuration Bits, Register Definitions and Maps

The position of the Configuration bits in the global register maps is described in I²C Registers Maps and Bit Definitions.

2.7.1 VSET[7:0] Code Definition

For the MCP16701, the entire output voltage range is covered with only one type of Buck converter. For this reason, the output voltage range is divided into two sub-ranges featuring different resolution (12.5 mV and 25 mV steps). One full byte, VSET[7:0], is allocated for output voltage coding, as illustrated in the following table. For the VSET0 and VSET1 registers, if the value is programmed between '00000000' to '00110000', the output voltage is clamped at 0.6V. From the value of '11011000' to '11111111', the output voltage is clamped at 3.8V.

Two VSET[7:0] bytes are available for each:

- VSET0[7:0]: voltage setting when mode = '0'
- VSET1[7:0]: voltage setting when mode = '1'

If VSET0[7:0] is different from the VSET1[7:0] setting, the voltage will change from one level to the other upon a MODE bit or pin change (DVS).

The table also applies to LDOs output voltage coding.

For the LDO Controller, the output voltage range is limited to 0.6V to 1.6V with 12.5 mV resolution.

Table 2-3. Voltage Codes Definition Bits Vset [7:0]

VSET[4:0]	VSET[7:5]					
	001	010	011	100	101	110
00000	0.6	0.8	1.2	1.6	2.4	3.2
00001	0.6	0.8125	1.2125	1.625	2.425	3.225
00010	0.6	0.825	1.225	1.65	2.45	3.25
00011	0.6	0.8375	1.2375	1.675	2.475	3.275
00100	0.6	0.85	1.25	1.7	2.5	3.3
00101	0.6	0.8625	1.2625	1.725	2.525	3.325
00110	0.6	0.875	1.275	1.75	2.55	3.35
00111	0.6	0.8875	1.2875	1.775	2.575	3.375
01000	0.6	0.9	1.3	1.8	2.6	3.4
01001	0.6	0.9125	1.3125	1.825	2.625	3.425
01010	0.6	0.925	1.325	1.85	2.65	3.45
01011	0.6	0.9375	1.3375	1.875	2.675	3.475
01100	0.6	0.95	1.35	1.9	2.7	3.5
01101	0.6	0.9625	1.3625	1.925	2.725	3.525
01110	0.6	0.975	1.375	1.95	2.75	3.55
01111	0.6	0.9875	1.3875	1.975	2.775	3.575
10000	0.6	1	1.4	2	2.8	3.6
10001	0.6125	1.0125	1.4125	2.025	2.825	3.625
10010	0.625	1.025	1.425	2.05	2.85	3.65
10011	0.6375	1.0375	1.4375	2.075	2.875	3.675
10100	0.65	1.05	1.45	2.1	2.9	3.7
10101	0.6625	1.0625	1.4625	2.125	2.925	3.725
10110	0.675	1.075	1.475	2.15	2.95	3.75
10111	0.6875	1.0875	1.4875	2.175	2.975	3.775
11000	0.7	1.1	1.5	2.2	3	3.8

Table 2-3. Voltage Codes Definition Bits Vset [7:0] (continued)

VSET[4:0]	VSET[7:5]					
	001	010	011	100	101	110
11001	0.7125	1.1125	1.5125	2.225	3.025	3.8
11010	0.725	1.125	1.525	2.25	3.05	3.8
11011	0.7375	1.1375	1.5375	2.275	3.075	3.8
11100	0.75	1.15	1.55	2.3	3.1	3.8
11101	0.7625	1.1625	1.5625	2.325	3.125	3.8
11110	0.775	1.175	1.575	2.35	3.15	3.8
11111	0.7875	1.1875	1.5875	2.375	3.175	3.8

Note 1: Truncated to 0.6V.

2: User accessible, 12.5 mV resolution (LDO Controller limited to 1.600V).

3: User accessible, 25 mV resolution.

4: Truncated to 3.800V.

2.7.2 Switching (Oscillator) Frequency Displacement Programming Bits

The frequency displacement acts on the main oscillator. The switching frequencies of all regulators and all timings are shifted accordingly.

The switching frequency can be adjusted by programing bits FSD[1:0]. Possible values are presented in the table below.

Table 2-4. Switching Frequency Displacement Bits FSD[1:0]

FSD[1:0]	Frequency Displacement
00	0%
01	0%
10	–16.50%
11	+16.50%

2.7.3 Switching (Oscillator) Phase Displacement Programming Bits

The phase displacement acts on the selected Buck regulator, shifting the switching event according.

The Switching (Oscillator) Phase can be adjusted by changing the value of bits PHASE[1:0]. Possible values are presented in the table below.

Table 2-5. Buck Clock Phase Displacement Bits Phase[1:0]

PHASE[1:0]	Phase Displacement
00	0°
01	90°
10	180°
11	270°

2.7.4 SYNCO Frequency vs. FREQOUT[2:0] Bits

When an external sync signal is applied, the frequency of the main oscillator can be still adjusted by modifying the value of bits FREQOUT[2:0]. Possible values are presented in the table below.

If bit ENSYNO = '1', the SYNCO pin will output a sub-multiple of the Buck switching frequency (nominally 2 MHz) as follows:

Table 2-6. SYNCO Frequency vs. FREQOUT[2:0] Bits

FREQOUT[2:0]	Division Factor	SYNCO Frequency	FREQOUT[2:0]	Division Factor	SYNCO Frequency
000	:1	2 MHz	100	:5	400 kHz
001	:2	1 MHz	101	:6	333 kHz
010	:3	667 kHz	110	:8 :7	250 kHz 286 kHz
011	:4	500 kHz	111	:8	250 kHz

2.7.5 SYNCO Output Phase Displacement Bits PHAOUT[1:0]

When an external sync signal is applied, the phase of the main oscillator can be still adjusted by modifying the value for bits PHAOUT[1:0]. Possible values are presented in the table below.

Table 2-7. SYNCO Output Phase Displacement Bits PHAOUT[1:0]

PHAOUT[1:0]	Phase Displacement
00	0°
01	90°
10	180°
11	270°

2.7.6 nRSTO_P / nRSTO_A Deassertion Delays Bits nRPDLY[3:0] and nRADLY[3:0]

The deassertion delays for the pins nRSTO_P/nRSTO_A can be adjusted by modifying the value for bits nRPDLY[3:0] and nRADLY[3:0]. Possible values are presented in the table below.

Table 2-8. nRSTO_P / nRSTO_A Deassertion Delays Bits nRPDLY[3:0] and nRADLY[3:0]

nRPDLY[3:0]	nRSTO_P Deassertion Delay (ms)	nRADLY[3:0]	nRSTO_A Deassertion Delay (ms)
0000	0	0000	0
0001	0.25	0001	0.25
0010	0.5	0010	0.5
0011	0.75	0011	0.75
0100	1	0100	1
0101	1.5	0101	1.5
0110	2	0110	2
0111	3	0111	3
1000	4	1000	4
1001	5	1001	5
1010	6	1010	6
1011	8	1011	8
1100	16	1100	16
1101	32	1101	32
1110	64	1110	64
1111	128	1111	128

2.7.7 EN Transitions Debouncing Delays Bits ENDBNR[2:0] and ENDBNF[2:0]

Bits ENDBNR[2:0] define debounce time for the L-to-H (Rising) edge (or initial H status upon AVCC and VDD UVLO release) and bits ENDBNF[2:0] define debounce time for the H-to-L (Falling) edge. Possible values are presented in the table below.

Table 2-9. EN Transitions Debouncing Delays Bits ENDBNR[2:0] and ENDBNF[2:0]

ENDBNR[2:0]	Delay (ms)	ENDBNF[2:0]	Delay (ms)
000	0	000	0
001	0.5	001	0.5
010	1	010	1
011	2	011	2
100	4	100	4
101	8	101	8
110	16	110	16
111	32	111	32

2.7.8 Turn-on Sequence Step Assignment Bits ONSEQ[1:0]

Sequence steps are defined by bits ONSEQ[1:0]. Possible values are presented in the table below.

Table 2-10. Turn-on Sequence Step Assignment Bits ONSEQ[1:0]

ONSEQ[1:0]	Turn-On Sequence Step
00	1
01	2
10	3
11	4

2.7.9 Turn-on Sequence Step Delay Bits ONDLY[3:0]

Turn-on delays within each sequence step are defined by bits ONDLY[3:0]. Possible values are presented in the table below.

Table 2-11. Turn-on Sequence Step Delay Bits ONDLY[3:0]

ONDLY[3:0]	Delay (ms)	ONDLY[3:0]	Delay (ms)
0000	0	1000	6
0001	0.5	1001	8
0010	1	1010	10
0011	1.5	1011	12
0100	2	1100	14
0101	3	1101	16
0110	4	1110	18
0111	5	1111	20

2.7.10 Turn-off Sequence Step Delay Bits OFFDLY[5:0]

All channels are turned off (upon deassertion of EN and debouncing) only based on their OFFDLY[5:0] bits. The OFFDLY[5:0] delay marks the beginning of the Immediate OFF. Possible values are presented in the table below.

Table 2-12. Turn-off Sequence Step Delay Bits OFFDLY[5:0]

OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)
000000	0	010000	8	100000	38	110000	70
000001	0.2	010001	9	100001	40	110001	72
000010	0.4	010010	10	100010	42	110010	74
000011	0.6	010011	12	100011	44	110011	76
000100	0.8	010100	14	100100	46	110100	78
000101	1	010101	16	100101	48	110101	80

Table 2-12. Turn-off Sequence Step Delay Bits OFFDLY[5:0] (continued)

OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)	OFFDLY[5:0]	Delay (ms)
000110	1.5	010110	18	100110	50	110110	82
000111	2	010111	20	100111	52	110111	84
001000	2.5	011000	22	101000	54	111000	86
001001	3	011001	24	101001	56	111001	88
001010	3.5	011010	26	101010	58	111010	90
001011	4	011011	28	101011	60	111011	92
001100	4.5	11100	30	101100	62	111100	94
001101	5	011101	32	101101	64	111101	96
001110	6	011110	34	101110	66	111110	98
001111	7	011111	36	101111	68	111111	100

2.7.11 Power-down Delay Programming Bits PDENDLY[2:0]

During the execution of the turn-off sequence, and for a programmable delay set by the PDENDLY[2:0] bits listed in the table below, the EN pin is masked and any L-to-H transition will be ignored until the PDENDLY[2:0] delay has expired. Possible values are presented in the table below.

Table 2-13. Power-down Delay Programming Bits PDENDLY[2:0]

PDENDLY[2:0]	Power-Down Delay	PDENDLY[2:0]	Power-Down Delay
000	0 ms (no PD delay)	100	4 ms
001	0.5 ms	101	6 ms
010	1 ms	110	8 ms
011	2 ms	111	10 ms

2.7.12 Soft-start Rates Programming Bits ONSR[2:0]

Soft-start rate is programmable through bits ONSR[2:0]. Possible values are presented in the table below:

Table 2-14. Soft-start Rates Programming Bits ONSR[2:0]

ONSR[2:0]	tstep @ Vstep = 25 mV (µs)	tstep @ Vstep = 12.5 mV (µs)	Ramp Rate (V/ms)
000	4	2	6.25
001	8	4	3.125
010	16	8	1.562
011	32	16	0.781
100	64	32	0.390
101	128	64	0.195
110	256	128	0.097
111	512	256	0.048

2.7.13 DVS Rate Programming Bits DVSSR[1:0]

The DVS rate is programmable through bits DVSSR[1:0]. The same rate applies to both positive and negative DVS transitions and its programmability is shown in the following table.

Table 2-15. DVS Rate Programming Bits DVSSR[1:0]

DVSSR[1:0]	tstep @ Vstep = 25 mV (µs)	tstep @ Vstep = 12.5 mV (µs)	Ramp Rate (V/ms)
00	2	1	12.5
01	4	2	6.25

Table 2-15. DVS Rate Programming Bits DVSSR[1:0] (continued)

DVSSR[1:0]	tstep @ Vstep = 25 mV (µs)	tstep @ Vstep = 12.5 mV (µs)	Ramp Rate (V/ms)
10	8	4	3.125
11	16	8	1.562

2.8 I²C Registers Maps and Bit Definitions

The MCP16701 has two types of memory:

- An embedded EEPROM for default power-up configuration programming. This non-volatile memory is typically written by the end user at the time of project manufacturing and prior to powering up the entire application. The purpose of EEPROM programming is to configure the hardware and initial default settings. The Configuration bits accessible are stored from address 0x010 to 0x084.
- A volatile register array into which the relevant EEPROM content is copied upon POR. These bits can be changed through the I²C interface. Unless otherwise noted, the bit values in volatile registers control the device configuration. Changes to the volatile registers are lost when VDD drops below the lower UVLO threshold, and the default configuration stored in EEPROM will be reloaded upon the next POR.

The volatile addresses are located in the upper portion of the address space, from 0x200 to 0x3FF.

The copy of the EEPROM Configuration bits from address 0x010 to 0x084 is made in the volatile addresses 0x210 to 0x284.

2.8.1 NVM Registers Map (see NVM Registers)

Where available, click on the address to see the register.

Table 2-16. OTP NVM Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
DEVICE ADDRESS and DEVICE ID										
ADDR	0x000	**NAME**	**Reserved**	**ADR[6]**	**ADR[5]**	**ADR[4]**	**ADR[3]**	**ADR[2]**	**ADR[1]**	**ADR[0]**
		DEFAULT	R-0	R-1	R-0	R-1	R-1	R-0	R-1	R-1
ID	0x001	**NAME**	**ID[3]**	**ID[2]**	**ID[1]**	**ID[0]**	**REV[3]**	**REV[2]**	**REV[1]**	**REV[0]**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend:
R = READ access only: **Do not overwrite!**
R/W = READ/WRITE access
-0/-1 = Factory default values.

Table 2-17. EEPROM NVM Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
SYSTEM										
SYSCFG	0x010	**NAME**	**TSDMSK**	**TWRMSK**	**TWRTH**	**Reserved**	**PDENDLY[2]**	**PDENDLY[1]**	**PDENDLY[0]**	**INVMODEP**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCCFG	0x011	**NAME**	**ENSYNO**	**FREQOUT[2]**	**FREQOUT[1]**	**FREQOUT[0]**	**PHAOUT[1]**	**PHAOUT[0]**	**FSD[1]**	**FSD[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ENDBN	0x012	**NAME**	**Reserved**	**ENDBNR[2]**	**ENDBNR[1]**	**ENDBNR[0]**	**Reserved**	**ENDBNF[2]**	**ENDBNF[1]**	**ENDBNF[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

Table 2-17. EEPROM NVM Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
VMONDBN	0x013	NAME	Reserved	Reserved	OVDBN[1]	OVDBN[0]	Reserved	Reserved	UVDBN[1]	UVDBN[0]
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
WATCHDOG CONFIGURATION										
WDCFG1	0x014	NAME	WDEN	WDMODE	WDRPEN	WDWNDW	WDI_DIS	WDT_DIS	WDRSP[1]	WDRSP[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WDCFG2	0x015	NAME	Reserved	WDTOD[2]	WDTOD[1]	WDTOD[0]	WD_CNT_MAX[3]	WD_CNT_MAX[2]	WD_CNT_MAX[1]	WD_CNT_MAX[0]
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

Table 2-18. Buck Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
BUCK1										
B1CFG1	0x019	NAME	MR	ENRSSH	MODEPMSK	MODEB	DISFRQDIV	DISMODE1	DISMODE0	ENABLE
		DEFAULT	R-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1CFG2	0x01A	NAME	ENRSRFLT	DISRSTFLT	DISINTFLT	Reserved	Reserved	DISHCP	Reserved	Reserved
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B1CFG3	0x01B	NAME	DIS100D	SLPSEL[1]	SLPSEL[0]	ENVMON	OVTH[1]	OVTH[0]	UVTH[1]	UVTH[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1ON	0x01C	NAME	PHASE[1]	PHASE[0]	ONSEQ[1]	ONSEQ[0]	ONDLY[3]	ONDLY[2]	ONDLY[1]	ONDLY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1OFF	0x01D	NAME	Reserved	DISCHEN	OFFDLY[5]	OFFDLY[4]	OFFDLY[3]	OFFDLY[2]	OFFDLY[1]	OFFDLY[0]
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1SR	0x01E	NAME	ONSR[2]	ONSR[1]	ONSR[0]	Reserved	Reserved	Reserved	DVSSR[1]	DVSSR[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B1VSET0	0x01F	NAME	VSET0[7]	VSET0[6]	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1VSET1	0x020	NAME	VSET1[7]	VSET1[6]	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK2										
B2CFG1	0x021	NAME	Mr	ENRSSH	MODEPMSK	MODEB	DISFRQDIV	DISMODE1	DISMODE0	ENABLE
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2CFG2	0x022	NAME	ENRSRFLT	DISRSTFLT	DISINTFLT	Reserved	Reserved	DISHCP	Reserved	Reserved
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B2CFG3	0x023	NAME	DIS100D	SLPSEL[1]	SLPSEL[0]	ENVMON	OVTH[1]	OVTH[0]	UVTH[1]	UVTH[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2ON	0x024	NAME	PHASE[1]	PHASE[0]	ONSEQ[1]	ONSEQ[0]	ONDLY[3]	ONDLY[2]	ONDLY[1]	ONDLY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2OFF	0x025	NAME	Reserved	DISCHEN	OFFDLY[5]	OFFDLY[4]	OFFDLY[3]	OFFDLY[2]	OFFDLY[1]	OFFDLY[0]
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2SR	0x026	NAME	ONSR[2]	ONSR[1]	ONSR[0]	Reserved	Reserved	Reserved	DVSSR[1]	DVSSR[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B2VSET0	0x027	NAME	VSET0[7]	VSET0[6]	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-18. Buck Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
B2VSET1	0x028	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK3										
B3CFG1	0x029	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3CFG2	0x02A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B3CFG3	0x02B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3ON	0x02C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3OFF	0x02D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3SR	0x02E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B3VSET0	0x02F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3VSET1	0x030	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK4										
B4CFG1	0x031	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4CFG2	0x032	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B4CFG3	0x033	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4ON	0x034	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4OFF	0x035	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4SR	0x036	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B4VSET0	0x037	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4VSET1	0x038	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK5										
B5CFG1	0x039	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5CFG2	0x03A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B5CFG3	0x03B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-18. Buck Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
B5ON	0x03C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5OFF	0x03D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5SR	0x03E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B5VSET0	0x03F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5VSET1	0x040	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK6										
B6CFG1	0x041	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6CFG2	0x042	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B6CFG3	0x043	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6ON	0x044	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6OFF	0x045	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6SR	0x046	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B6VSET0	0x047	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6VSET1	0x048	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK7										
B7CFG1	0x049	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7CFG2	0x04A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B7CFG3	0x04B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7ON	0x04C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7OFF	0x04D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7SR	0x04E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B7VSET0	0x04F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7VSET1	0x050	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-18. Buck Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
BUCK8										
B8CFG1	0x051	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8CFG2	0x052	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-0	R-0	R-0
B8CFG3	0x053	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8ON	0x054	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8OFF	0x055	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8SR	0x056	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B8VSET0	0x057	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8VSET1	0x058	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-19. LDO Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
LDO1										
L1CFG1	0x059	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0
L1CFG2	0x05A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L1ON	0x05B	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1OFF	0x05C	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1SR	0x05D	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L1VSET0	0x05E	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1VSET1	0x05F	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO2										
L2CFG1	0x060	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0
L2CFG2	0x061	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L2ON	0x062	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L2OFF	0x063	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-19. LDO Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
L2SR	0x064	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L2VSET0	0x065	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L2VSET1	0x066	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO3										
L3CFG1	0x067	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0
L3CFG2	0x068	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L3ON	0x069	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3OFF	0x06A	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3SR	0x06B	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L3VSET0	0x06C	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3VSET1	0x06D	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO4										
L4CFG1	0x06E	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0
L4CFG2	0x06F	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L4ON	0x070	**NAME**	**FBYPM/ POLSELV**	**ENSELVL4**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4OFF	0x071	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4SR	0x072	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L4VSET0	0x073	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4VSET1	0x074	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO CONTROLLER										
LCCFG1	0x075	**NAME**	**Reserved**	**Reserved**	**MODEMPSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0
LCCFG2	0x076	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
LCON	0x077	**NAME**	**Reserved**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-19. LDO Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
LCOFF	0x078	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCSR	0x079	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
LCVSET0	0x07A	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCVSET1	0x07B	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPO OUTPUT										
GPOCFG	0x07C	**NAME**	**GPOPOL**	**Reserved**	**MODEMPSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
GPOON	0x07D	**NAME**	**Reserved**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPOOFF	0x07E	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRSTO_A, nRSTO_P CONFIGURATION REGISTERS										
nRST_P1	0x07F	**NAME**	**Buck8**	**Buck7**	**Buck6**	**Buck5**	**Buck4**	**Buck3**	**Buck2**	**Buck1**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRST_P2	0x080	**NAME**	**LDO4**	**LDO3**	**LDO2**	**LDO1**	**Reserved**	**Reserved**	**Reserved**	**LDOC**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0
nRSTXDLY	0x081	**NAME**	**nRADLY[3]**	**nRADLY[2]**	**nRADLY[1]**	**nRADLY[0]**	**nRPDLY[3]**	**nRPDLY[2]**	**nRPDLY[1]**	**nRPDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRPODLY	0x082	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRAODLY	0x083	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
USER REGISTER										
USR	0x084	**NAME**	**USR[7]**	**USR[6]**	**USR[5]**	**USR[4]**	**USR[3]**	**USR[2]**	**USR[1]**	**USR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

2.8.2 Volatile Registers Map (see Volatile Registers)

Table 2-20. Volatile Status Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
SYSTEM STATUS										
STS-SYSD	0x290	**NAME**	**nUVLO_A**	**Reserved**	**NVM_BUSY**	**NVMWRT_NOK**	**Reserved**	**Reserved**	**BOOT_DONE**	**BOOT_NOK**
		DEFAULT	R-0	R-0	R-0	R/RoR-0	R-0	R-0	R-0	R/W-0
STS-SYSA	0x291	**NAME**	**Reserved**	**Reserved**	**TSD**	**TWR**	**Reserved**	**Reserved**	**STRTFAIL**	**STRTOK**
		DEFAULT	R-0	R-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0
BUCK CHANNELS STATUS										
STS-B1F	0x2A0	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B1S	0x2A1	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 2-20. Volatile Status Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
STS-B2F	0x2A2	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B2S	0x2A3	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B3F	0x2A4	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B3S	0x2A5	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B4F	0x2A6	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B4S	0x2A7	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B5F	0x2A8	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B5S	0x2A9	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B6F	0x2AA	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B6S	0x2AB	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B7F	0x2AC	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B7S	0x2AD	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-B8F	0x2AE	**NAME**	**FAULT**	**HICCUP**	**ILIM**	**ILIMNEG**	**ZCD**	**Reserved**	**Reserved**	**VMONINT**
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R/RoR-0
STS-B8S	0x2AF	**NAME**	**Reserved**	**Reserved**	**POK**	**OV**	**UV**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
LDOs AND LDO CONTROLLER STATUS										
STS-L1F	0x2B0	**NAME**	**FAULT**	**Reserved**	**ILIM**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/RoR-0	R-0	R/RoR-0	R-0	R-0	R-0	R-0	R-0
STS-L1S	0x2B1	**NAME**	**Reserved**	**Reserved**	**POK**	**Reserved**	**Reserved**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-L2F	0x2B2	**NAME**	**FAULT**	**Reserved**	**ILIM**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/RoR-0	R-0	R/RoR-0	R-0	R-0	R-0	R-0	R-0
STS-L2S	0x2B3	**NAME**	**Reserved**	**Reserved**	**POK**	**Reserved**	**Reserved**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-L3F	0x2B4	**NAME**	**FAULT**	**Reserved**	**ILIM**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/RoR-0	R-0	R/RoR-0	R-0	R-0	R-0	R-0	R-0
STS-L3S	0x2B5	**NAME**	**Reserved**	**Reserved**	**POK**	**Reserved**	**Reserved**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-L4F	0x2B6	**NAME**	**FAULT**	**Reserved**	**ILIM**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/RoR-0	R-0	R/RoR-0	R-0	R-0	R-0	R-0	R-0

Table 2-20. Volatile Status Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
STS-L4S	0x2B7	**NAME**	**SELVL4S**	**Reserved**	**POK**	**Reserved**	**Reserved**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-LCF	0x2B8	**NAME**	**FAULT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-LCS	0x2B9	**NAME**	**Reserved**	**Reserved**	**POK**	**Reserved**	**Reserved**	**SSDONE**	**Reserved**	**ENS**
		DEFAULT	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
WATCHDOG STATUS AND CONTROL										
WD_CNT	0x2C0	**NAME**	**WD_CNT[3]**	**WD_CNT[2]**	**WD_CNT[1]**	**WD_CNT[0]**	**Reserved**	**Reserved**	**Reserved**	**WD_CLEAR**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0

Legend:

R = READ access only

R/W = READ/WRITE access

R/RoR = READ and Reset-on-Read. The READ operation also attempts to clear the bit. If the event which has set the bit is still active (e.g., a current limit event), the bit is immediately set again.

The volatile registers listed in the tables below are mirroring all the applicable NVM EEPROM registers (0x010 to 0x084). The default values of the bits are loaded from the NVM EEPROM, as follows:

Default value of BIT_NAME at POR : = value of NVM_BIT_NAME

The volatile registers can be rewritten by the user, and the volatile value ultimately takes effect on the PMIC.

As noted for each of those in the previous tables, some special NVM bits do not have corresponding volatile bits.

Table 2-21. Volatile Configuration Registers Map

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
SYSTEM (VOLATILE)										
SYSCFG	0x210	**NAME**	**TSDMSK**	**TWRMSK**	**TWRTH**	**Reserved**	**PDENDLY[2]**	**PDENDLY[1]**	**PDENDLY[0]**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0
OSCCFG	0x211	**NAME**	**ENSYNO**	**FREQOUT[2]**	**FREQOUT[1]**	**FREQOUT[0]**	**PHAOUT[1]**	**PHAOUT[0]**	**FSD[1]**	**FSD[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ENDBN	0x212	**NAME**	**Reserved**	**ENDBNR[2]**	**ENDBNR[1]**	**ENDBNR[0]**	**Reserved**	**ENDBNF[2]**	**ENDBNF[1]**	**ENDBNF[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
VMONDBN	0x213	**NAME**	**Reserved**	**Reserved**	**OVDBN[1]**	**OVDBN[0]**	**Reserved**	**Reserved**	**UVDBN[1]**	**UVDBN[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
WATCHDOG CONFIGURATION (VOLATILE)										
WDCFG1	0x214	**NAME**	**WDEN**	**Reserved**	**WDRPEN**	**WDWNDW**	**WDI_DIS**	**WDT_DIS**	**WDRSP[1]**	**WDRSP[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WDCFG2	0x215	**NAME**	**Reserved**	**WDTOD[2]**	**WDTOD[1]**	**WDTOD[0]**	**WD_CNT_-MAX[3]**	**WD_CNT_-MAX[2]**	**WD_CNT_-MAX[1]**	**WD_CNT_-MAX[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
BUCK1 (VOLATILE)										
B1CFG1	0x219	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1CFG2	0x21A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B1CFG3	0x21B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
B1ON	0x21C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1OFF	0x21D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1SR	0x21E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B1VSET0	0x21F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B1VSET1	0x220	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK2 (VOLATILE)										
B2CFG1	0x221	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2CFG2	0x222	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B2CFG3	0x223	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2ON	0x224	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2OFF	0x225	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2SR	0x226	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B2VSET0	0x227	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B2VSET1	0x228	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK3 (VOLATILE)										
B3CFG1	0x229	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3CFG2	0x22A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B3CFG3	0x22B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3ON	0x22C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3OFF	0x22D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3SR	0x22E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B3VSET0	0x22F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B3VSET1	0x230	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
BUCK4 (VOLATILE)										
B4CFG1	0x231	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4CFG2	0x232	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B4CFG3	0x233	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4ON	0x234	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4OFF	0x235	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4SR	0x236	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B4VSET0	0x237	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B4VSET1	0x238	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK5 (VOLATILE)										
B5CFG1	0x239	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5CFG2	0x23A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B5CFG3	0x23B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5ON	0x23C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5OFF	0x23D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5SR	0x23E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B5VSET0	0x23F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5VSET1	0x240	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK6 (VOLATILE)										
B6CFG1	0x241	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6CFG2	0x242	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
B6CFG3	0x243	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6ON	0x244	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
B6OFF	0x245	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6SR	0x246	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B6VSET0	0x247	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B6VSET1	0x248	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK7 (VOLATILE)										
B7CFG1	0x249	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7CFG2	0x24A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B7CFG3	0x24B	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7ON	0x24C	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7OFF	0x24D	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7SR	0x24E	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B7VSET0	0x24F	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B7VSET1	0x250	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUCK8 (VOLATILE)										
B8CFG1	0x251	**NAME**	**Mr**	**ENRSSH**	**MODEPMSK**	**MODEB**	**DISFRQDIV**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8CFG2	0x252	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**DISHCP**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R-0	R-0
B8CFG3	0x253	**NAME**	**DIS100D**	**SLPSEL[1]**	**SLPSEL[0]**	**ENVMON**	**OVTH[1]**	**OVTH[0]**	**UVTH[1]**	**UVTH[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8ON	0x254	**NAME**	**PHASE[1]**	**PHASE[0]**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8OFF	0x255	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8SR	0x256	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
B8VSET0	0x257	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B8VSET1	0x258	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO1 (VOLATILE)										

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
L1CFG1	0x259	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
L1CFG2	0x25A	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L1ON	0x25B	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1OFF	0x25C	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1SR	0x25D	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L1VSET0	0x25E	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L1VSET1	0x25F	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO2 (VOLATILE)										
L2CFG1	0x260	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
L2CFG2	0x261	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L2ON	0x262	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L2OFF	0x263	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L2SR	0x264	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L2VSET0	0x265	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L2VSET1	0x266	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO3 (VOLATILE)										
L3CFG1	0x267	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
L3CFG2	0x268	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L3ON	0x269	**NAME**	**FBYPM**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3OFF	0x26A	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3SR	0x26B	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L3VSET0	0x26C	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L3VSET1	0x26D	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
LDO4 (VOLATILE)										
L4CFG1	0x26E	**NAME**	**Reserved**	**Reserved**	**MODEPMSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
L4CFG2	0x26F	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
L4ON	0x270	**NAME**	**FBYPM/ POLSELV**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4OFF	0x271	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4SR	0x272	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
L4VSET0	0x273	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
L4VSET1	0x274	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO CONTROLLER (VOLATILE)										
LCCFG1	0x275	**NAME**	**Reserved**	**Reserved**	**MODEMPSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
LCCFG2	0x276	**NAME**	**ENRSRFLT**	**DISRSTFLT**	**DISINTFLT**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0
LCON	0x277	**NAME**	**Reserved**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCOFF	0x278	**NAME**	**Reserved**	**DISCHEN**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCSR	0x279	**NAME**	**ONSR[2]**	**ONSR[1]**	**ONSR[0]**	**Reserved**	**Reserved**	**Reserved**	**DVSSR[1]**	**DVSSR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0
LCVSET0	0x27A	**NAME**	**VSET0[7]**	**VSET0[6]**	**VSET0[5]**	**VSET0[4]**	**VSET0[3]**	**VSET0[2]**	**VSET0[1]**	**VSET0[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCVSET1	0x27B	**NAME**	**VSET1[7]**	**VSET1[6]**	**VSET1[5]**	**VSET1[4]**	**VSET1[3]**	**VSET1[2]**	**VSET1[1]**	**VSET1[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPO OUTPUT (VOLATILE)										
GPOCFG	0x27C	**NAME**	**GPOPOL**	**Reserved**	**MODEMPSK**	**MODEB**	**Reserved**	**DISMODE1**	**DISMODE0**	**ENABLE**
		DEFAULT	R/W-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
GPOON	0x27D	**NAME**	**Reserved**	**Reserved**	**ONSEQ[1]**	**ONSEQ[0]**	**ONDLY[3]**	**ONDLY[2]**	**ONDLY[1]**	**ONDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPOOFF	0x27E	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRSTO_A, nRSTO_P CONFIGURATION REGISTERS (VOLATILE)										
nRST_P1	0x27F	**NAME**	**Buck8**	**Buck7**	**Buck6**	**Buck5**	**Buck4**	**Buck3**	**Buck2**	**Buck1**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRST_P2	0x280	**NAME**	**LDO4**	**LDO3**	**LDO2**	**LDO1**	**Reserved**	**Reserved**	**Reserved**	**LDOC**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R/W-0

Table 2-21. Volatile Configuration Registers Map (continued)

Register Name	Address	—	B7	B6	B5	B4	B3	B2	B1	B0
nRSTXDLY	0x281	**NAME**	**nRADLY[3]**	**nRADLY[2]**	**nRADLY[1]**	**nRADLY[0]**	**nRPDLY[3]**	**nRPDLY[2]**	**nRPDLY[1]**	**nRPDLY[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRPODLY	0x282	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
nRAODLY	0x283	**NAME**	**Reserved**	**Reserved**	**OFFDLY[5]**	**OFFDLY[4]**	**OFFDLY[3]**	**OFFDLY[2]**	**OFFDLY[1]**	**OFFDLY[0]**
		DEFAULT	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
USER REGISTER (VOLATILE)										
USR	0x284	**NAME**	**USR[7]**	**USR[6]**	**USR[5]**	**USR[4]**	**USR[3]**	**USR[2]**	**USR[1]**	**USR[0]**
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

2.9 I²C Registers

Click on the register address to see its map.

2.9.1 NVM REGISTERS (See NVM Registers Map)

Register 1: SYSCFG (Address 0x010)

Bit	7	6	5	4	3	2	1	0
	TSDMSK	TWRMSK	TWRTH	—	PDENDLY[2:0]			INVMODEP
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **TSDMSK** Thermal Shutdown nINTO Assertion Masking bit.

Bit 6 – **TWRMSK** Thermal Early Warning nINTO Assertion Masking bit.

Bit 5 – **TWRTH** Thermal Early Warning Threshold Programming bit.

Bit 4 – **Reserved**

Bit 3:1 – **PDENDLY[2:0]** EN Inhibit Delay After Power-Down Programming bits.

Bit 0 – **INVMODEP** Invert MODE Pin bit. INVMODEP determines the polarity inversion of the MODE pin. Setting INVMODEP = '1' determines polarity inversion for MODE pin. **NVM bit ONLY.**

Register 2: OSCCFG (Address 0x011)

Bit	7	6	5	4	3	2	1	0
	ENSYNO	FREQOUT[2:0]			PHAOUT[1:0]		FSD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **ENSYNO** Enable Synchronization Output.

Bit 6:4 – **FREQOUT[2:0]** SYNCO Frequency Division programming.

Bit 3:2 – **PHAOUT[1:0]** SYNCO Output Phase Alignment programming.

Bit 1:0 – **FSD[1:0]** Free-Running Switching Frequency Displacement Programming bits.

Register 3: ENDBN (Address 0x012)

Bit	7	6	5	4	3	2	1	0
	—	ENDBNR[2:0]			—	ENDBNF[2:0]		
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **Reserved**

Bit 6:4 – **ENDBNR[2:0]** EN Rising Edge Debounce Delay bits.

Bit 3 – **Reserved**

Bit 2:0 – **ENDBNR[2:0]** EN Falling Edge Debounce Delay bits.

Register 4: VMONDBN (Address 0x013)

Bit	7	6	5	4	3	2	1	0
	—	—	OVDBN[1:0]		—	—	UVDBN[1:0]	
Read/Write	R	R	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5:4 – **OVDBN[1:0]** Output Voltage Monitor OV Debounce Delay Programming bits. Affects all channels having ENVMON = '1'

Bit 3:2 – **Reserved**

Bit 1:0 – **UVDBN[1:0]** Output Voltage Monitor UV Debounce Delay Programming bits. Affects all channels having ENVMON = '1'

Register 5: WDCFG1 (Address 0x014)

Bit	7	6	5	4	3	2	1	0
	WDEN	WDMODE	WDRPEN	WDWNDW	WDI_DIS	WDT_DIS	WDRSP[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **WDEN** Watchdog Enable bit. WDEN = '0' – Watchdog disabled; WDEN = '1' – enabled.

Bit 6 – **WDMODE** Watchdog Mode Selection bit. WDMODE = '0' – WDI/nWDO Watchdog; WDMODE = '1'– interface cleared watchdog. **NVM bit ONLY.**

Bit 5 – **WDRPEN** Watchdog Enable on nRSTO_P. WDRPEN = '0' – enabled upon nRSTO_A deassertion, WDRPEN = '1' – enabled upon nRSTO_P deassertion. Applies to both watchdog modes.

Bit 4 – **WDWNDW** Watchdog Windowing bit. WDWNDW = '0' – watchdog is not windowed, WDWNDW = '1' – windowed watchdog. Applies to both watchdog modes.

Bit 3 – **WDI_DIS** WDI Count Disable. Applies to WDMODE = '1' only. If WDI_DIS = '1', the WD_CNT[3:0] counter will not be incremented on WDI HIGH-to-LOW transitions.

Bit 2 – **WDT_DIS** WD Timeout Count Disable. Applies to WDMODE = '1' only. If WDT_DIS = '1', the WD_CNT[3:0] counter will not be incremented on Watchdog Timer time-out.

Bit 1:0 – **WDRSP[1:0]** Watchdog Output Pulse Width Selection bits. Applicable only for WDMODE = '0'.

Register 6: WDCFG2 (Address 0x015)

Bit	7	6	5	4	3	2	1	0
	—	WDTOD[2:0]			WD_CNT_MAX[3:0]			
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	1

Bit 7 – **Reserved**

Bit 6:4 – **WDTOD[2:0]** Watchdog Time-Out Delay Selection bits. Applies to both watchdog modes.

Bit 3:0 – **WD_CNT_MAX[3:0]** Watchdog time-outs counter maximum. When the WD_CNT[3:0] counter content becomes greater than or equal to WD_CNT_MAX[3:0], a watchdog event is declared, and the device initiates a hardware reset and restart procedure. Applicable only for WDMODE = '1'.

Register 7: B#CFG1 (Address 0x019, 0x021, 0x029, 0x031, 0x039, 0x041, 0x049, 0x051)

Bit	7	6	5	4	3	2	1	0
	Mr	ENRSSH	MODEPMSK	MODEB	DISFRQDIV	DISMODE1	DISMODE0	ENABLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1/0	0	0	0	0	0	0	0

Bit 7 – **Mr** MAIN/Replica Configuration bit. Mr = '1' – MAIN; Mr = '0' – replica. For Buck1 and Buck5, this bit is always hardcoded as '1' and cannot be changed by the user. A power cycle is required after setting Mr = '1' in order for the setting to be applied.

Bit 6 – **ENRSSH** Enable Replica Stage Shedding bit. This bit is only relevant if Mr = '0'. This bit is used in combination with bit Mr and ENABLE to enable individual replica channel turn-off (stage shedding). If ENRSSH = '0', the replica channel follows the MAIN channel regardless of everything. If ENRSSH = '1', the replica channel can be individually disabled/enabled using the ENABLE bit. This bit is read-only for Buck1 and Buck5, as these cannot be replicas.

Bit 5 – **MODEPMSK** MODE Pin Masking bit. This bit is used in combination with bit MODEB to enforce a certain operation mode of the channel, regardless of the MODE pin. MODEPMSK = '0' – MODE pin is not masked; MODEPMSK = '1' – MODE pin is masked. Only relevant if Mr = '1'.

Bit 4 – **MODEB** MODE bit. This bit is only relevant if Mr = '1' and MODEMSK = '1'. If MODEMSK = '1', then the MODE pin is irrelevant and the value of bit MODEB applies. For example, if MODEMSK = '1' and MODEB = '1', the Buck channel will always run in FPWM, regardless of the MODE pin setting. If MODEMSK = '1' and MODEB = '0', the Buck channel will always run in AutoPFM, regardless of the MODE pin setting. Only relevant if Mr = '1'.

Bit 3 – **DISFRQDIV** Disable Frequency Division bit. Used to disable the frequency division algorithm in AutoPFM (mode = '0'). Can be used to further reduce output voltage ripple in AutoPFM, at the expense of lower light-load efficiency. Only relevant if Mr = '1'.

Bit 2 – **DISMODE1** Disable bit for mode = '1'. Used in conjunction with the ENABLE bit. If ENABLE = '1' and DISMODE1='1', the Buck channel will be disabled when mode = '1'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE1. Only relevant if Mr = '1'.

Bit 1 – **DISMODE0** Disable bit for mode = '0'. Used in conjunction with the ENABLE bit. If ENABLE = '1' and DISMODE0 = '1', the Buck channel will be disabled when mode = '0'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE0. Only relevant if Mr = '1'.

Bit 0 – **ENABLE** ENABLE bit. ENABLE = '0' means the Buck is not activated during the start-up sequence, and it will not determine the generation of nRSTO_A or nRSTO_P regardless of its definition. If ENABLE = '0', to turn the channel ON during operation, it is necessary to set the corresponding ENABLE bit in the corresponding volatile shadow register. ENABLE = '0' will also cause DISMODE0 and DISMODE1 to appear as '1' for the enable logic. If Mr = '0' and ENRSSH = '1' and ENABLE = '0', the channel is defined as a replica but remains OFF, even if its MAIN is ON. To enable it, it is necessary to set the corresponding ENABLE bit in the corresponding volatile shadow register.

Register 8: B#CFG2 (Address 0x01A, 0x022, 0x02A, 0x032, 0x03A, 0x042, 0x04A, 0x052)

Bit	7	6	5	4	3	2	1	0
	ENRSRFLT	DISRSTFLT	DISINTFLT	—	—	DISHCP	—	—
Read/Write	R/W	R/W	R/W	R	R	R/W	R	R
Initial Value	0	0	0	1	1	0	0	0

Bit 7 – **ENRSRFLT** Enable Restart on FAULT bit. If ENRSRFLT = '1', a FAULT on the channel will invoke an automatic restart sequence after a 100 ms delay. **This bit should be set only if the channel is used to generate some special rails (such as VDD1 of LPDDRx) whose failure can endanger the load if other channels continue operating. Only relevant if Mr = '1'.**

Bit 6 – **DISRSTFLT** Disable Reset on FAULT bit. For a channel having ENABLE = '1', this bit disables automatic nRSTO_A and/or nRSTO_P deassertion upon a channel FAULT during run time. If a channel with ENABLE = '0' is turned on through the interface after the assertion of nRSTO_A and nRSTO_P, it is also necessary to set the corresponding volatile shadow bit DISRSTFLT in order to prevent the deassertion of nRSTO_A and nRSTO_P upon a FAULT.

Bit 5 – **DISINTFLT** Disable Interrupt on FAULT bit. This bit disables automatic nINTO assertion upon channel FAULT during run time. Only relevant if Mr = '1'.

Bit 4:3 – **Reserved**

Bit 2 – **DISHCP** Disable bit for hiccup mode overcurrent protection. If DISHCP = '1' the converter will only operate with cycle-by-cycle current limit protection. Only relevant if Mr = '1'. It is strongly recommend that the DISHCP bit is set to 0 (Hiccup mode overcurrent protection enable).

Bit 1:0 – **Reserved**

Register 9: B#CFG3 (Address 0x01B, 0x023, 0x02B, 0x033, 0x03B, 0x043, 0x04B, 0x053)

Bit	7	6	5	4	3	2	1	0
	DIS100D	SLPSEL[1:0]		ENVMON	OVTH[1]	OVTH[0]	UVTH[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **DIS100D** Disables 100% duty cycle capability. Duty cycle will be limited to 75%. Only relevant if Mr = '1'.

Bit 6:5 – **SLPSEL[1:0]** Slope Compensation Selection bits. Only relevant if Mr = '1'.

Bit 4 – **ENVMON** Enable Voltage Monitor. If ENVMON = '0', the OV/UV output voltage monitor is disabled and the OV/UV bits will be '0'. If ENVMON = '1' and DISINTFLT = '0', an interrupt will be generated (nINTO asserted LOW and the VMONINT bit set to '1') when an OV or UV condition is detected in steady-state operation. If ENVMON = '1' and DISINTFLT = '1', OV/UV status bits will be set, but no interrupt is generated and VMONINT won't be set. Only relevant if Mr = '1'.

Bit 3 – **OVTH[1]** Overvoltage Threshold Selection bit (MSB). Only relevant if Mr = '1'.

Bit 2 – **OVTH[0]** Overvoltage Threshold Selection bit (LSB). Only relevant if Mr = '1'.

Bit 1:0 – **UVTH[1:0]** Undervoltage Threshold Selection bits. Only relevant if Mr = '1'.

Register 10: B#ON (Address 0x01C, 0x024, 0x02C, 0x034, 0x03C, 0x044, 0x04C, 0x054)

Bit	7	6	5	4	3	2	1	0
	PHASE[1:0]		ONSEQ[1:0]		ONDLY[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **PHASE[1:0]** Sets the phase displacement of the Buck converter switch turn-on edge.

Bit 5:4 – **ONSEQ[1:0]** Assigns the converter to a certain ON sequence step (0, 1, 2 or 3).

Bit 3:0 – **ONDLY[3:0]** Programs the delay between the end of the previous sequence step and the beginning of the converter turn-on (soft-start ramp).

Register 11: B#OFF (Address 0x01D, 0x025, 0x02D, 0x035, 0x03D, 0x045, 0x04D, 0x055)

Bit	7	6	5	4	3	2	1	0
	—	DISCHEN	OFFDLY[5:0]					
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **Reserved**

Bit 6 – **DISCHEN** Discharge Enable. DISCHEN = '1' enables the turn-off of the pull-down discharge resistor after the converter output has been three-stated immediately.

Bit 5:0 – **OFFDLY[5:0]** Programs the delay between the deassertion of the EN input and the beginning of the converter turn-off (tri-state).

Register 12: B#SR (Address 0x01E, 0x026, 0x02E, 0x036, 0x03E, 0x046, 0x04E, 0x056)

Bit	7	6	5	4	3	2	1	0
	ONSR[2:0]			—	—	—	DVSSR[1:0]	
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:5 – **ONSR[2:0]** Slew-rate Programming bits for soft start ramp.

Bit 4:2 – **Reserved**

Bit 1:0 – **DVSSR[1:0]** Slew-rate Programming bits for DVS transitions. Applies to both positive and negative DVS transitions.

Register 13: B#VSET0 (Address 0x01F, 0x027, 0x02F, 0x037, 0x03F, 0x047, 0x04F, 0x057)

Bit	7	6	5	4	3	2	1	0
	VSET0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET0[7:0]** VSET output voltage for mode = '0'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 14: B#VSET1 (Address 0x020, 0x028, 0x030, 0x038, 0x040, 0x048, 0x050, 0x058)

Bit	7	6	5	4	3	2	1	0
	VSET1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET1[7:0]** VSET output voltage for mode = '1'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 15: L#CFG1 (Address 0x059, 0x060, 0x067, 0x06E)

Bit	7	6	5	4	3	2	1	0
	—	—	MODEPMSK	MODEB	—	DISMODE1	DISMODE0	ENABLE
Read/Write	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	1	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **MODEPMSK** MODE Pin Masking bit. This bit is used in combination with bit MODEB to enforce a certain operation mode of the channel, regardless of the MODE pin. MODEPMSK = '0' – MODE pin is not masked; MODEPMSK = '1' – MODE pin is masked.

Bit 4 – **MODEB** MODE bit. This bit is only relevant if MODEMSK = '1'. If MODEMSK = '1', then the MODE pin is irrelevant, and the value of bit MODEB applies.

Bit 3 – **Reserved**

Bit 2 – **DISMODE1** Disable bit for mode = '1'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE1='1', the Buck channel will be disabled when mode = '1'; otherwise, it will be enabled. This is used to turn the channel ON or OFF upon “mode” change. If ENABLE = '0', the channel stays OFF regardless of DISMODE1.

Bit 1 – **DISMODE0** Disable bit for mode = '0'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE0 = '1', the Buck channel will be disabled when mode = '0'; otherwise, it will be enabled. This is used to turn the channel ON or OFF upon a “mode” change. If ENABLE = '0', the channel stays OFF regardless of DISMODE0.

Bit 0 – **ENABLE** ENABLE bit. ENABLE= '0' means the LDO is not activated during the start-up sequence, and it will not determine the generation of nRSTO_A or nRSTO_P regardless of its definition. If ENABLE = '0', to turn the channel ON during operation, it is necessary to set the corresponding ENABLE bit in the corresponding volatile shadow register. ENABLE = '0'will also cause DISMODE0 and DISMODE1 to appear as '1' for the enable logic.

Register 16: L#CFG2 (Address 0x05A, 0x061, 0x068, 0x06F)

Bit	7	6	5	4	3	2	1	0
	ENRSRFLT	DISRSTFLT	DISINTFLT	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **ENRSRFLT** Enable Restatt on FAULT bit. If ENRSRFLT = '1', a FAULT on the channel will invoke an automatic restart sequence after a 100 ms delay.

Bit 6 – **DISRSTFLT** Disable Reset on FAULT bit. For a channel having ENABLE = '1', this bit disables automatic nRSTO_A and/or nRSTO_P deassertion upon a channel FAULT during run time. If a channel having ENABLE = '0' is turned on through interface after the assertion of nRSTO_A and nRSTO_P, it is also necessary to set the corresponding volatile shadow bit DISRSTFLT in order to prevent deassertion of nRSTO_A and nRSTO_P upon FAULT.

Bit 5 – **DISINTFLT** Disable Interrupt on FAULT bit. This bit disables automatic nINTO assertion upon channel FAULT during run time.

Bit 4:0 – **Reserved**

Register 17: L#ON (Address 0x05B, 0x062, 0x069, 0x070)

Bit	7	6	5	4	3	2	1	0
	FBYPM	—	ONSEQ[1:0]		ONDLY[3:0]			
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **FBYPM** Forces LDO in Load-Switch mode.

Bit 6 – **Reserved**

Bit 5:4 – **ONSEQ[1:0]** Assigns the converter to a certain ON sequence step (0, 1, 2 or 3).

Bit 4:0 – **ONDLY[3:0]** Programs the delay between the end of the previous sequence step and the beginning of the converter turn-on (soft-start ramp).

Note: See register L4ON for bits 7 and 6 of LDO4:
Bit 7 – **FBYPM/POLSELV** Forces LDO in Load-Switch mode if bit ENSELVL4 = '0'. Selects polarity of SELVL4 logic if ENSELVL4 = '1'.

Bit 6 – **ENSELVL4** ENSELVL4 = '1' enables pin SELVL4 to control LDO4 voltage between 1.8V and 3.3V. **NVM bit ONLY.**

Register 18: L#OFF (Address 0x05C, 0x063, 0x06A, 0x071)

Bit	7	6	5	4	3	2	1	0
	—	DISCHEN	OFFDLY[5:0]					
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **Reserved**

Bit 6 – **DISCHEN** Discharge Enable. DISCHEN = '1' enables the turn-off of the pull-down discharge resistor after the converter output has been three-stated immediately.

Bit 5:0 – **OFFDLY[5:0]** Programs the delay between the deassertion of the EN input and the beginning of the converter turn-off (tri-state).

Register 19: L#SR (Address 0x05D, 0x064, 0x06B, 0x072)

Bit	7	6	5	4	3	2	1	0
	ONSR[2:0]			—	—	—	DVSSR[1:0]	
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:5 – **ONSR[2:0]** Slew-rate Programming bits for the soft-start ramp.

Bit 4:2 – **Reserved**

Bit 1:0 – **DVSSR[1:0]** Slew-rate Programming bits for DVS transitions. Applies to both positive and negative DVS transitions.

Register 20: L#VSET0 (Address 0x05E, 0x065, 0x06C, 0x073)

Bit	7	6	5	4	3	2	1	0
	VSET0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET0[7:0]** VSET output voltage for mode = '0'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 21: L#VSET1 (Address 0x05F, 0x066, 0x06D, 0x074)

Bit	7	6	5	4	3	2	1	0
	VSET1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET1[7:0]** VSET output voltage for mode = '1'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 22: LCCFG1 (Address 0x075)

Bit	7	6	5	4	3	2	1	0
	—	—	MODEPMSK	MODEB	—	DISMODE1	DISMODE0	ENABLE
Read/Write	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	1	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **MODEPMSK** MODE Pin Masking bit. This bit is used in combination with bit MODEB to enforce a certain operation mode of the channel, regardless of the MODE pin. MODEPMSK = '0' – MODE pin is not masked; MODEPMSK = '1' – MODE pin is masked.

Bit 4 – **MODEB** MODE bit. This bit is only relevant if MODEMSK = '1'. If MODEMSK = '1' then the MODE pin is irrelevant and the value of bit MODEB applies.

Bit 3 – **Reserved**

Bit 2 – **DISMODE1** Disable bit for mode = '1'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE1='1', the Buck channel will be disabled when mode = '1'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE1.

Bit 1 – **DISMODE0** Disable bit for mode = '0'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE0 = '1', the Buck channel will be disabled when mode = '0'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE0.

Bit 0 – **ENABLE** ENABLE bit. ENABLE= '0' means the LDO is not activated during the start-up sequence, and it will not determine the generation of nRSTO_A or nRSTO_P regardless of its definition. If ENABLE = '0', to turn the channel ON during operation, it is necessary to set the corresponding ENABLE bit in the corresponding volatile shadow register. ENABLE = '0' will also cause DISMODE0 and DISMODE1 to appear '1' for the enable logic.

Register 23: LCCFG2 (Address 0x076)

Bit	7	6	5	4	3	2	1	0
	ENRSRFLT	DISRSTFLT	DISINTFLT	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **ENRSRFLT** Enable Restart on FAULT bit. If ENRSRFLT = '1', a FAULT on the channel will invoke an automatic restart sequence after a 100 ms delay.

Bit 6 – **DISRSTFLT** Disable Reset on FAULT bit. For a channel having ENABLE = '1', this bit disables automatic nRSTO_A and/or nRSTO_P deassertion upon channel FAULT during run time. If a channel having ENABLE = '0' is turned on through the interface after the assertion of nRSTO_A and nRSTO_P, it is also necessary to set the corresponding volatile shadow bit DISRSTFLT in order to prevent the deassertion of nRSTO_A and nRSTO_P upon FAULT.

Bit 5 – **DISINTFLT** Disable Interrupt on FAULT bit. This bit disables automatic nINTO assertion upon channel FAULT during run time.

Bit 4:0 – **Reserved**

Register 24: LCON (Address 0x077)

Bit	7	6	5	4	3	2	1	0
	—	—	ONSEQ[1:0]		ONDLY[3:0]			
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5:4 – **ONSEQ[1:0]** Assigns the converter to a certain ON sequence step (0, 1, 2 or 3).

Bit 4:0 – **ONDLY[3:0]** Programs the delay between the end of the previous sequence step and the beginning of the converter turn-on (soft-start ramp).

Register 25: LCOFF (Address 0x078)

Bit	7	6	5	4	3	2	1	0
	—	DISCHEN	OFFDLY[5:0]					
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **Reserved**

Bit 6 – **DISCHEN** Discharge Enable. DISCHEN = '1' enables turn-off of the pull-down discharge resistor after the converter output has been three-stated immediately.

Bit 5:0 – **OFFDLY[5:0]** Programs the delay between the deassertion of the EN input and the beginning of the converter turn-off (tri-state).

Register 26: LCSR (Address 0x079)

Bit	7	6	5	4	3	2	1	0
	ONSR[2:0]			—	—	—	DVSSR[1:0]	
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:5 – **ONSR[2:0]** Slew-rate programming bits for soft-start ramp.

Bit 4:2 – **Reserved**

Bit 1:0 – **DVSSR[1:0]** Slew-rate programming bits for DVS transitions. Applies to both positive and negative DVS transitions.

Register 27: LCVSET0 (Address 0x07A)

Bit	7	6	5	4	3	2	1	0
	VSET0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET0[7:0]** VSET output voltage for mode = '0'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 28: LCVSET1 (Address 0x07B)

Bit	7	6	5	4	3	2	1	0
	VSET1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:0 – **VSET1[7:0]** VSET output voltage for mode = '1'. DVS will be executed upon mode change if VSET0[7:0] ≠ VSET1[7:0], provided that DISMODE1 = DISMODE0 = '0'.

Register 29: GPOCFG (Address 0x07C)

Bit	7	6	5	4	3	2	1	0
	GPOPOL	—	MODEPMSK	MODEB	—	DISMODE1	DISMODE0	ENABLE
Read/Write	R/W	R	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **GPOPOL** GPO Polarity Selection bit. GPOPOL = '0' – normal logic (GPO asserted = HIGH); GPOPOL = '1'–inverted logic (GPO asserted = LOW).

Bit 6 – **Reserved**

Bit 5 – **MODEPMSK** MODE Pin Masking bit. This bit is used in combination with bit MODEB to enforce a certain operation mode of the channel, regardless of the MODE pin. MODEPMSK = '0' – MODE pin is not masked; MODEPMSK = '1' – MODE pin is masked.

Bit 4 – **MODEB** MODE bit. This bit is only relevant if MODEMSK = '1'. If MODEMSK = '1' then the MODE pin is irrelevant and the value of bit MODEB applies.

Bit 3 – **Reserved**

Bit 2 – **DISMODE1** Disable bit for mode = '1'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE1='1', the Buck channel will be disabled when mode = '1'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE1.

Bit 1 – **DISMODE0** Disable bit for mode = '0'. Used in conjunction with bit ENABLE. If ENABLE = '1' and DISMODE0 = '1', the Buck channel will be disabled when mode = '0'; otherwise, it will be enabled. Used to turn the channel ON or OFF upon "mode" change. If ENABLE = '0', the channel stays OFF regardless of DISMODE0.

Bit 0 – **ENABLE** ENABLE bit. ENABLE='0' means the GPO is not activated during the start-up sequence. If ENABLE = '0', to turn the channel ON during operation, it is necessary to set the corresponding ENABLE bit in the corresponding volatile shadow register. ENABLE = '0' will also cause DISMODE0 and DISMODE1 to appear '1' for the enable logic.

Register 30: GPOON (Address 0x07D)

Bit	7	6	5	4	3	2	1	0
	—	—	ONSEQ[1:0]		ONDLY[3:0]			
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5:4 – **ONSEQ[1:0]** Assigns the GPO to a certain ON sequence step (0, 1, 2 or 3).

Bit 4:0 – **ONDLY[3:0]** Programs the delay between the end of the previous sequence step and the GPO assertion.

Register 31: GPOOFF (Address 0x07E)

Bit	7	6	5	4	3	2	1	0
	—	—	OFFDLY[5:0]					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – Reserved

Bit 5:0 – OFFDLY[5:0] Programs the delay between the deassertion of the EN input and the GPO deassertion.

Register 32: nRST_P1 (Address 0x07F)

Bit	7	6	5	4	3	2	1	0
	Buck8	Buck7	Buck6	Buck5	Buck4	Buck3	Buck2	Buck1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – Buck8 Buck8 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1' and Mr = '1'.

Bit 6 – Buck7 Buck7 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1' and Mr = '1'.

Bit 5 – Buck6 Buck6 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1' and Mr = '1'.

Bit 4 – Buck5 Buck5 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1'.

Bit 3 – Buck4 Buck4 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1'.

Bit 2 – Buck3 Buck3 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1' and Mr = '1'.

Bit 1 – Buck2 Buck2 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1' and Mr = '1'.

Bit 0 – Buck1 Buck1 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if Buck ENABLE = '1'.

Register 33: nRST_P2 (Address 0x080)

Bit	7	6	5	4	3	2	1	0
	LDO4	LDO3	LDO2	LDO1	—	—	—	LDOC
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – LDO4 LDO4 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if LDO ENABLE = '1'.

Bit 6 – LDO3 LDO3 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if LDO ENABLE = '1'.

Bit 5 – LDO2 LDO2 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if LDO ENABLE = '1'.

Bit 4 – LDO1 LDO1 = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if LDO ENABLE = '1'.

Bit 3:1 – Reserved

Bit 0 – LDOC LDOC = '1': channel taken into account in the deassertion of nRSTO_P. Only relevant if LDO Controller ENABLE = '1'.

Register 34: nRSTXDLY (Address 0x081)

Bit	7	6	5	4	3	2	1	0
	nRADLY[3:0]				nRPDLY[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:4 – **nRADLY[3:0]** nRSTO_A Reset Delay Deassertion Programming bits.

Bit 3:0 – **nRPDLY[3:0]** nRSTO_P Reset Delay Deassertion Programming bits.

Register 35: nRPODLY (Address 0x082)

Bit	7	6	5	4	3	2	1	0
	—	—	OFFDLY[5:0]					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 3:0 – **OFFDLY[5:0]** Programs the delay between the deassertion of the EN input (after debouncing) and the assertion of nRSTO_P.

Register 36: nRAODLY (Address 0x083)

Bit	7	6	5	4	3	2	1	0
	—	—	OFFDLY[5:0]					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 3:0 – **OFFDLY[5:0]** Programs the delay between the deassertion of the EN input (after debouncing) and the assertion of nRSTO_A.

2.9.2 VOLATILE REGISTERS (see Volatile Registers Map)

Register 37: STS-SYSD (Address 0x290)

Bit	7	6	5	4	3	2	1	0
	nUVLO_A	—	NVM_BUSY	NVMWRT_NOK	—	—	BOOT_DONE	BOOT_NOK
Read/Write	R	R	R	R/RoR	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **nUVLO_A** AVCC UVLO bit (inverted). If nUVLO_A is '1', then AVCC is present and within its valid range. If AVCC is not present or is outside its valid range, then nUVLO_A = '0'. If nUVLO_A = '0', all the remaining status bits in the STS-SYSA and STS-XXX registers are not valid and should be ignored.

Bit 6 – **Reserved**

Bit 5 – **NVM_BUSY** NVM Busy status during write operations. This bit goes high when the internal NVM memory is being written. It automatically goes back to '0' as soon as the NVM memory is ready to accept another write operation.

Bit 4 – **NVMWRT_NOK** NVM WRITE Not OK Flag. This bit is set whenever the WRITE operation to the internal EEPROM fails, i.e. the readback of the written value into a given EEPROM address does not match, nINTO will be asserted concurrently. Reading the register will reset the bit and cause nINTO deassertion.

Bit 3:2 – **Reserved**

Bit 1 – **BOOT_DONE** Boot DONE. This bit is '0' when the boot process is in progress, '1' otherwise.

Bit 0 – **BOOT_NOK** Boot process is NOT OK. This bit goes to '1' if the checksum calculation after boot fails. Writing a '0' to this bit while BOOT_DONE = '1' enforces a repetition of the boot process and checksum calculation.

Register 38: STS-SYSA (Address 0x291)

Bit	7	6	5	4	3	2	1	0
	—	—	TSD	TWR	—	—	STRTFAIL	STRTOK
Read/Write	R	R	R/RoR	R/RoR	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **TSD** Thermal Shutdown Flag.

Bit 4 – **TWR** Thermal Warning Flag.

Bit 3:2 – **Reserved**

Bit 1 – **STRTFAIL** Start-up FAIL. This bit becomes '1' in the event of a start-up failure (nRSTO_A fails to deassert).

Bit 0 – **STRTOK** Start-up OK. This bit becomes '1' in the event of a successful start-up (nRSTO_A has succeeded in deasserting).

Register 39: STS-B#F (Bucks Flags, Address 0x2A0, 0x2A2, 0x2A4, 0x2A6, 0x2A8, 0x2AA, 0x2AC, 0x2AE)

Bit	7	6	5	4	3	2	1	0
	FAULT	HICCUP	ILIM	ILIMNEG	ZCD	—	—	VMONINT
Read/Write	R/RoR	R/RoR	R/RoR	R/RoR	R/RoR	R	R	R/RoR
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **FAULT** FAULT flag.

Bit 6 – **HICCUP** HICCUP Fault flag.

Bit 5 – **ILIM** Current Limit Fault flag.

Bit 4 – **ILIMNEG** Negative Inductor Current Limit flag.

Bit 3 – **ZCD** Inductor Zero-Current Detection flag.

Bit 2:1 – **Reserved**

Bit 0 – **VMONINT** Voltage Monitor Interrupt flag. VMONINT is set concurrently with the nINTO assertion upon detection of OV/UV conditions in steady-state operation.

Register 40: STS-B#S (Bucks Statuses, Address 0x2A1, 0x2A3, 0x2A5, 0x2A7, 0x2A9, 0x2AB, 0x2AD, 0x2AF)

Bit	7	6	5	4	3	2	1	0
	—	—	POK	OV	UV	SSDONE	—	ENS
Read/Write	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **POK** Power OK Status bit.

Bit 4 – **OV** Overvoltage Status bit.

Bit 3 – **UV** Undervoltage Status bit.

Bit 2 – **SSDONE** SSDONE is '1' if the channel has completed the soft-start ramp.

Bit 1 – **Reserved**

Bit 0 – **ENS** Enable Status. ENS = '1' means that the channel is currently enabled.

Register 41: STS-L#F (LDOs Flags, Address 0x2B0, 0x2B2, 0x2B4, 0x2B6)

Bit	7	6	5	4	3	2	1	0
	FAULT	—	ILIM	—	—	—	—	—
Read/Write	R/RoR	R	R/RoR	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **FAULT** FAULT flag.

Bit 6 – **Reserved**

Bit 5 – **ILIM** Current Limit Fault flag.

Bit 4:0 – **Reserved**

Register 42: STS-L#S (LDOs Statuses, Address 0x2B1, 0x2B3, 0x2B5, 0x2B7)

Bit	7	6	5	4	3	2	1	0
	—	—	POK	—	—	SSDONE	—	ENS
Read/Write	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **POK** Power OK Status bit.

Bit 4:3 – **Reserved**

Bit 2 – **SSDONE** SSDONE is '1' if the channel has completed the soft-start ramp.

Bit 1 – **Reserved**

Bit 0 – **ENS** Enable Status. ENS = '1' means that the channel is currently enabled.

Note: LDO4 only:
Bit 7 – **SELVL4S** If NVM_ENSELVL4 = '1', SELVL4S represents the instantaneous logic level read on the SELVL4 pin. If NVM_ENSELVL4 = '0', this bit is always read as '0'. **Reserved** for other LDOs.

Register 43: STS-LCF (LDO Controller Flags, Address 0x2B8)

Bit	7	6	5	4	3	2	1	0
	FAULT	—	—	—	—	—	—	—
Read/Write	R/RoR	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 – **FAULT** FAULT Flag.

Bit 6:0 – **Reserved**

Register 44: STS-LCS (LDO Controller Statuses, Address 0x2B9)

Bit	7	6	5	4	3	2	1	0
	—	—	POK	—	—	SSDONE	—	ENS
Read/Write	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7:6 – **Reserved**

Bit 5 – **POK** Power OK Status bit.

Bit 4:3 – **Reserved**

Bit 2 – **SSDONE** SSDONE is '1' if the channel has completed the soft-start ramp.

Bit 1 – **Reserved**

Bit 0 – **ENS** Enable Status. ENS = '1' means that the channel is currently enabled.

Register 45: WD_CNT (Address 0x2C0)

Bit	7	6	5	4	3	2	1	0
	WD_CNT[3:0]				—	—	—	WD_CLEAR
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7:4 – WD_CNT[3:0] Watchdog timeouts and/or WDI H-to-L edges counter. Only applicable is NVM_WDMODE = '1'. If NVM_WDMODE = '0', the content will always be '0000'. When WD_CNT[3:0] becomes greater or equal to WD_CNT_MAX[3:0], a watchdog event is declared and the MCP16701 performs a full hardware reset and restart.

Bit 3:1 – Reserved

Bit 3:1 – WD_CLEAR WD_CLEAR is treated as a read-only bit when NVM_WDMODE='0'. In this case, WD_CLEAR is '1' whenever the Watchdog Timer is counting and '0' otherwise. WD_CLEAR is available a R/W bit when NVM_WDMODE = '1' and WDT_DIS = '0'. WD_CLEAR goes to '1' as soon as the internal Watchdog Timer start counting. The WD_CLEAR must be rewritten by the host as '1' within the valid time window in order to reset the internal timer. If this does not happen, the WD_CNT[3:0] gets incremented by 2. If WD_CLEAR is rewritten within the valid window, WD_CNT[3:0] gets decremented by 1.

2.10 I²C Interface Description

The MCP16701 features an I²C interface supporting the High-speed mode (Hs-mode) data transfer with a bit rate of up to 3.4 Mbit/s, as described in the official I²C standard.

The I²C interface is always accessible, even in the OFF state, as long as the VDD pin is powered and above its UVLO Threshold. AVCC UVLO is irrelevant to I²C interface operation.

2.10.1 CRC-8 Support

The I²C protocol used by MCP16701 support optional CRC-8.

The generator polynomials are listed in the following:

Equation 2-1. CRC-8-SAE J1850 polynomials:

$C(x) = x^8 + x^4 + x^3 + x^2 + 1$ **(0x1D)**, seed = 0xFF

Equation 2-2. CRC-8-CCITT (SMBus PEC):

$C(x) = x^8 + x^2 + x + 1$ **(0x07)**

CRC-8 is implemented by appending a CRC-8 Code byte at the end of each message transfer.

As each protocol transaction specifies the number of data bytes, there is no need for a specific opcode to command the transmission of the CRC-8. MCP16701 is always prepared to receive and transmit data with or without a CRC-8. CRC-8 will be received/transmitted on the bus based on subsequent SCL cycles generated by the host after the last data byte.

During a target-receive transfer, the MCP16701 will interpret the byte supplied after the last data byte as the additional CRC-8, check it for validity in real time, and provide an ACK/NACK upon CRC-8 check.

During a target-transmit transfer, the MCP16701 will respond to additional clocks after the last byte transfer and furnish a CRC-8 to the host receiver requesting it.

Therefore, each bus protocol transaction has two variants: one with the CRC-8 byte and one without.

The CRC-8 error-checking byte **is calculated on all the message bytes (including DEV_ADDR, READ/write bit, OPCODE_H, OPCODE_L, data and master code in case of Hs-mode data transfers).** The calculation does not include ACK (A) or NACK (N) bits or START (S), STOP (P) or REPEATED START(Sr) conditions. The CRC-8 is computed over the entire message **from the first START condition.**

As such, when executing data transfers in Hs-mode where the first START condition is generated before the master code is sent, the master code will be included in the CRC-8 calculation.

The master code provided by the host to initiate an Hs-mode (3.4 MHz) is never transmitted with a separated CRC-8.

2.10.2 Device Address (DEV_ADDR)

The MCP16701 uses a 7-bit address (0x5B by default). The device address is programmable as configured in a reserved NVM location.

2.10.3 Register Address and Byte Count (OPCODE_H, OPCODE_L)

Immediately after the Device Address, TWO bytes (OPCODE_H, OPCODE_L with OPCODE_H sent first) are sent to address a specific register - which may be an NVM EEPROM address - and to specify the number of bytes involved in the transaction.

The structure of OPCODE_H is as follows:

Table 2-22. OPCODE_H BYTE Structure

b7	b6	b5	b4	b3	b2	b1	b0
N5	**N4**	**N3**	**N2**	**N1**	**N0**	**A9**	**A8**

Where:

N5-N0 specify the number of bytes in the transaction (1 to 63). 0 **is not** a valid number (no data bytes will be transferred, it is not an allowed operation).

A9-A8 are the two MSBs of the 10-bit register address A9-A0 (1024 registers addresses are possible). Therefore, the overall registers' space can be split into 4 pages ('00' to '11') of 256 addresses each.

The structure of OPCODE_L is as follows:

Table 2-23. OPCODE_L BYTE Structure

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

Where:

A7-A0 are the lower 8 bits of the 10-bit register address A9-A0.

The data bytes are written/read starting from the register address specified in OPCODE_H, OPCODE_L bytes and will automatically increment by one at each subsequent data byte.

There is no address wrap-around after A9-A0 = 0x3FF. Writing beyond the last register location will have no effect. Reading beyond the last register location will stream out all '1's.

2.10.4 Block Write Transactions

The Block Write transactions (without and with CRC-8) are shown in the following figures. The diagrams assume DEV_ADDR is correct, and therefore the MCP16701 issues an ACK (A). Otherwise, a NACK(N) will be issued, and the remaining part of the transaction will be ignored.

Figure 2-7. Block Write Protocol without CRC-8 (Sr Applies to HS-Mode Transfer).

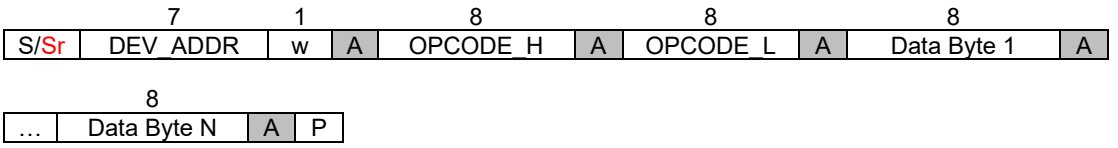
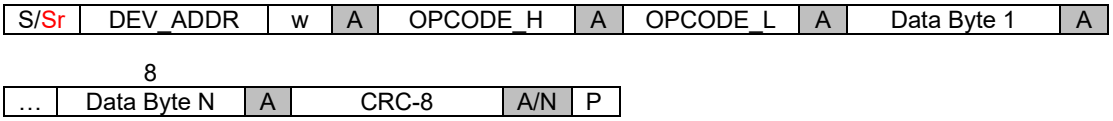


Figure 2-8. Block Write Protocol with CRC-8 (Sr Applies to HS-Mode Transfer).



As the Block Write transaction may be preceded by the master code announcing Hs-mode transfer, the first START condition will actually be a REPEATED START.

In Target-Receiver mode, the MCP16701 will issue a NACK (N) if the CRC-8 is present but not correct. The host can then decide further actions e.g. to retry transmission.

Writing to reserved and/or non-existent registers will not cause the MCP16701 to generate a NACK. An ACK will still be generated, but the written byte(s) will have no effect.

When a WRITE operation is performed to NVM registers, a password procedure to get write permission is required. See I²C Special Commands for details.

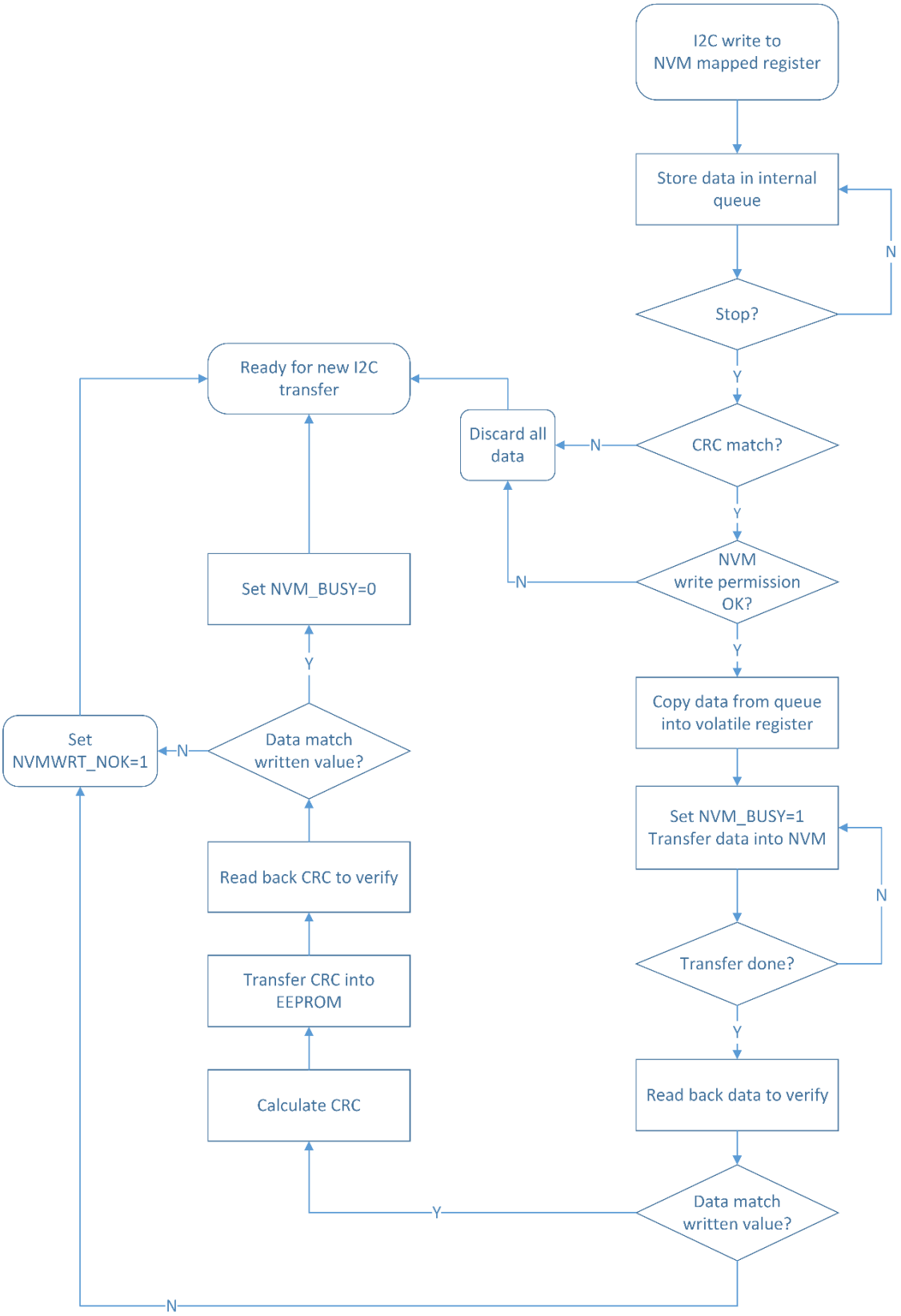
Furthermore the NVM controller also performs additional actions such as:

Setting bit NVM_BUSY in the SYS-STS register. NVM_BUSY automatically goes back to '0' as soon as the NVM memory is ready to accept another write operation.

Set NVMWRT_NOK (NVM WRITE Not OK) bit if there is a mismatch between the original data and the readback of the data just written in the EEPROM. nINTO will also be asserted concurrently. Reading the SYS-STS register will reset the NVMWRT_NOK bit and cause nINTO deassertion. Note that the EEPROM readback check is performed after the reception of the I²C data, and therefore the ACK is correctly generated even though at a later time the NVMWRT_NOK bit may be set.

The following flowchart describes the internal process of receiving I²C data and transferring them to the NVM EEPROM.

Figure 2-9. NVM Write Operation Flowchart.



The I²C block write operation allows the user to write multiple bytes of data to the memory in a single I²C transaction.

However, due to a known limitation in the current design, block writes that cross a page boundary and end at the first byte of the new page are not supported.

To avoid issues, ensure that any block write operation does not cross a page boundary and end at the first byte of the new page. Specifically, the starting address of the block write should be within the same page as the ending address, or if crossing a page boundary, the ending address should not be the first byte of the new page.

Example:

If the starting address is 0x000, writing 8 bytes (0x000 to 0x007) is valid.

If the starting address is 0x005, writing 3 bytes (0x005 to 0x007) is valid.

If the starting address is 0x007, writing 8 bytes (0x007 to 0x00E) is valid because it crosses the page boundary but did not end at the first byte of the new page (0x008).

If the starting address is 0x007, writing 2 bytes (0x007 to 0x008) is not valid because it crosses the page boundary and ends at the first byte of the new page (0x008).

If the starting address is 0x007, writing 10 bytes (0x007 to 0x010) is not valid because it crosses the page boundary and ends at the first byte of the new page (0x010). Attempting to write in such a manner will result in unpredictable behavior.

There are 64 pages in the EEPROM, each of which consists of 8 bytes. The start and end addresses for each page can be found below:

Table 2-24. EEPROM Pages

Page	Byte Address	Page	Byte Address	Page	Byte Address	Page	Byte Address
0	0x000-0x007	16	0x080-0x087	32	0x100-1x007	48	0x180-0x187
1	0x008-0x00F	17	0x088-0x08F	33	0x108-0x10F	49	0x188-0x18F
2	0x010-0x017	18	0x090-0x097	34	0x110-0x117	50	0x190-0x197
3	0x018-0x01F	19	0x098-0x09F	35	0x118-0x11F	51	0x198-0x19F
4	0x020-0x027	20	0x0A0-0x0A7	36	0x120-0x127	52	0x1A0-0x1A7
5	0x028-0x02F	21	0x0A8-0x0AF	37	0x128-1x02F	53	0x1A8-0x1AF
6	0x030-0x037	22	0x0B0-0x0B7	38	0x130-1x037	54	0x1B0-0x1B7
7	0x038-0x03F	23	0x0B8-0x0BF	39	0x138-0x13F	55	0x1B8-0x1BF
8	0x040-0x047	24	0x0C0-0x0C7	40	0x140-0x147	56	0x1C0-0x1C7
9	0x048-0x04F	25	0x0C8-0x0CF	41	0x148-0x14F	57	0x1C8-0x1CF
10	0x050-0x057	26	0x0D0-0x0D7	42	0x150-0x157	58	0x1D0-0x1D7
11	0x058-0x05F	27	0x0D8-0x0DF	43	0x158-0x15F	59	0x1D8-0x1DF
12	0x060-0x067	28	0x0E0-0x0E7	44	0x160-0x167	60	0x1E0-0x1E7
13	0x068-0x06F	29	0x0E8-0x0EF	45	0x168-0x16F	61	0x1E8-0x1EF
14	0x070-0x077	30	0x0F0-0x0F7	46	0x170-0x177	62	0x1F0-0x1F7
15	0x078-0x07F	31	0x0F8-0x0FF	47	0x178-0x17F	63	0x1F8-0x1FF

2.10.5 Block Read Transactions

The Block Read transactions (with and without CRC-8) are shown in the following figures:

Figure 2-10. Block Read Protocol without CRC-8 (Sr Applies to HS-Mode Transfer).

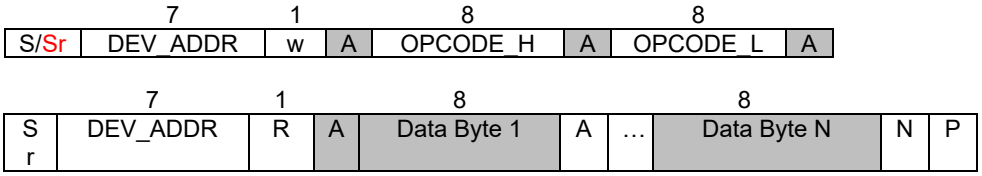
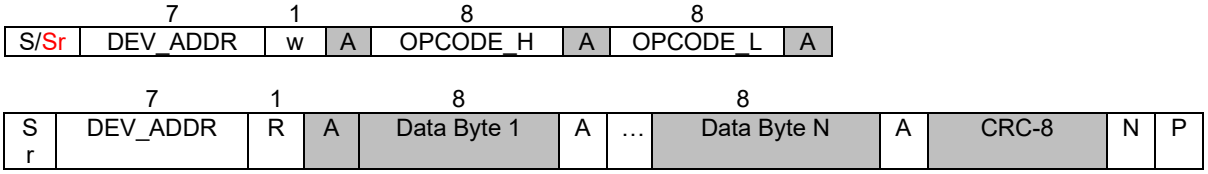


Figure 2-11. Block Read Protocol with CRC-8 (Sr Applies to HS-Mode Transfer).



As the block read transaction may be preceded by the master code announcing Hs-mode transfer, the first START condition will actually be a REPEATED START.

In target-transmitter mode, the MCP16701 will ALWAYS stream out at least one data byte, which is the content of the register A9.A0 - even though N5.N0 = '000000'.

Therefore, the block read operation will stream out only one data byte for both N5.N0 = '000000' and N5.N0 = '000001'.

Reading from a reserved/non-existing address will stream out all '1's (0xFF).

The CRC-8 generated by the MCP16701 includes the 0xFF bytes generated because of reading from reserved/non-existing addresses.

All single/block write must be followed by a dummy read.

When executing a block read command, the master device indicates the number of data bytes it intends to read at the beginning of the communication. The design assumes that the host device will complete the entire block read operation as specified, without prematurely terminating the transaction. Terminating the block read operation before the specified number of bytes have been transferred, by sending a NACK issued by the host device, can lead to unpredictable behavior. In the worst-case scenario, **the I²C bus will experience a stuck bus condition**.

A way in which you can avoid any stuck bus conditions is to use multiple single read commands instead of a block read command.

If it is known that the block read command may be interrupted, the block read command should be replaced by single reads.

2.10.6 I²C Special Commands

The following special I²C commands consist of 4-byte communications followed by a STOP bit. CRC-8 is not applicable to special commands.

- Byte1: DEV_ADDR = 0x5B with write bit
- Byte2: OPCODE_H = 0x07
- Byte3: special key (value is 0xXX - see table below for details)
- Byte4: password 0xDD

Table 2-25. Special I^2C Commands

Key	Description
0xD1	Key to enable I^2C write operations to NVM addresses (addresses 0x010 to 0x084)
0xD2	Key to revoke write permission to NVM addresses (addresses 0x010 to 0x084)
0xD3	Password key to enable I^2C write operations to xxVSETx volatile register addresses (e.g. B1VSET0 at address 0x21F, B1VSET1 at address 0x220, and so on)
0xD4	Password key to revoke write permission to xxVSETx volatile registers addresses
0xDB	REBOOT. The REBOOT command is equivalent to a device turn-off (same as if it was issued by EN), then reloads ALL values from EEPROM content to volatile registers, followed by a new start-up sequence.
Note: Special command effects are located in the volatile memory. Every time VDD is cycled, the granted permissions (keys 0xD1, 0xD3) are lost.	

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

PVINx to PGNDx	-0.3V to +6V
PGNDx to PGNDy	-0.3V to +0.3V
Output Switch Voltage SWx to PGNDx (DC)	-0.3V to V_{PVINx} +0.3V
FBx, FBLx to AGND	-0.3V to +6V
INL12, INL34 to AGND	-0.3V to +6V
OUTL1, OUTL2 to AGND	-0.3V to MIN (+6V, V_{INL12})
OUTL3, OUTL4 to AGND	-0.3V to MIN (+6V, V_{INL34})
AVCC to AGND	-0.3V to +6V
VDD to AGND	-0.3V to +6V
AGND, REFGND, DGND to PGNDx	-0.3V to +0.3V
AGND to REFGND	-0.3V to +0.3V
AGND to DGND	-0.3V to +0.3V
GNLC to AGND	-0.3V to MIN (+6V, V_{AVCC}+0.3V)
GNLC to FBLC	+4V to +4.2V
nRSTO_P, nRSTO_A, nINTO to AGND	-0.3V to +6V
EN, MODE, SELVL4 to AGND	-0.3V to +6V
SYNC, WDI to DGND	-0.3V to +6V
SDA, SCL to DGND	-0.3V to +6V
SYNCO to DGND	-0.3V to MIN (+6V, V_{VDD}+0.3V)
nWDO to DGND	-0.3V to +6V
General	
Maximum Junction Temperature	150°C
Storage Temperature	–65°C to 150°C
ESD Protection on all Pins:	
HBM	2 kV
HBM (SCL and SDA only)	1 kV
CDM	750V

Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2 Operating Ratings

PVINx Supply Voltage	+2.7V to +5.5V
INL12, INL34 Supply Voltage	+2.7V to +5.5V
VDD Supply Voltage	+2.7V to +5.5V
AVCC Supply Voltage	+2.7V to +5.5V
Junction Temperature Range (T_J)	–40°C to +105°C

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside the operating range.

3.3 Electrical Characteristics Table

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; L1 to L8 = 1.5 µH; C_{OUT1} to C_{OUT8} = 22 µF, unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Power Supply						
Supply Voltage Range (AVCC, PVINx, VDD)	V_{IN}	**2.7**	—	**5.5**	V	AVCC, PVINx, VDD connected together
Undervoltage Lockout Threshold (AVCC)	$V_{UVLO\_TH\_A}$	**2.4**	2.55	**2.7**	V	Turn-On
Undervoltage Lockout Hysteresis (AVCC)	$V_{UVLO\_HYS\_A}$	—	125	—	mV	
Undervoltage Lockout Threshold (VDD)	$V_{UVLO\_TH\_D}$	**2.4**	2.55	**2.7**	V	Turn-On
Undervoltage Lockout Hysteresis (VDD)	$V_{UVLO\_HYS\_D}$	—	125	—	mV	
Shutdown (OFF) Current	I_{SHDN}	—	42	**60**	µA	V_{EN} = 0V
Operational Quiescent Current (Switching), MODE = '0'	I_{QOP0_1}	—	1.6	—	mA	All channels enabled, except LDO Controller. Bucks in AutoPFM, typical application configuration.
Operational Quiescent Current (Switching), MODE = '1'	I_{QOP1}	—	30	—	mA	All channels enabled, Bucks in FPWM, typical application.
Timebase (Digital Oscillator)						
Timebase Frequency		—	8	—	MHz	
Timebase (Digital Oscillator) Accuracy	TB_ACC	**–10**	—	**+10**	%	
Switching Frequency Oscillator and Synchronization						
Free-Running Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FSD[1:0] = 00, 01, FPWM
Switching Frequency Displacement	FSD_10	—	–16.5	—	%	FPWM, FSD[1:0] = 10
	FSD_11	—	+16.5	—	%	FPWM, FSD[1:0] = 11
SYNC Frequency Range	f_{SYNC}	3		5	MHz	FPWM, $f_{SW} = f_{SYNC}/2$, application requirement only
SYNC HIGH Level	V_{IH_SYNC}	**1.5**	—	—	V	
SYNC LOW Level	V_{IL_SYNC}	—		**0.4**	V	
SYNC Minimum Pulse Width HIGH		—	50	—	ns	
SYNC Minimum Pulse Width LOW		—	50	—	ns	
SYNCO HIGH Level	V_{OH_SYNCO}	**2.6**	—	—	V	V_{VDD} = 3.0V, I_{OL} = –8 mA
SYNCO LOW Level	V_{OL_SYNCO}	—	—	**0.4**	V	V_{VDD} = 3.0V, I_{OL} = 8 mA
Thermal Showdown Protection and Thermal Early Warning						
Overtemperature Shutdown Threshold	T_{TSD}	—	160	—	°C	Bit TSD to '1'
Overtemperature Shutdown Hysteresis	T_{TSD_HYS}	—	20	—	°C	Bit TSD to '0'
Overtemperature Warning Threshold, TWRTH = '1'	T_{TWR1}	—	135	—	°C	Bit TWR to '1'
Overtemperature Warning Threshold, TWRTH = '0'	T_{TWR0}	—	125	—	°C	Bit TWR to '1'
Overtemperature Warning Hysteresis	T_{TWR_HYS}	—	5	—	°C	Bit TWR to '0'
Buck1 to Buck8 — Independent Operation						
Input Operating Voltage Range	V_{PVIN}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{OUT}	0.6	—	3.8	V	0.6V to 1.6V: 12.5 mV steps 1.6V to 3.8V: 25 mV steps

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; L1 to L8 = 1.5 µH; C_{OUT1} to C_{OUT8} = 22 µF, unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PVINx Shutdown Current	I_{PVIN_SHDN}	—	0.05	**2**	µA	V_{EN} = 0V, V_{PVINx} = 5V
Operational Quiescent Current, AutoPFM	I_{QOP_PFM}	—	50	—	µA	I_{OUTx} = 0 mA, AutoPFM, ΔIQ for Buck activated, 1V8 output
Operational Quiescent Current, FPWM	I_{QOP_PWM}	—	4.4	—	mA	I_{OUTx} = 0 mA, FPWM, ΔIQ for Buck activated
Feedback Voltage Accuracy	ACC_FB	**–0.8**	—	**+0.8**	%	$V_{FB} \ge 1V$
Output Voltage Peak-to-Peak Ripple, FPWM	ΔV_{OUTpp_PWM}	—	2	—	mVpp	V_{OUTx} = 1.0V, I_{OUTx} = 10 mA, FSD[1:0] = 00, 01 – BW = 20 MHz
Output Voltage Peak-to-Peak Ripple, AutoPFM	ΔV_{OUTpp_PFM}	—	10	—	mVpp	V_{OUTx} = 1.0V, I_{OUTx} = 10 mA, FSD[1:0] = 00, 01– BW= 20 MHz
Output Voltage Peak-to-Peak Ripple, AutoPFM, Frequency Division Disabled	$\Delta V_{OUTpp\_PFM\_FDD}$	—	5	—	mVpp	V_{OUTx} = 1.0V, I_{OUTx} = 10 mA, FSD[1:0] = 00, 01– BW= 20 MHz, DISFRQDIV = '1'
Output Voltage Line Regulation	$LINE\_REG_{PWM}$	—	0.05	—	%	I_{OUTx} =0 mA, FPWM, V_{OUTx} = 1.0V $V_{IN} = V_{PVINx} = V_{AVCC}$ = 2.7V to 5.5V
	$LINE\_REG_{PFM}$	—	0.1	—	%	I_{OUTx} = 0 mA, AutoPFM, V_{OUTx} = 1.0V $V_{IN} = V_{PVINx} = V_{AVCC}$ = 2.7V to 5.5V
Output Voltage Load Regulation	$LOAD\_REG_{PWM}$	—	0.3	—	%	I_{OUTx} = 0A to 1.5A, FPWM
	$LOAD\_REG_{PFM}$	—	0.5	—	%	I_{OUTx} = 0A to 1.5A, AutoPFM
Free-Running Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM, not synchronized (VSYNC = 0V), FSD[1:0] = 00, 01
Maximum Duty Cycle	D_{MAX}	**100**	—	**—**	%	Functionality test, DIS100D = '0'
		—	75	**—**	%	Functionality test, DIS100D = '1'
High-Side Switch ON-Resistance (PVINx to SWx)	$R_{DS(on)P}$	—	165	—	mΩ	$V_{PVINx} = V_{AVCC}$ = 5V
Low-Side Switch ON-Resistance (SWx to PGNDx)	$R_{DS(on)N}$	—	130	—	mΩ	$V_{PVINx} = V_{AVCC}$ = 5V
High-Side Peak Current Limit (Cycle by Cycle)	I_{LIM_HS}	2.0	2.7	3.4	A	
Current Limit Frequency Foldback Threshold	V_{TH_FFB}	**—**	500	**—**	mV	
Hiccup-Mode Short Circuit Protection Wait Time	t_{HICCUP}	**—**	3x Soft-Start Time	**—**	ms	
Low-Side Negative Peak Current Limit (FPWM)	I_{LIM_NEG}	—	–1.5	—	A	
Zero Current Detection Threshold	I_{ZCD}	**0**	75	**170**	mA	

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; L1 to L8 = 1.5 µH; C_{OUT1} to C_{OUT8} = 22 µF, unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Active Discharge Resistance	R_{DISCH_OUT}	—	25	—	Ω	DISCHEN = 1, enabled when regulator disabled
Feedback Resistance	R_{FB}	—	500	—	kΩ	
Output Overvoltage Threshold 00	OV_TH_00	**102.5**	104	**105.5**	%	% of $V_{FBx(nom)}$, FB rising, OVTH[1:0]='00'
Output Overvoltage Threshold 01	OV_TH_01	**104.5**	106	**107.5**	%	% of $V_{FBx(nom)}$, FB rising, OVTH[1:0]='01'
Output Overvoltage Threshold 10	OV_TH_10	**106**	108	**110**	%	% of $V_{FBx(nom)}$, FB rising, OVTH[1:0]='10'
Output Overvoltage Threshold 11	OV_TH_11	**108**	110	**112**	%	% of $V_{FBx(nom)}$, FB rising, OVTH[1:0]='11'
Output Overvoltage Threshold Hysteresis	OV_TH_HYS	—	1	—	%	% of $V_{FBx(nom)}$, FB falling, all OVTH[1:0] settings
Output Undervoltage Threshold 00	UV_TH_00	**94.5**	96	**97.5**	%	% of $V_{FBx(nom)}$, FB falling, UVTH[1:0]='00'
Output Undervoltage Threshold 01	UV_TH_01	**92.5**	94	**95.5**	%	% of $V_{FBx(nom)}$, FB falling, UVTH[1:0]='01'
Output Undervoltage Threshold 10	UV_TH_10	**90.5**	92	**93.5**	%	% of $V_{FBx(nom)}$, FB falling, UVTH[1:0]='10'
Output Undervoltage Threshold 11	UV_TH_11	**88**	90	**92**	%	% of $V_{FBx(nom)}$, FB falling, UVTH[1:0]='11'
Output Undervoltage Threshold Hysteresis	UV_TH_HYS	—	1	—	%	% of $V_{FBx(nom)}$, FB rising, all UVTH[1:0] settings
POK Threshold	POK_TH	**90.5**	92.5	**94.5**	%	% of $V_{FBx(nom)}$, FB rising
POK Hysteresis	POK_HYS	—	4	—	%	% of $V_{FBx(nom)}$, FB falling
Start-Up POK (UV) Bypass Threshold	$V_{POKB\_TH\_B}$	—	560	—	mV	PVINx-FBx, FBx rising, PVINx = 3.0V, $V_{OUTx(NOM)}$ = 3.3V
Start-Up POK (UV) Bypass Threshold Hysteresis	$V_{POKB\_HYS\_B}$	—	26	—	mV	FBx falling, PVINx = 3.0V

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; L1 to L8 = 1.5 µH; C_{OUT1} to C_{OUT8} = 22 µF, unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Soft-start Rate	ONSR_000	—	2	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	4	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_001	—	4	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	8	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_010	—	8	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	16	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_011	—	16	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	32	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_100	—	32	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	64	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_101	—	64	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	128	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_110	—	128	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	256	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step
	ONSR_111	—	256	—	µs/step	$0.6V \le V_{OUTx} \le 1.6V$, ±12.5 mV step
		—	512	—	µs/step	$1.6V \le V_{OUTx} \le 3.8V$, ±25 mV step

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; L1 to L8 = 1.5 µH; C_{OUT1} to C_{OUT8} = 22 µF, unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Dynamic Voltage Scaling Rate	DVSR_00	—	1	—	µs/step	0.6V ≤ V_{OUTx} ≤ 1.6V, ±12.5 mV step
		—	2	—	µs/step	1.6V ≤ V_{OUTx} ≤ 3.8V, ±25 mV step
	DVSR_01	—	2	—	µs/step	0.6V ≤ V_{OUTx} ≤ 1.6V, ±12.5 mV step
		—	4	—	µs/step	1.6V ≤ V_{OUTx} ≤ 3.8V, ±25 mV step
	DVSR_10	—	4	—	µs/step	0.6V ≤ V_{OUTx} ≤ 1.6V, ±12.5 mV step
		—	8	—	µs/step	1.6V ≤ V_{OUTx} ≤ 3.8V, ±25 mV step
	DVSR_11	—	8	—	µs/step	0.6V ≤ V_{OUTx} ≤ 1.6V, ±12.5 mV step
		—	16	—	µs/step	1.6V ≤ V_{OUTx} ≤ 3.8V, ±25 mV step
Buck1 to Buck8 — Parallel Operation						
Channel-to-Channel High-Side ON-Resistance Mismatch	$\%\Delta R_{DS(on)P}$	—	10	—	%	PVINx = AVCC = 5V TYP = 1x std dev, in % - pin-to-pin
Channel-to-Channel Low-Side ON-Resistance Mismatch	$\%\Delta R_{DS(on)N}$	—	10	—	%	PVINx = AVCC = 5V TYP = 1x std dev, in % - pin-to-pin
Inductor Peak Current Limit (Cycle by Cycle), 2 in Parallel	I_{LIM_Px2}	—	5.4	—	A	L = 1 µH C_{OUT} = 47 µF
Inductor Peak Current Limit (Cycle by Cycle), 3 in Parallel	I_{LIM_Px3}	—	8.1	—	A	L = 680 nH C_{OUT} = 68 µF
Inductor Peak Current Limit (Cycle by Cycle), 4 in Parallel	I_{LIM_Px4}	—	10.8	—	A	L = 470 nH C_{OUT} = 100 µF
Inductor Negative Peak Current Limit (FPWM), 2 in Parallel	$I_{LIM\_NEG\_Px2}$	—	-3.1	—	A	L = 1 µH C_{OUT} = 47 µF
Inductor Negative Peak Current Limit (FPWM), 3 in Parallel	$I_{LIM\_NEG\_Px3}$	—	-4.65	—	A	L = 680 nH C_{OUT} = 68 µF
Inductor Negative Peak Current Limit (FPWM), 4 in Parallel	$I_{LIM\_NEG\_Px4}$	—	-6.2	—	A	L = 470 nH C_{OUT} = 100 µF
Inductor Zero Current Detection Threshold, 2 in Parallel	I_{ZCD_Px2}	—	150	—	mA	L = 1 µH C_{OUT} = 47µF
Inductor Zero Current Detection Threshold, 3 in Parallel	I_{ZCD_Px3}	—	225	—	mA	L = 680 nH C_{OUT} = 68 µF
Inductor Zero Current Detection Threshold, 4 in Parallel	I_{ZCD_Px4}	—	300	—	mA	L = 470 nH C_{OUT} = 100 µF

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{INL12} = V_{INL34} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; bit NVM_ENSELVL4 = '0'; $V_{OUTL1} = V_{OUTL2} = V_{OUTL3} = V_{OUTL4} = 2.5V$; $C_{INL12} = C_{INL34} = 4.7\ \mu F$ at least, $C_{OUTLx} = 2.2\ \mu F$, ($I_{OUTLx} = 150$ mA) or 4.7 µF ($I_{OUTLx} = 300$ mA) unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
LDO1, LDO2, LDO3, LDO4						
Input Operating Voltage Range	V_{INL}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{OUTL}	0.6	—	3.8	V	0.6V to 1.6V: 12.5 mV steps 1.6V to 3.8V: 25 mV steps
Stable Output Capacitance Range	C_{OUTL}	2.2	—	20	µF	$I_{OUTLx} \le 150$ mA – application requirement only
		4.7	—	20	µF	$I_{OUTLx} \le 300$ mA – application requirement only
INL12, INL34 Shutdown Current	I_{INL_SHDN}	—	—	**2**	µA	LDOs disabled, $V_{INL} = 5V$
Operational Quiescent Current	I_{INL_Q}	—	47	—	µA	$I_{OUTLx} = 0$ mA, ΔIQ for one LDO activated
Feedback Voltage Accuracy	ACC_FBL	**–1**	—	**+1**	%	$V_{FBx} \ge 1.8V$
Dropout Voltage	V_{DO}	—	150	**215**	mV	$V_{INLxy} = 5V$, $V_{DO} = V_{INLxy} - V_{OUTLx/y}$, $I_{OUTLx/y} = 300$ mA, FBYPM = '1', one LDO loaded only
		—	175	500		$V_{INLxy} = 3.3V$, VDO = $V_{INLxy} - V_{OUTLx/y}$, $I_{OUTLx/y} = 300$ mA, FBYPM = '1', one LDO loaded only
Output Voltage Line Regulation	LINE_REG	—	0.01	—	%	$V_{OUTLx} = 1.8V$, $V_{IN} = V_{INLxx} = V_{AVCC} = 2.7V$ to 5.5V $I_{OUTLx} = 0.1$ mA
		—	0.015	—	%	$V_{OUTLx} = 2.5V$ $V_{IN} = V_{INLxx} = V_{AVCC} = 2.7V$ to 5.5V $I_{OUTLx} = 0.1$ mA
Output Voltage Load Regulation	LOAD_REG	—	0.3	—	%	$V_{OUTLx} = 2.5V$ $I_{OUTLx} = 0.1$ mA to 300 mA
PSRR	PSRRx	—	59	—	dB	f = 1 kHz, $I_{OUTLx} = 20$ mA, $V_{OUTLx} = 1.8V$, AVCC and I_{NLxx} modulated
		—	73	—	dB	f = 1 kHz, $I_{OUTLx} = 20$ mA, $V_{OUTLx} = 1.8V$, $V_{AVCC} = 5V$, I_{NLxx} modulated
		—	38	—	dB	f = 10 kHz, $I_{OUTLx} = 20$ mA, $V_{OUTLx} = 1.8V$, AVCC and I_{NLxx} modulated
		—	51	—	dB	f = 10kHz, $I_{OUTLx} = 20$ mA, $V_{OUTLx} = 1.8V$, $V_{AVCC} = 5V$, I_{NLxx} modulated
Total Output Voltage Noise		—	265	—	µVRMS	10 Hz to 100 kHz, $I_{OUTLx} = 20$ mA
Current Limit	I_{LIM_OUTL}	**280**	420	**550**	mA	$V_{AVCC} = V_{INLxx} = 4.5V$, $V_{FBLx} = 80\%$ of nominal

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{INL12} = V_{INL34} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; bit NVM_ENSELVL4 = '0'; $V_{OUTL1} = V_{OUTL2} = V_{OUTL3} = V_{OUTL4} = 2.5V$; $C_{INL12} = C_{INL34} = 4.7\ \mu F$ at least, $C_{OUTLx} = 2.2\ \mu F$, ($I_{OUTLx} = 150$ mA) or $4.7\ \mu F$ ($I_{OUTLx} = 300$ mA) unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Active Discharge Resistance	R_{DISCH_OUTL}	—	25	—	Ω	DISCHEN=1, Enabled when regulator disabled, during negative DVS
Feedback Resistance	R_{FB}	—	1500	—	kΩ	
POK Threshold	POK_TH	**90.5**	92.5	**94.5**	%	% of $V_{FBx(nom)}$, FB rising
POK Hysteresis	POK_HYS	—	4	—	%	% of $V_{FBx(nom)}$, FB falling
Start-Up POK Bypass Threshold	$V_{POKB\_TH\_L}$	—	700	—	mV	INLxx - OUTLx, OUTLx rising, $V_{INLxx} = 3.0V$, $V_{OUTLx(NOM)} = 3.3V$
Start-Up POK Bypass Threshold Hysteresis	$V_{POKB\_HYS\_L}$	—	28	—	mV	OUTLx falling, $V_{INLxx} = 3.0V$
Forced Bypass Mode Maximum Output Voltage	V_{FBYPM_OUTLx}	**5.06**	5.25	**5.44**	V	FBYPM = '1', $I_{OUTLx} = 0.1$ mA

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{INL12} = V_{INL34} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; bit NVM_ENSELVL4 = '0'; $V_{OUTL1} = V_{OUTL2} = V_{OUTL3} = V_{OUTL4} = 2.5V$; $C_{INL12} = C_{INL34} = 4.7\ \mu F$ at least, $C_{OUTLx} = 2.2\ \mu F$, ($I_{OUTLx} = 150$ mA) or 4.7 µF ($I_{OUTLx} = 300$ mA) unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Soft-start Rate	ONSR_000	—	2	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5mV step
		—	4	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_001	—	4	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	8	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_010	—	8	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	16	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_011	—	16	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	32	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_100	—	32	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	64	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_101	—	64	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	128	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_110	—	128	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	256	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	ONSR_111	—	256	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	512	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{INL12} = V_{INL34} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{SYNC} = 0V$; bit NVM_ENSELVL4 = '0'; $V_{OUTL1} = V_{OUTL2} = V_{OUTL3} = V_{OUTL4} = 2.5V$; $C_{INL12} = C_{INL34} = 4.7\ \mu F$ at least, $C_{OUTLx} = 2.2\ \mu F$, ($I_{OUTLx} = 150$ mA) or 4.7 µF ($I_{OUTLx} = 300$ mA) unless otherwise specified. Bold values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Dynamic Voltage Scaling Rate	DVSR_00	—	1	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	2	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	DVSR_01	—	2	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	4	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	DVSR_10	—	4	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	8	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
	DVSR_11	—	8	—	µs/step	$0.6V \le V_{OUTLx} \le 1.6V$, ±12.5 mV step
		—	16	—	µs/step	$1.6V \le V_{OUTLx} \le 3.8V$, ±25 mV step
SELVL4 Input						
Logic HIGH Input Voltage VIH	V_{IH_SELVL4}	**1.5**	—	—	V	$V_{INL34} = V_{AVCC} = V_{VDD}$ = 2.7V to 5.5V
Logic LOW Input Voltage VIL	V_{IL_SELVL4}	—	—	**0.4**	V	$V_{INL34} = V_{AVCC} = V_{VDD}$ = 2.7V to 5.5V

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{FBLC(nom)} = 1.05V$; Q1 = SiAA02DJ; $V_{DRAIN(Q1)} = V_{FBLC(nom)} + 300$ mV = 1.35V, $C_{OUTLC} = 4.7\ \mu F$, ($I_{OUTLC} \le 300$ mA), 22 µF; ($I_{OUTLC} \le 1.5A$) unless otherwise specified. **Bold** values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
LDO Controller						
Input Operating Voltage Range	V_{AVCC}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{FBLC}	0.6	—	1.6	V	12.5 mV steps
Stable Output Capacitance Range	C_{OUTLC}	4.7	—	120	µF	$I_{OUTLC} \le 300$ mA
		22	—	120	µF	$I_{OUTLC} \le 1.5A$
Operational Quiescent Current	$I_{AVCC\_LC\_Q}$	—	0.5	—	mA	ΔI_Q for LDO Controller activated
Feedback Voltage Accuracy	ACC_FBLC	**–1.5**	—	**+1**	%	$V_{FBLC} \ge 0.9V$
Output Voltage Line Regulation, from Bias (AVCC)	LINE_REG_BIAS	—	0.015	—	%	$V_{AVCC} = (V_{FBLC(nom)} + 2.5V)$ to 5.5V, $I_{OUTLC} = 20$ mA
Output Voltage Line Regulation, from Input (VDRAIN(Q1))	LINE_REG _INPUT	—	0.01	—	%	$V_{DRAIN(Q1)} = (V_{FBLC(nom)} + 300$ mV) to 5.5V, $I_{OUTLC} = 20$ mA
Output Voltage Load Regulation	LOAD_REG	—	0.02	—	%	I_{OUTLC} = 1 mA to 1.5A
Maximum GNLC Output Current (Sink/ Source)	I_{GNLC}	—	12	—	mA	

Electrical Characteristics Table (continued)

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{PVINx} = V_{VDD} = 5V$; $V_{FBLC(nom)} = 1.05V$; Q1 = SiAA02DJ; $V_{DRAIN(Q1)} = V_{FBLC(nom)} + 300\ mV = 1.35V$, $C_{OUTLC} = 4.7\ \mu F$, ($I_{OUTLC} \le 300\ mA$), 22 µF; ($I_{OUTLC} \le 1.5A$) unless otherwise specified. **Bold** values indicate $-40°C \le T_J \le +105°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Gate-Source Clamping Level, Positive Polarity	V_{GNFB_CLAMP}	—	4.75	**5**	V	Bias FBLC to AGND, measured voltage at GNLC, $V_{AVCC} = 5.5V$
Gate-Source Clamping Level, Negative Polarity	V_{FBGN_CLAMP}	—	4.75	**5**	V	Bias FBLC to AGND, measured voltage at GNLC, $V_{AVCC} = 5.5V$
PSRR	PSRR	—	54	—	dB	f = 1 kHz, I_{OUTLC} = 20 mA, AVCC modulated, C_{OUTLC} = 22 µF
		—	76	—	dB	f = 1 kHz, I_{OUTLC} = 20 mA, V_{AVCC} = 5V, drain of Q1 modulated, C_{OUTLC} = 22 µF
		—	33	—	dB	f = 10 kHz, I_{OUTLC} = 20 mA, AVCC modulated, C_{OUTLC} = 22 µF
		—	55	—	dB	f = 10 kHz, I_{OUTLC} = 20 mA, V_{AVCC} = 5V, drain of Q1 modulated, C_{OUTLC} = 22 µF
		—	51	—	dB	f = 100 kHz, I_{OUTLC} = 20 mA, AVCC modulated, C_{OUTLC} = 22 µF
		—	60	—	dB	f = 100 kHz, I_{OUTLC} = 20 mA, V_{AVCC} = 5V, drain of Q1 modulated, C_{OUTLC} = 22 µF
Total Output Voltage Noise		—	265	—	µVRMS	10 Hz to 100 kHz, I_{OUTLC} = 20 mA
Active Discharge Resistance	R_{DISCH_FBLC}	—	25	—	Ω	DISCHEN = 1, Enabled when regulator disabled, during negative DVS
POK Threshold	POK_TH	**90.5**	92.5	**94.5**	%	% of $V_{FBLC(nom)}$, FB rising
POK Hysteresis	POK_HYS	—	4	—	%	% of $V_{FBLC(nom)}$, FB falling
Soft-start Rate	ONSR_000	—	2	—	µs/step	0.6V ≤ V_{FBLC} ≤ 1.6V, ±12.5 mV step
	ONSR_001	—	4	—	µs/step	
	ONSR_010	—	8	—	µs/step	
	ONSR_011	—	16	—	µs/step	
	ONSR_100	—	32	—	µs/step	
	ONSR_101	—	64	—	µs/step	
	ONSR_110	—	128	—	µs/step	
	ONSR_111	—	256	—	µs/step	
Dynamic Voltage Scaling Rate	DVSR_00	—	1	—	µs/step	
	DVSR_01	—	2	—	µs/step	
	DVSR_10	—	4	—	µs/step	
	DVSR_11	—	8	—	µs/step	

Electrical Specifications: $T_A = T_J = +25°C$; $V_{IN} = V_{AVCC} = V_{VDD} = 5V$ unless otherwise specified. **Bold** values indicate $-40°C \le T_J \le +105°C$						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
EN Input						
Logic HIGH Input Voltage	V_{IH_EN}	**1.5**	—	—	V	$V_{AVCC} = V_{VDD}$ = 2.7V to 5.5V
Logic LOW Input Voltage	V_{IL_EN}	—	—	**0.4**	V	$V_{AVCC} = V_{VDD}$ = 2.7V to 5.5V
EN Analog Deglitch Time	t_{DT_EN}	—	10	—	µs	
EN Input Leakage Current	I_{lkg_EN}	**–1**	—	**1**	µA	
nRSTO_A, nRSTO_P, nINTO, nWDO Logic Outputs						
Output Voltage LOW	V_{OL}	—	—	**0.4**	V	$V_{AVCC} = V_{VDD}$ = 2.7V to 5.5V, I_{OL} = 2 mA
Leakage Current	I_{lkg}	—	—	**1**	µA	5.5V applied, output driver OFF
Watchdog Timer						
WDI Logic HIGH Input Voltage	V_{IH_WDI}	**1.5**	—	—	V	V_{VDD} = 2.7V to 5.5V
WDI Logic LOW Input Voltage	V_{IL_WDI}	—	—	**0.4**	V	V_{VDD} = 2.7V to 5.5V
WDI Minimum Pulse Width	t_{WP}	—	140	—	ns	
Watchdog Timeout Period (WDMODE = '0')	t_{WD}	—	2	—	ms	WDTOD[2:0] = ’000’
		—	8	—	ms	WDTOD[2:0] = ’001’
		—	32	—	ms	WDTOD[2:0] = ’010’
		—	128	—	ms	WDTOD[2:0] = ’011’
		—	512	—	ms	WDTOD[2:0] = ’100’
		—	2048	—	ms	WDTOD[2:0] = ’101’
		—	8192	—	ms	WDTOD[2:0] = ’110’
		—	32768	—	ms	WDTOD[2:0] = ’111’
Watchdog Output nWDO Pulse Width (WDMODE = '0')	t_{WR}	—	16	—	ms	WDRSP[1:0] = ’00’
		—	32	—	ms	WDRSP[1:0] = ’01’
		—	64	—	ms	WDRSP[1:0] = ’10’
		—	128	—	ms	WDRSP[1:0] = ’11’
I^2C Interface Pins (SDA, SCL)						
SCL, SDA Logic HIGH Input Voltage	V_{IH}	**1.5**	—	—	V	V_{VDD} = 2.7V to 5.5V
SCL, SDA Logic LOW Input Voltage	V_{IL}	—	—	**0.4**	V	V_{VDD} = 2.7V to 5.5V
Hysteresis of Schmitt Trigger Inputs	V_{hys}	—	0.2	—	V	
SDA, SCL Leakage Current	I_{lkg}	—	—	**1**	µA	SDA driver OFF, V_{SDA} = 5.5V, V_{SCL} = 5.5V
SDA Output Voltage LOW	V_{OL}	—	—	**0.4**	V	V_{VDD} = 2.7V to 5.5V, I_{OL} = 20 mA
Maximum SCL Clock Frequency, FS+ Mode	f_{SCL_FS+}	—	1	—	MHz	
Maximum SCL Clock Frequency, HS Mode	f_{SCL_HS}	—	3.4	—	MHz	C_{BUS} < 100 pF
Maximum Pulse Width of Input Spikes that must be Suppressed, FS+ Mode(1) – Note 1	t_{SP_FS+}	—	50	—	ns	
Maximum Pulse Width of Input Spikes that must be Suppressed, HS Mode(2) – Note 2	t_{SP_HS}	—	10	—	ns	After ACK to Master Code
GPO (General Purpose Output)						
GPO Output Voltage HIGH	V_{OH_GPO}	**2.6**	—	—	V	V_{VDD} = 3.0V, I_{OL} = –8 mA
GPO Output Voltage LOW	V_{OL_GPO}	—	—	**0.4**	V	V_{VDD} = 3.0V, I_{OL} = 8 mA

Notes:

1. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 10 ns.

3.4 Thermal Characteristics

Table 3-1. Package Information

Package	No. of Pins	Junction-to-Ambient Thermal Resistence (θ_{JA})	Junction-to-Case Thermal Resistence (θ_{JC})	Junction-to-Bottom Thermal Resistence (θ_{JB})	Ψ_{JC}
8 mm x 8 mm VQFN	64	17.068°C/W	10.511°C/W	3.064°C/W	0.236°C/W

4. Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 4-1. MOSFET $R_{DS(ON)}$ vs. Temperature (V_{IN} = 5V)

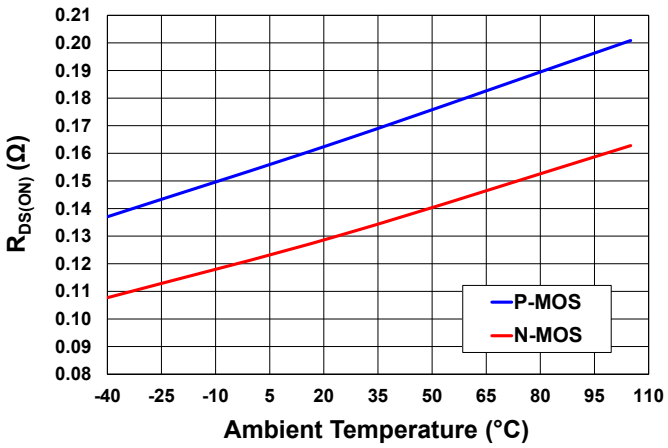


Figure 4-2. V_{IN} Operating Current vs. Input Voltage vs. Temperature (FPWM Mode)

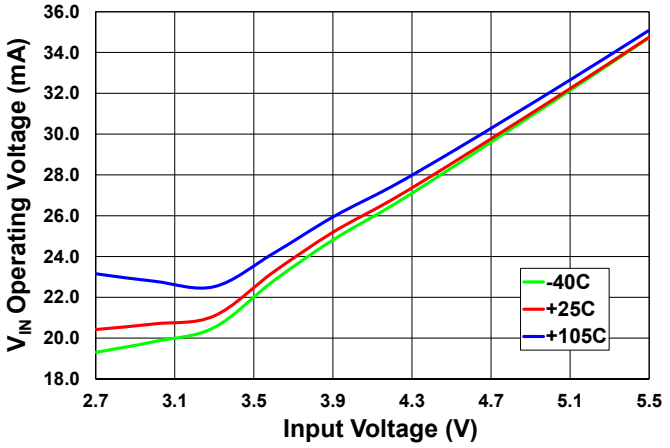


Figure 4-3. Buck 1 to Buck 4 in Parallel Configuration Efficiency vs. Load Current (V_{OUT} = 1.0V)

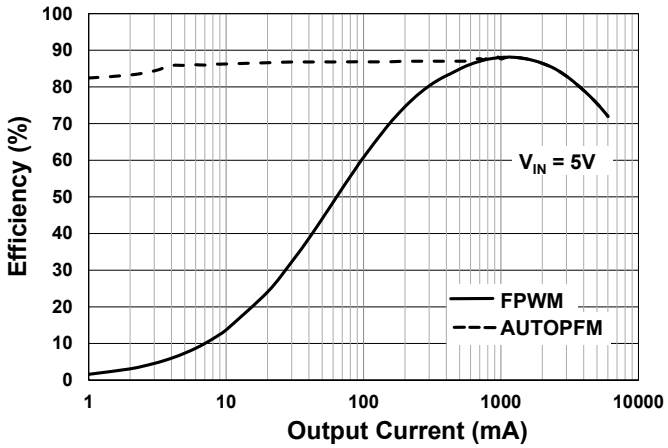


Figure 4-4. Buck 5 and Buck 6 in Parallel Configuration Efficiency vs. Load Current (V_{OUT} = 1.35V)

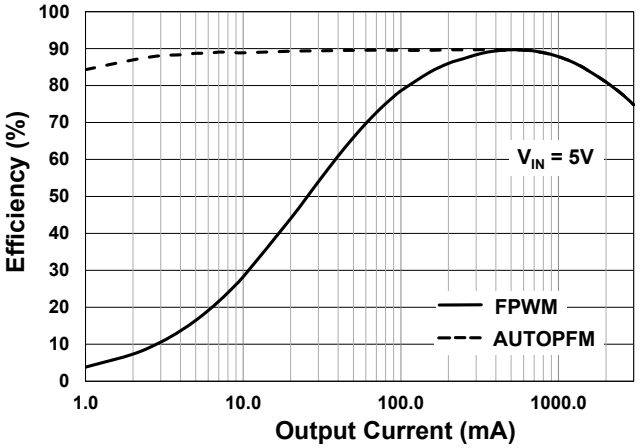


Figure 4-5. Buck 7 Efficiency vs. Load Current (V_{OUT} = 3.3V)

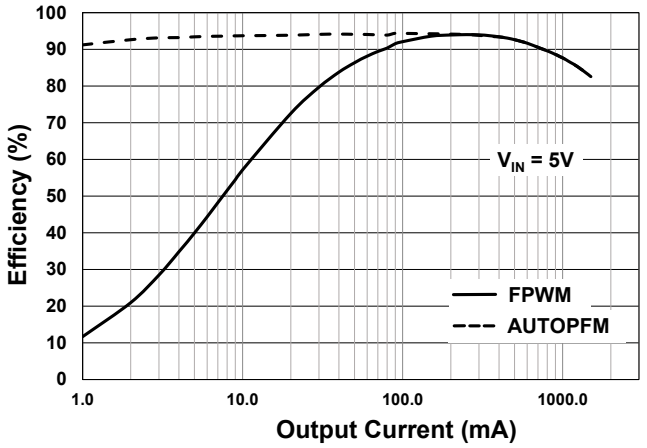


Figure 4-6. LDO1 Dropout Voltage vs Load Current

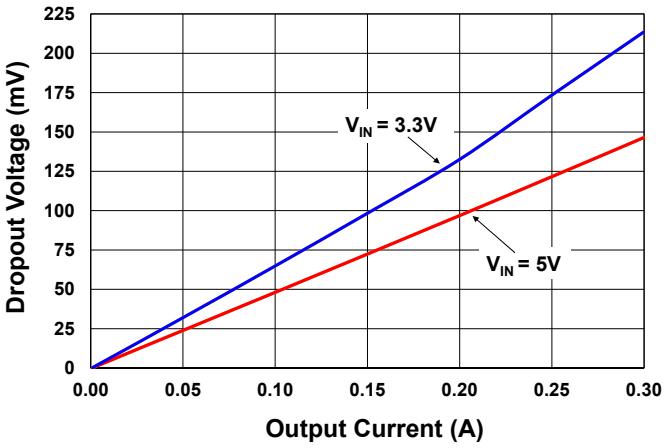


Figure 4-7. EN pin Start-up Sequence

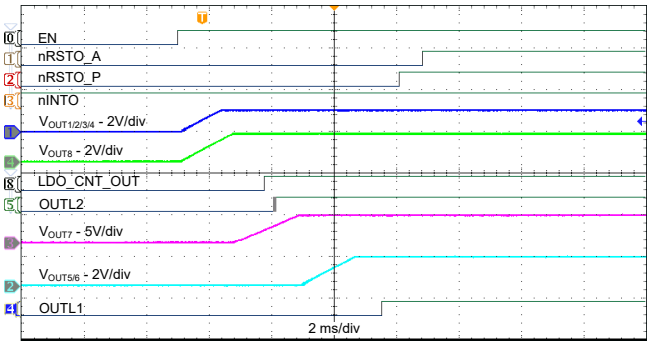


Figure 4-8. EN pin Shutdown Sequence

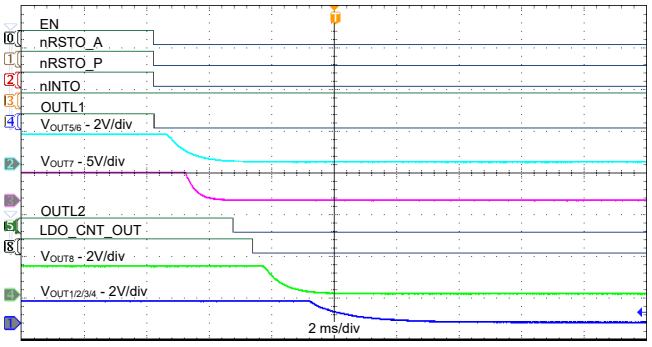


Figure 4-9. Buck Channels Output Voltage Ripple (AutoPFM Mode)

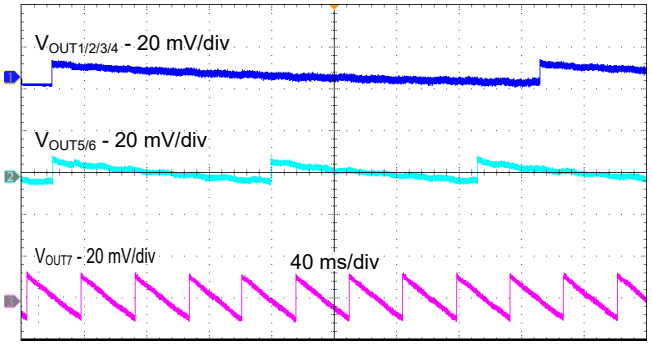


Figure 4-10. Buck Channels Output Voltage Ripple (FPWM Mode)

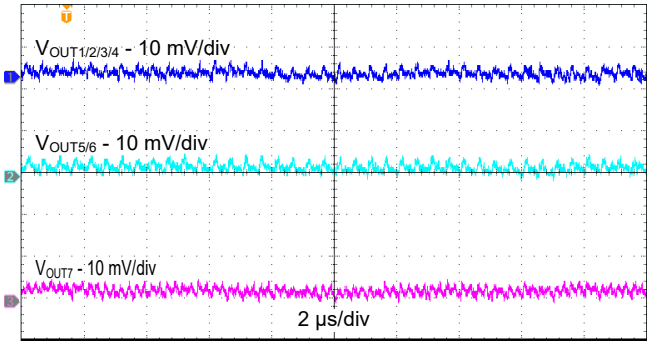


Figure 4-11. Line Transient Response (FPWM Mode)

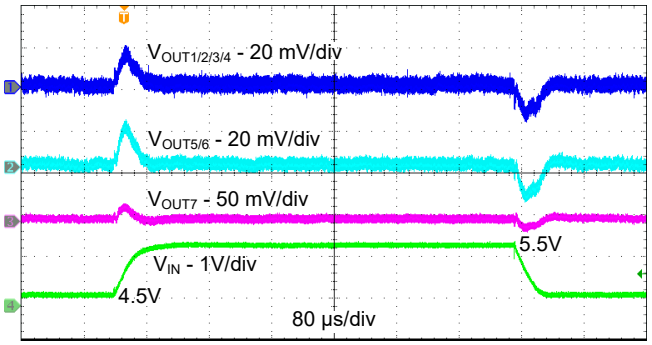


Figure 4-12. Buck 1 to Buck 4 in Parallel Configuration Load Transient Response (FPWM Mode, $V_{OUT1/2/3/4}$ = 1V)

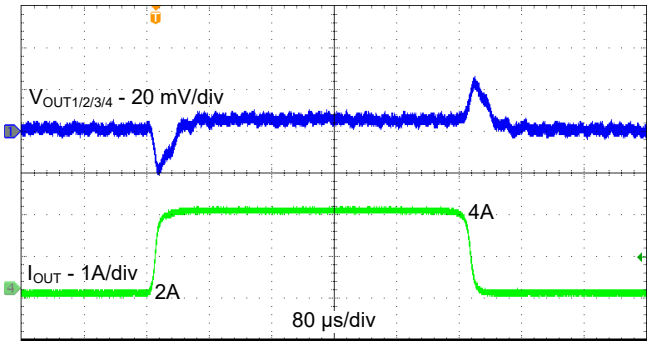


Figure 4-13. Buck 5 and Buck 6 in Parallel Configuration Load Transient Response (FPWM Mode, $V_{OUT5/6}$ = 1.35V)

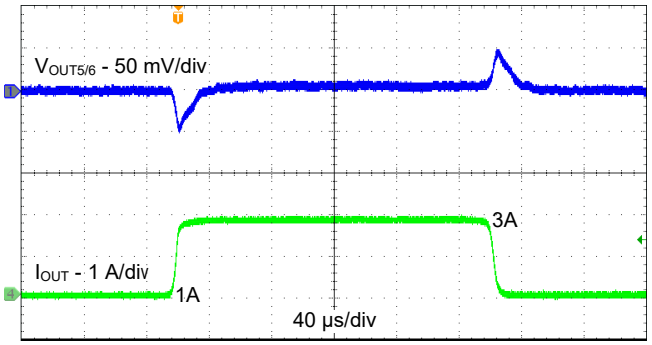


Figure 4-14. Buck 7 Load Transient Response (FPWM Mode, V_{OUT7} = 3.3V)

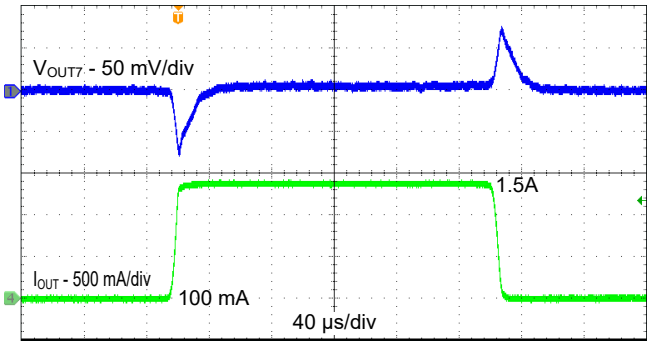


Figure 4-15. LDO Controller Load Transient Response (V_{OUT_LDOCNT} = 1.05V)

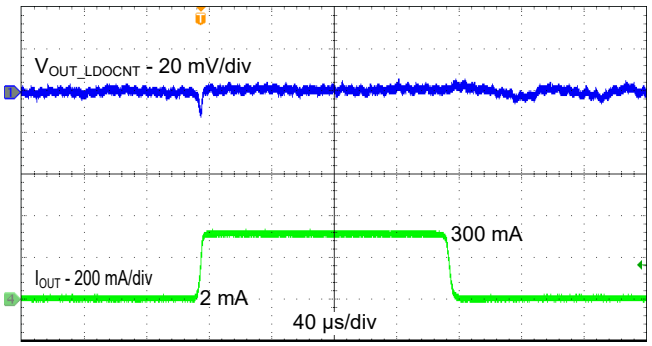


Figure 4-16. LDO1 Load Transient Response (OUTL1 = 1.8V)

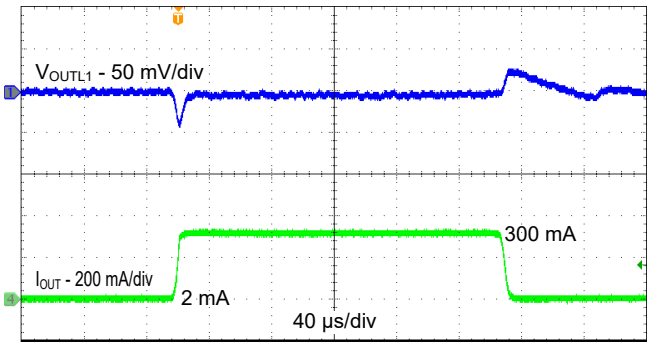


Figure 4-17. Transition IN and OUT of Forced Bypass Mode (I_{OUT} = 100 mA, V_{IN} = 5.5V)

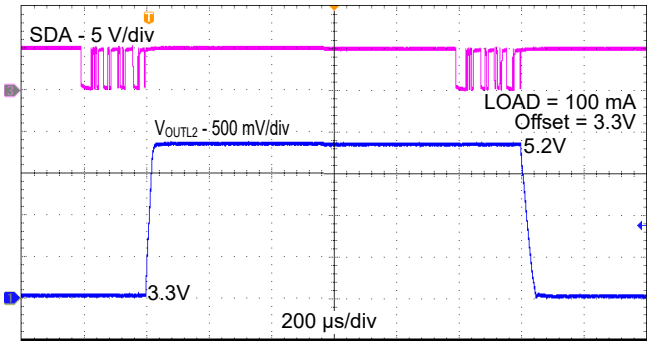


Figure 4-18. SELVL4 Pin Transition (ENSELVL4 = 1, POLSELV = 1)

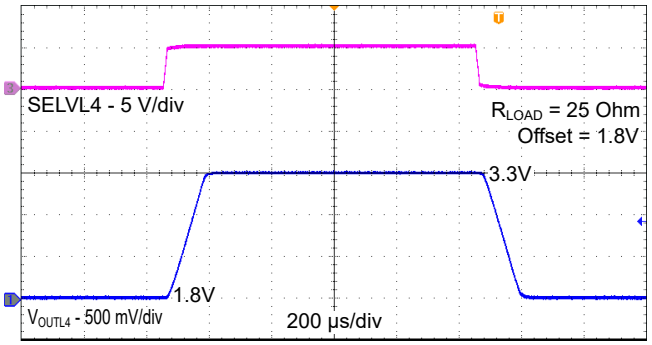


Figure 4-19. Output Short Circuit – Buck 1 to Buck 4 in Parallel Configuration (DISHCP = 0)

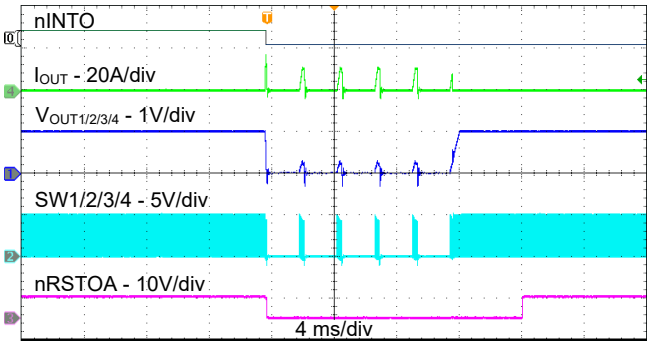


Figure 4-20. Output Short Circuit – Buck 5 and Buck 6 in Parallel Configuration (DISHCP = 0)

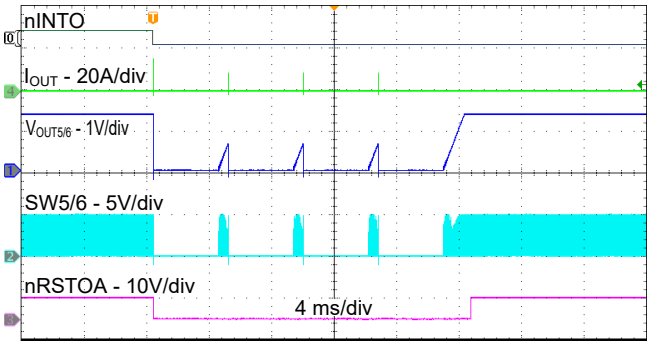
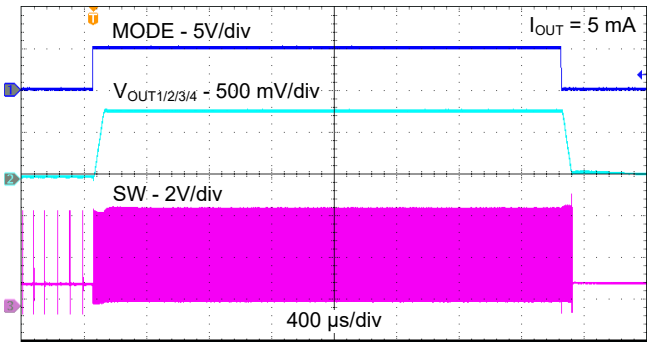


Figure 4-21. MODE Pin Transition – Buck 1 to Buck 4 in Parallel Configuration ($V_{OUT1/2/3/4}$ = 1V to 1.8V)



5. Application Information

5.1 Recommended External Components

Table 5-1. Recommended External Components for MCP16701

Item	Part Number	Manufacturer	Description	Notes
CPVIN1-CPVIN8 (Independent Buck channel), CINL12, CINL34, COUTL1 - COUTL4 (300mA LDO current)	C1608X7S1A475K080AC	TDK Corporation	Capacitor, 4.7 µF, 10V, 10%, X7S, Size 0603	
	885012106012	Würth Elektronik	Capacitor, 4.7 µF, 20V, 10%, X5R, Size 0603	
	GRM188C71A475KE11D	Murata Electronics®	Capacitor, 4.7 µF, 10V, 10%, X7S, Size 0603	
C_AVCC, C_VDD	C1608X7R1E105K080AB	TDK Corporation	Capacitor, 1 µF, 25V, 10%, X7R, Size 0603	
	885012206076	Würth Elektronik	Capacitor, 1 µF, 25V, 10%, X5R, Size 0603	
	GCM188R71E105KA64J	Murata Electronics	Capacitor, 1 µF, 25V, 10%, X7R, Size 0603	
COUT_LDOC, CIN_LDOC, COUT (Independent operation)	C2012X7S1A226M125AC	TDK Corporation	Capacitor, 22 µF, 10V, 20%, X7S, Size 0805	
	885012107011	Würth Elektronik	Capacitor, 22 µF, 10V, 20%, X5R, Size 0805	
	GRM21BR61A226ME44L	Murata Electronics	Capacitor, 22 µF, 10V, 20%, X5R, Size 0805	
COUT (two Buck channels in parallel)	C3225X7S0J476M250AC	TDK Corporation	Capacitor, 47 µF, 6.3V, 20%, X7S, Size 1210	Min required 1 x 47 µF or 2 x 22 µF
	885012109003	Würth Elektronik	Capacitor, 47 µF, 6.3V, 20%, X7S, Size 1210	
	GCM32ER70J476KE19L	Murata Electronics	Capacitor, 47 µF, 6.3V, 10%, X7S, Size 1210	
COUT (three Buck channels in parallel)	C3216X5R1A686M160AC	TDK Corporation	Capacitor, 68 µF, 10V, X5R, 20%, Size 1206	Min required 1 x 47 µF and 1 x 22 µF
COUT (four Buck channels in parallel)	C3216X5R0J107M160AB	TDK Corporation	Capacitor, 100 µF, 6.3V, X5R, 20%, Size 1206	Min required 2 x 47 µF
	885012108005	Würth Elektronik	Capacitor, 100 µF, 6.3V, X5R, 20%, Size 1206	
	GRM31CR60J107MEA8K	Murata Electronics	Capacitor, 100 µF, 6.3V, X5R, 20%, Size 1206	
L (independent operation)	DFE252012P-1R5M=P2	Murata Electronics	1.5 µH, 60 mΩ, 3.5A, 20%, Size 1008	
	74479288215	Würth Elektronik	1.5 µH, 77 mΩ, 4.25A, 20%, Size 1008	
	TFM252012ALMA1R5MTAA	TDK Corporation	1.5 µH, 60 mΩ, 3.1A, Size 1008	
	LPS4012-152MRC	Coilcraft	1.5 µH, 70 mΩ, 2.2A, 20%, Size L3.9mm x W3.9mm	
L (two Buck channels in parallel)	SPM4030T-1R0M	TDK Corporation	1 µH, 15.5 mΩ, 8A, Size L4.2mm x W4H3.0mm	
	74437324010	Würth Elektronik	1 µH, 27 mΩ,5A, Size L4.45 mm x W4.06 mm	
	XGL4015-102MEC	Coilcraft	1 µH, 18 mΩ, 6.5A, 20%, Size 616	
L (three Buck channels in parallel)	744383560068HT	Würth Elektronik	680 nH, 9.2 mΩ, 8.1A, Size L5.40 mm x W5.40 mm	
	XGL3530-601MEC	Coilcraft	600 nH, 6.9 mΩ, 14.7A, Size L3.5 mm x W3.2 mm	

Table 5-1. Recommended External Components for MCP16701 (continued)

Item	Part Number	Manufacturer	Description	Notes
L (four Buck channels in parallel)	SPM4020T-R47M-LR	TDK Corporation	470 nH, 11.8 mΩ, 8.7A, Size L4.4 mm x W4.1 mm H2.0 mm	
	744393230047	Würth Elektronik	470 nH, 6.69 mΩ, 14.5A, Size L4.3 mm x W4.3 mm	
	XGL4018-471MEC	Coilcraft	470 nH, 11A, 6.1 mΩ, 20%, Size 1616	

5.2 Switching Frequency Oscillator with External Synchronization

The MCP16701 dedicated synchronizable oscillator generates the switching frequencies and phases for all DC-DC channels.

In free-running mode, the oscillator frequency is nominally 8 MHz (supporting selectable 4-phase operation of the Bucks). Each Buck runs at 2 MHz, and its turn-on switching can be programmed to 0°, 90°, 180° or 270°phase-shift.

The oscillator always starts on its own free-running frequency. In the absence of external frequency synchronization fed at SYNC, FSD[1:0] bits may shift the oscillator's free-running frequency as soon as the volatile registers become operational. Until then, FSD[1:0] = 00.

The oscillator can be externally synchronized to an external clock fed at pin SYNC. This clock will typically be generated by a GPIO of the FPGA/MPU or the housekeeping MCU and could also be spread-spectrum modulated.

As soon as the SYNC signal is detected, the oscillator frequency is locked to the SYNC frequency. Therefore, the external synchronization used in the MCP16701 falls into the category of PLL-based techniques.

When the SYNC signal disappears, the PLL filter is slowly reset, and the controlling voltage for the oscillator frequency seamlessly decays towards the free-running value.

The oscillator can also provide an optional external synchronization output signal with a programmable divider ratio (referred to the switching frequency i.e., 2 MHz) at pin SYNCO.

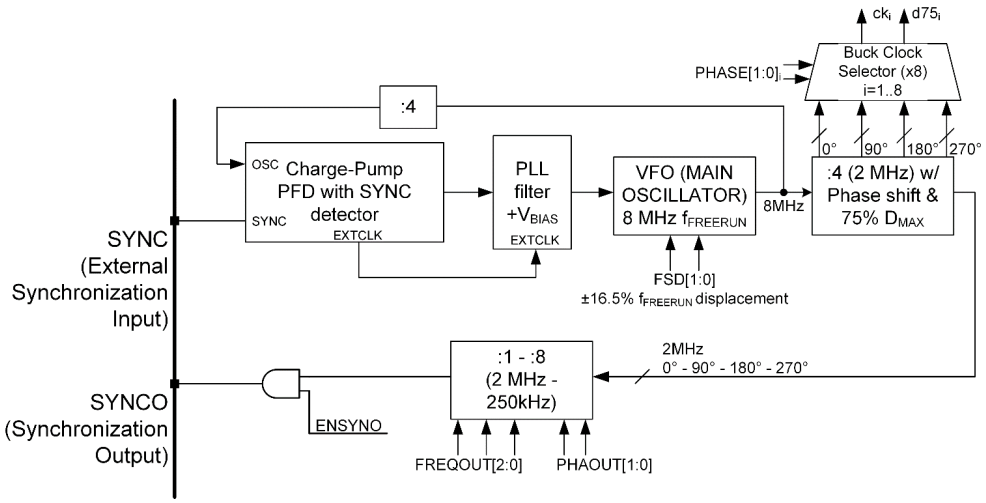
The dividing ratio is programmable through bits FREQOUT[2:0] from 1:1 to 1:8.

The purpose of the SYNCO output is to synchronize a front-end DC-DC converter. The phase displacement of the SYNCO signal is also programmable with bits PHAOUT[1:0].

When externally synchronized, there are no restrictions on the lock-in time delay and the operating current of the oscillator.

When synchronized at pin SYNC, all Buck converters will be forced into FPWM mode, regardless of the MODE pin or NVM_MODEB/MODEB bits.

Figure 5-1. Synchronization Concept.



5.3 Soft-Start, DVS and Considerations

The Bucks and the LDOs' output voltage settings have a non-uniform step size (12.5 mV/25 mV).

When the output voltage is dynamically changed from one level in the 12.5 mV/step region to another level in the 25 mV/step region (or vice-versa), the output change will take place at 12.5 mV/step in the corresponding region, but using twice the update rate for the reference.

By doing this, there will be no slope changes (on average) when crossing the boundary between the 12.5 mV/step and 25 mV/step regions.

This applies during soft-start and DVS changes.

The figures below illustrate the concept:

Figure 5-2. Soft-Start and Shutdown

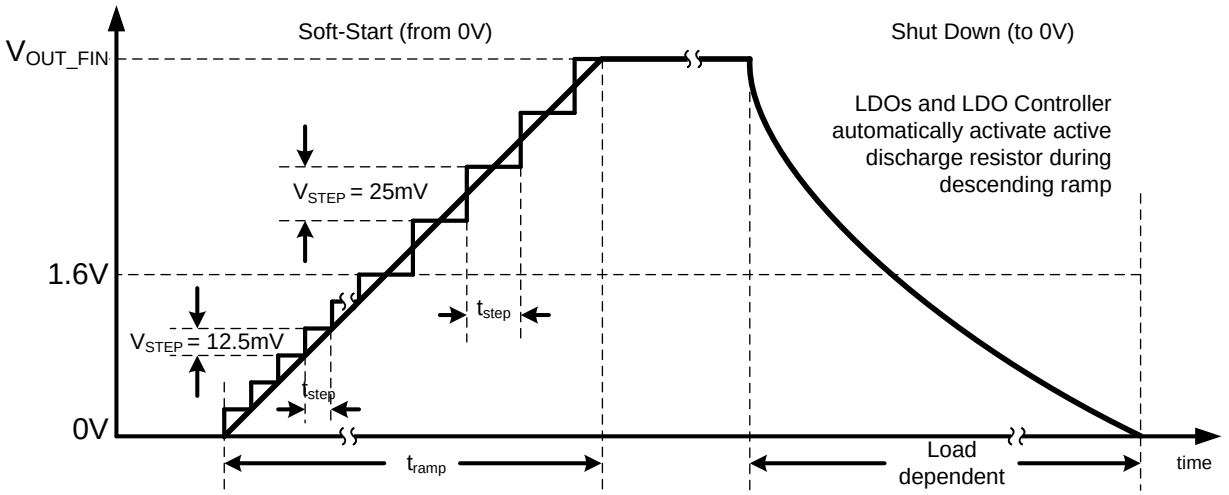
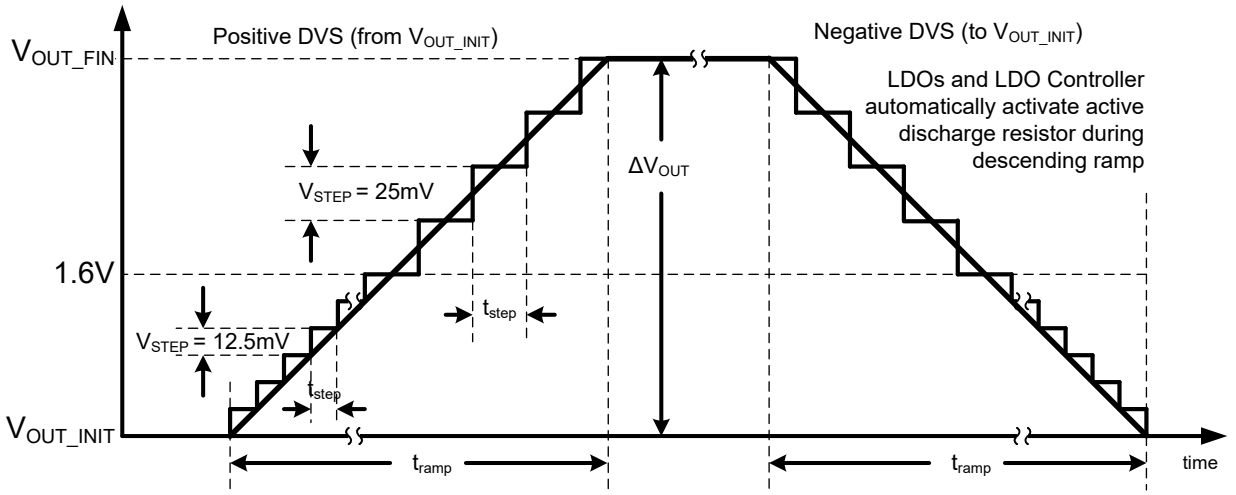


Figure 5-3. DVS



The soft-start rate is programmable through bits ONSR[2:0], as shown in Soft-Start Programming Bits ONSR[2:0]. The time base for tstep is generated by the digital 8 MHz oscillator and it is not related to the switching frequency.

The DVS rate is programmable through bits DVSSR[1:0]. The same rate applies to both positive and negative DVS transitions, and its programmability is shown in DVS Rate Programming DVSSR[1:0]. While the DVSR on the LDOs and LDOC can be done at no load, in case of the Bucks, there is a recommended minimum load of 25 mA for best performance.

5.4 Directly Paralleled Replica Configuration - Parallel Broadcasting

To avoid propagation delays inherent in a daisy-chain approach, a dedicated logic block managing an assigned group of Buck channels provides to each paralleled channel (including the MAIN) with the turn-on command such that the signal reaches all the gate driving stages with virtually no skew or delays. The turn-on command is generated based on the request from the MAIN PWM logic and the Mr setting bits for the assigned group of Buck channels.

For the MCP16701, the 8 available Buck channels are divided into two groups (Buck1 to Buck4 on the left side, and Buck5 to Buck8 on the right side). The MAIN-replica logic is designed to manage 4 Bucks. For a given channel defined as MAIN, only subsequent channels can be connected as replicas. Therefore, Buck1 and Buck5 can never be replicas (Mr bit of Buck1 and Buck5 are hardwired to HIGH), and Buck4 and Buck8 can never be a MAIN for a subsequent replica (only independent).

In the main-replica operation, all power stages are directly connected in parallel (all SW nodes are connected together).

If a Buck is configured as a main (Mr = '1' and a power cycle is completed after setting this bit) driving one or more replicas, **the power train components (inductor and output capacitor) shall be scaled with the number of paralleled power stages**. Typical application presents an example for component scaling of two stand-alone Buck configurations (Buck7 and Buck8); two parallel Buck configurations (Buck5 and Buck6), and four parallel buck configurations (Buck 1, 2, 3, 4).

5.5 Slope Compensation

Slope Compensation bits will affect the response of the regulator when a load transient is applied.

If a Buck is configured as a main (Mr = ‘1’) driving one or more replicas, and the power train components (inductor and output capacitor) are scaled with the number of paralleled power stages, the regulation loop frequency compensation does not need to be changed, nor does the slope compensation.

If you are unsure about how changing the slope compensation will affect your design, leave the value at the default ‘00’ .

The default slope compensation value can be changed by the user using bits NVM_SLPSEL[1:0]/ SLPSEL[1:0] as follows.

Table 5-2. Slope Compensation Selection bits SLPSEL [1:0]

SLPSEL[1:0]	Slope Compensation
00	Default value – calculated for dead-beat slope compensation with L = 1.5 µH
01	Slope compensation is half of the default value
10	Slope compensation is double the default value
11	Slope compensation is disabled (no slope compensation)

5.6 Thermal Shutdown Protection and Warning

The MCP16701 Thermal Shutdown protection is generated by the main temperature sensor, powered from the AVCC rail. As such, the Thermal Shutdown protection won't be active when the VDD is the only power supply applied to the MCP16701 during EEPROM initial configuration.

Thermal Shutdown Protection will immediately terminate power delivery on all power channels when the die temperature exceeds the upper Thermal Shutdown threshold. As a consequence, nRSTO_A and nRSTO_P will both be asserted (i.e. they go LOW).

Upon Thermal Shutdown trigger, all channels will be immediately turned off .

Default values stored in EEPROM will NOT be reloaded upon Thermal Shutdown.

When the die temperature decreases below the lower Thermal Shutdown threshold (hysteresis = 20°C) and after an additional 100 ms cool-down time, if EN is still HIGH at the end of the 100 ms, the MCP16701 will attempt to resume operation as programmed in the volatile registers.

Thermal Shutdown Protection and Warning is also responsible for the generation of Thermal Early Warning (TWR).

The Thermal Early Warning threshold is programmable via the TWRTH bit in two different values: 125°C (TWRTH = '0') and 135°C (TWRTH = '1').

When die temperature exceeds the programmed Thermal Early Warning threshold, the TWR bit will be set. nINTO will be asserted unless TWR is masked (TWRMSK = '1').

5.7 WDI/nWDO Watchdog Timer Modes

1. WDI/nWDO Watchdog Timer (NVM_WDMODE = '0')

This is the simplest Watchdog Timer implementation, selected with bit NVM_WDMODE = '0'.

In this mode, WDI is an edge-sensitive input driven by a GPIO of an MCU, and nWDO is an open-drain output which will be asserted LOW upon timeout expiration. It can also be used for reset generation for the host.

The assertion of nWDO is totally independent of the operation of the power channels, which will continue operating regardless of the nWDO assertion.

A falling edge transition on the WDI pin is required to first start the timeout count.

The WDI input cannot respond until the EN pin has started the MCP16701.

The WDI input can also be made insensitive to transitions until nRSTO_P or nRSTO_A are deasserted, depending on the bit WDRPEN, such that spurious glitches during reset on the GPIO driving the WDI input are rejected.

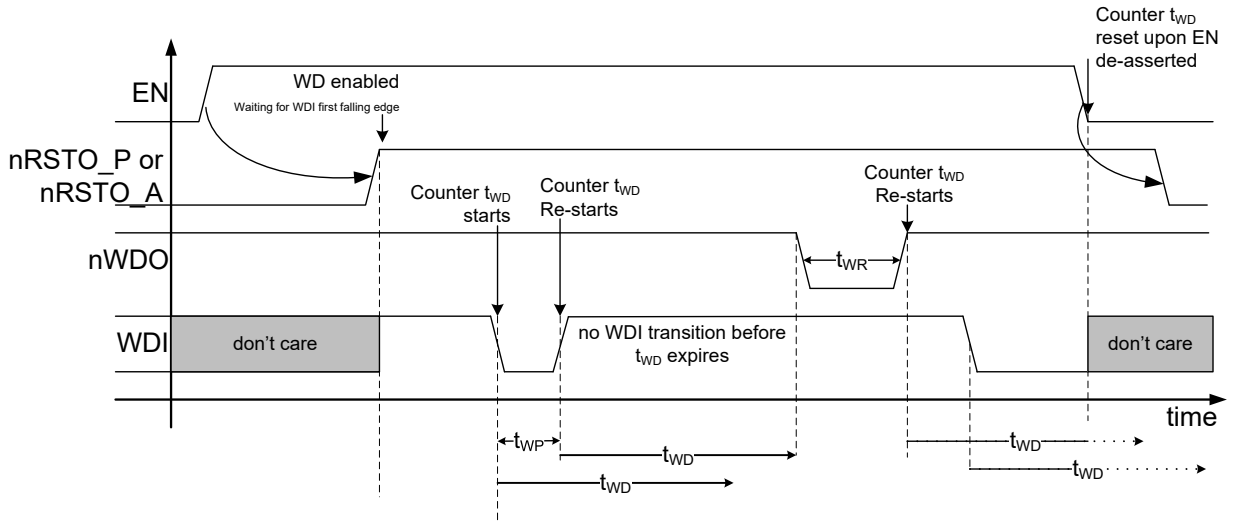
If the WDI input does not toggle within the Watchdog Time-out delay t_{WD}, the nWDO output will be pulled low for a user-programmable duration t_{WR}. The minimum pulse width (t_{WP}) for a WDI status change to be captured is 140 ns (constraint due to 8 MHz digital clock and its tolerance).

The Watchdog Time-out delay is programmable by bits WDTOD[2:0].

The nWDO pulse width is user-programmable by bits WDRSP[1:0].

If a WDI edge transition is detected on the WDI input while nWDO is asserted LOW, the nWDO assertion pulse t_{WR} is terminated and the time-out delay counter t_{WD} is immediately restarted.

Figure 5-4. Watchdog Timer Timing Diagram (NVM_WDMODE = '0').



WDI input should not be left floating, especially after the deassertion of nRSTO_P/nRSTO_A. If the GPIO driving the WDI input cannot be set to a known logic state during reset, then a small (100 kΩ) pull-up resistor to VDD is recommended. Driving WDI through an open-drain output with a small pull-up resistor is also possible.

The watchdog timeout can also be windowed using bit WDWNDW. If WDWNDW = '0', the WDI transition is considered valid at any point during the t_{WD} programmed by the WDTOD[2:0] timer. If WDWNDW = '1', the WDI transition will be considered valid only if it happens in the second half of the t_{WD}.

Whenever the Watchdog Timer is counting, bit WD_CLEAR is automatically set to '1'. This enables the host to verify that the Watchdog Timer is indeed counting.

2. Interface-cleared Watchdog Timer with WDI transitions count and hardware reset and restart (NVM_WDMODE = '1')

This mode is selected by setting NVM_WDMODE = '1'.

In this mode, it is assumed that the WDI pin is toggled LOW because of the expiration of an embedded (host) Watchdog Timer.

This event is counted as a host watchdog time-out failure event and generates an increment of the watchdog event counter WD_CNT[3:0]. The WD_CNT[3:0] counter is only active for NVM_WDMODE = '1'.

A Watchdog Timer is provided by the MCP16701 also in this mode of operation. The watchdog time-out delay is the same as for NVM_WDMODE = '0', i.e. the same WDTOD[2:0] time-out delay programming applies.

However, the time-out delay reset mechanism is different.

As soon as the watchdog timer starts counting (after the deassertion of nRSTO_P or nRSTO_A depending on WDRPEN bit), the WD_CLEAR bit in the corresponding status register is set.

The host must access the WD_CLEAR bit through the I^2C interface within the valid time window (WDWNDW bit windowing applies) and rewrite a '1' into WD_CLEAR.

If this happens, the WRITE is interpreted as a successful watchdog refresh and the watchdog time-out delay timer gets reset. The successful watchdog refresh causes the WD_CNT[3:0] counter to be decremented by 1 (note: the WD_CNT[3:0] counter can't be decremented below zero).

If the host does not rewrite WD_CLEAR within the time-out delay and/or misses the valid window, the WD_CNT[3:0] counter gets incremented by 2.

The time-out delay counter is immediately re-started after the expiration of the previous time-out delay count.

Therefore, the watchdog event counter can be incremented in two ways:

1. The WDI pin toggles LOW due to a host (MPU/FPGA) watchdog failure: **increment by 1;**
2. The watchdog time-out delay counter reaches its EOC without a WRITE operation performed by the host onto WD_CLEAR bit within the valid time window: **increment by 2.**

Both ways are active at the same time, i.e. executed as parallel branches in the flowchart depicted in Figure 5-5.

The WD_CNT[3:0] is decremented by 1 upon a successful watchdog refresh (rewrite of WD_CLEAR), and can be also cleared by the host by over-writing the WD_CNT[3:0] content.

The WDI transitions count and internal watchdog timer time-outs can also be disabled individually, such that the only one of the WD_CNT[3:0] increment mechanisms can be activated. These are controlled by the WDI_DIS and WDT_DIS bits.

WDI_DIS = '1' means the WDI transitions count is not causing any increment of WD_CNT[3:0].

WDT_DIS = '1' means the internal watchdog timer is disabled, and it cannot generate any increment. WD_CLEAR will remain at '0'.

Setting both WDI_DIS = '1' and WDT_DIS = '1' is equivalent to WDEN = '0'.

The purpose of the WD_CNT[3:0] counter is to ensure no permanent cyclic watchdog condition occurs. Bit-field WD_CNT_MAX[3:0] is provided such that the user can put a limit on the number of watchdog time-outs (either internal or embedded in the host).

If WD_CNT[3:0] reaches WD_CNT_MAX[3:0], that means the software is stuck and the host has become unresponsive, in spite of the presence of an embedded watchdog.

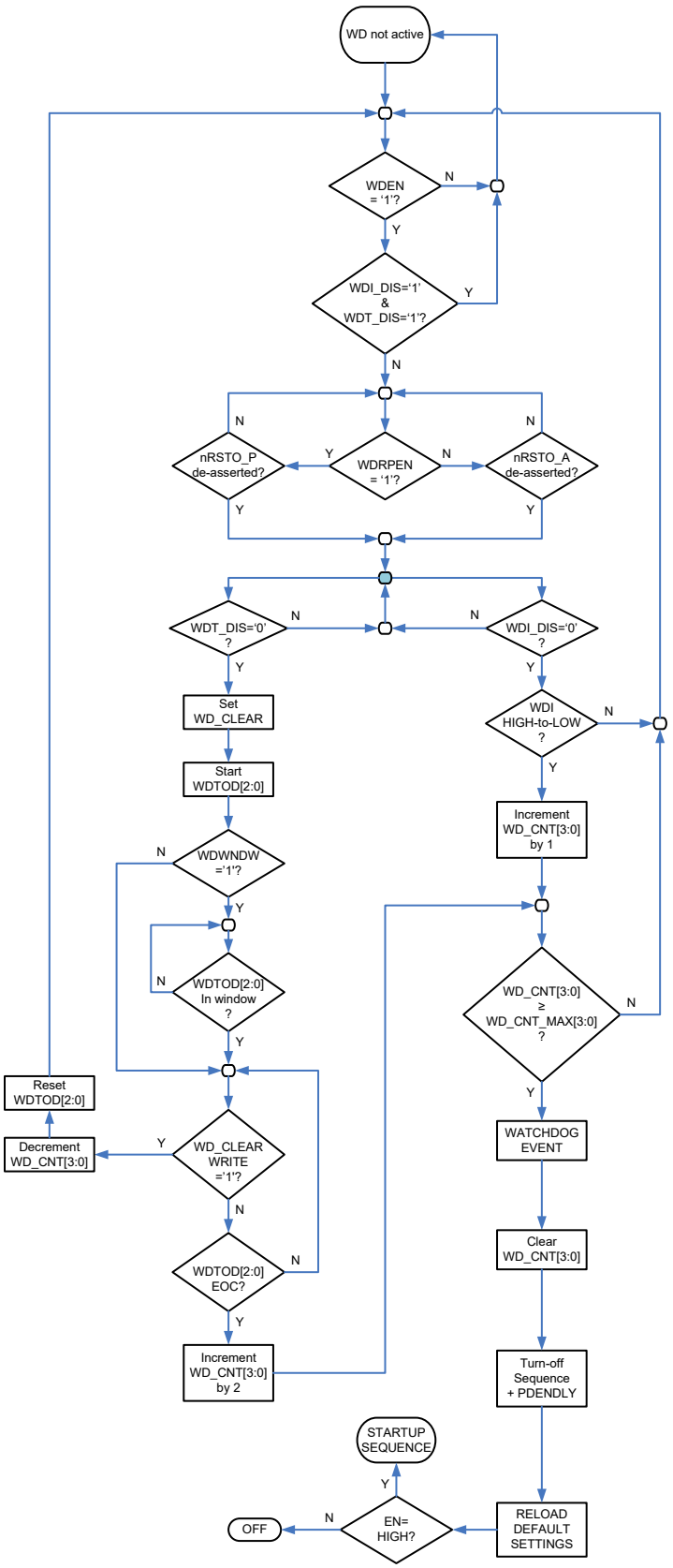
Therefore, a watchdog event is declared, and a full hardware reset and restart is generated. Then:

1. The MCP16701 automatically executes a turn-off sequence (no need to deassert EN). Signals nRSTO_A, nRSTO_P and GPO will be asserted/deasserted as programmed in the turn-off sequence.
2. After the completion of the turn-off sequence and the power-down enable delay PDENDLY[2:0], the MCP16701 **reloads the default configuration from the EEPROM.** The time it takes to reload the default configuration is effectively added to the PDENDLY.
3. If EN is still high at the time the default configuration reload has completed, the MCP16701 initiates a new turn-on sequence.

The WD_CNT[3:0] counter is also cleared after triggering the watchdog event.

In the MCP16701, there is no limit on the number of hardware resets and restarts caused by watchdog events.

Figure 5-5. Watchdog Flowchart for NVM_WDMODE = '1'.



5.8 Overcurrent Protection (Buck Channels)

The overcurrent protection for MCP16701 consists of a cycle-by-cycle, high-side current limit with digital filtering, followed by a hiccup mode for protection against short-circuits conditions. **Hiccup can be disabled by the user by setting bit DISHCP = '1'; however, it is strongly recommended that the DISHCP bit is set to 0 (Hiccup mode overcurrent protection enabled).**

The cycle-by-cycle, high-side current limit includes frequency fold-back. Because of Leading-Edge-Blanking in peak-current-mode control, frequency fold-back (with a factor = 4) is used to allow more time for inductor discharge and prevent current runaway in deep overload condition.

Frequency fold-back operation is entered when:

1. A high-side current limit event has been detected;
2. The feedback voltage is less than 500 mV (typical).

Cycle-by-cycle overcurrent protection with frequency fold-back is always active, and it is the first current limit protection mechanism.

The second current limit mechanism is hiccup mode protection, which is enabled by default (DISHCP = '0'), including during the soft-start ramp and DVS transitions. DISHCP = '1' disables the hiccup mode protection.

If hiccup mode protection is active, there will be a limitation on the maximum simultaneous DC and capacitive loading to ensure that the hiccup mode protection will not be engaged during the soft-start ramp.

Hiccup is invoked based on digital counting of high-side overcurrent (HS OC) events, regardless of the frequency at which they take place (full switching frequency or fold-back switching frequency).

Each time the overcurrent protection detects a high-side current limit event, the current ON time is terminated and a HS OC Event counter is incremented. The length of the HS OC Events counter is 4-bits.

The HS OC Events counter can be reset during run time **in two ways:**

1. After 15 consecutive HS turn-on pulses without any overcurrent event. This counting is done by the RESET counter. Note that all counting is switching-event based, so it is not relevant if the switching takes place at fsw or at fsw/4 (i.e., in frequency fold-back). This is the only possible method if DISHCP = '1'.
2. Upon reaching EOC and entering hiccup mode, if DISHCP = '0'. The reset of the HS OC Events counter may take place at any time during the hiccup dwell time, e.g., at the end of the dwell time and just before initiating a new soft-start retry.

If DISHCP = '0' and the HS OC Events counter reaches/has reached its EOC and the instantaneous value of POK signal is/goes LOW, the Buck converter enters Immediate OFF mode, and hiccup mode protection is triggered (flag HICCUP = '1' and ILIM = '1'). This will generate a FAULT (hiccup Fault).

If DISHCP = '1' and the counter reaches its EOC and the instantaneous value of the POK signal is/goes LOW, the converter will continue to operate, relying only on cycle-by-cycle current limiting. The ILIM flag will be asserted (not the HICCUP flag) and this event will also generate a FAULT (current limit Fault). The converter will remain in current limit Fault (i.e. ILIM = '1') until the HS OC Counter is reset by the RESET counter.

The FAULT (hiccup Fault or current limit Fault for Bucks, or any other Fault) on any of the power channels (except the LDO Controller) can have different behaviors, depending on the DISINTFLT, DISRSTFLT, and ENRSRFLT bits of the corresponding channel.

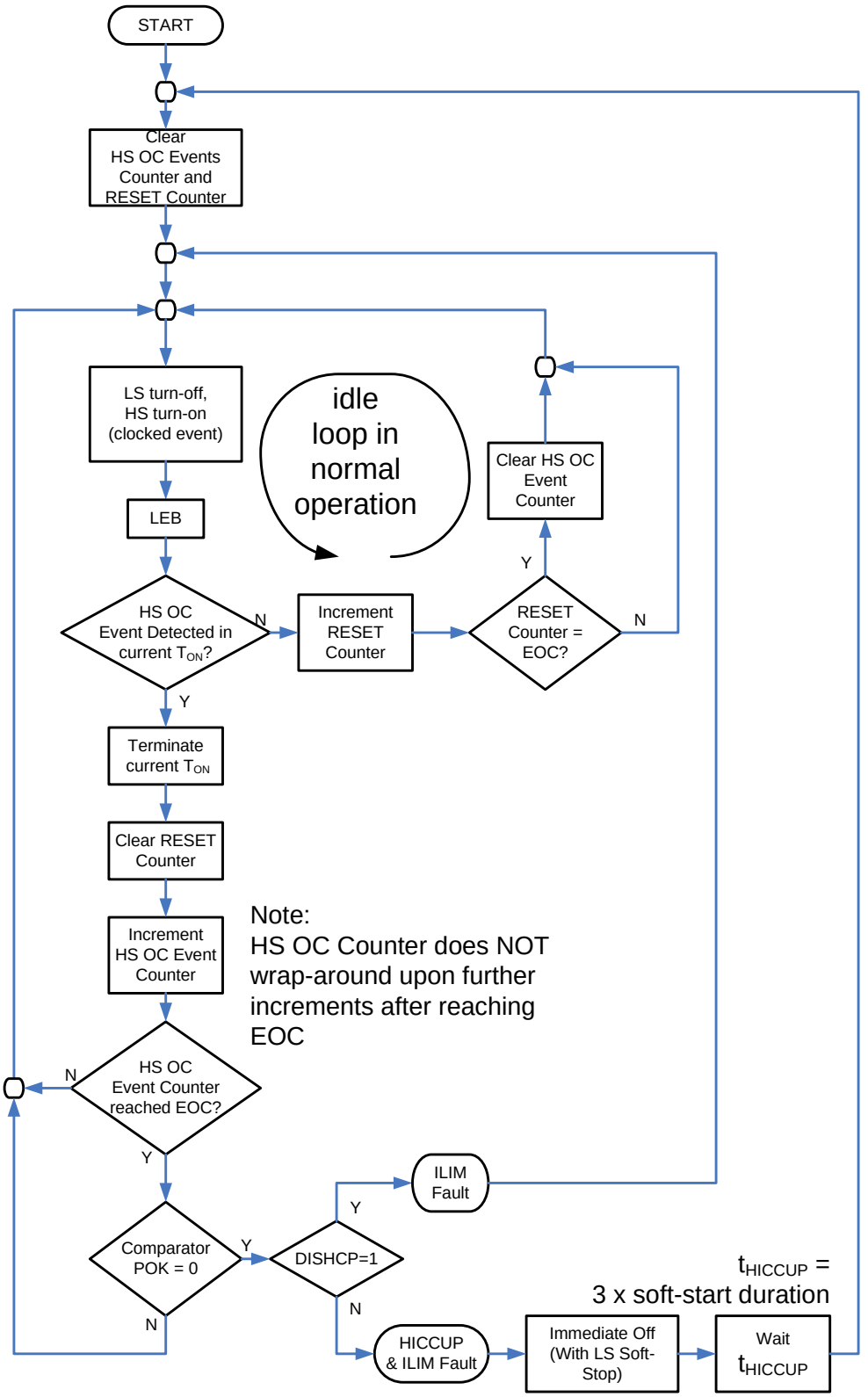
Assuming ENRSRFLT = '0', after entering hiccup through Immediate OFF, the responsible channel will be kept off for a certain hiccup time (t_{HICCUP}), which corresponds to 3x soft-start time on that

channel. After the hiccup time, a new soft-start is attempted. The Buck channel will continue to operate in this condition until the overload is removed.

If the overload condition is removed and the affected channel resumes normal operation (POK returns HIGH), nRSTO_A and (if applicable) nRSTO_P will be deasserted after their programmed reset delay (nRADLY[3:0] and nRPDLY[3:0] bits).

The Buck overcurrent protection flowchart is detailed below:

Figure 5-6. Hiccup Protection Flowchart



5.9 Output Current Limiting (LDOs)

LDOs feature a brick-wall linear current limit, which is also active in Load Switch mode (FBYPM = '1').

When the current limit is engaged, the ILIM flag is set in the corresponding LDO status register.

Engaging the current limit on an LDO output does not necessarily invoke a FAULT. The LDO must also be outside of soft-start and/or not performing positive DVS transitions, and POK must also go LOW.

5.10 LDO Controller Overcurrent

Overload protection for the LDO Controller channel is supported by the Buck channel, which powers the input of the LDO Controller (external MOSFET drain). The LDO Controller does not have any autonomous overcurrent protection.

For safety and robustness against short-circuits on the LDO Controller output, the hiccup mode protection of the Buck feeding the LDO Controller should never be disabled; otherwise, excessive power dissipation across the external MOSFET or permanent damage may result.

5.11 Power Channels Fault Definitions and Fault Management

5.11.1 Fault Definitions for Power Channels

For Buck converters the definition of a FAULT event is:

FAULT = Mr and [(not(DISHCP) and HICCUP) or (DISHCP and ILIM and not(POK) and SSDONE)

When a Buck channel is a replica and has Mr = 0, it will never generate a Fault event.

For LDOs, the definition of a FAULT event is

FAULT = (ILIM and not (POK) and SSDONE)

5.11.2 Fault Management

The subsequent behavior after the occurrence of a FAULT on a certain power channel depends on the bits setting of ENRSRFLT, DISRSTFLT, and DISINTFLT for that channel.

ENRSRFLT: Enable Restart on FAULT bit. If ENRSRFLT = '1', a FAULT on the channel will cause an immediate OFF of ALL channels currently ON, then invoke an automatic Restart sequence of enabled channels after a 100 ms delay.

The nRSTO_P/_A resets will be automatically asserted (with no delay) as a consequence of the simultaneous immediate OFF of all channels. It is relevant only if Mr = '1' for Bucks.

DISRSTFLT: Disable Reset on FAULT bit. For a channel having ENABLE = '1', this bit disables automatic nRSTO_A and/or nRSTO_P deassertion upon channel FAULT during run time.

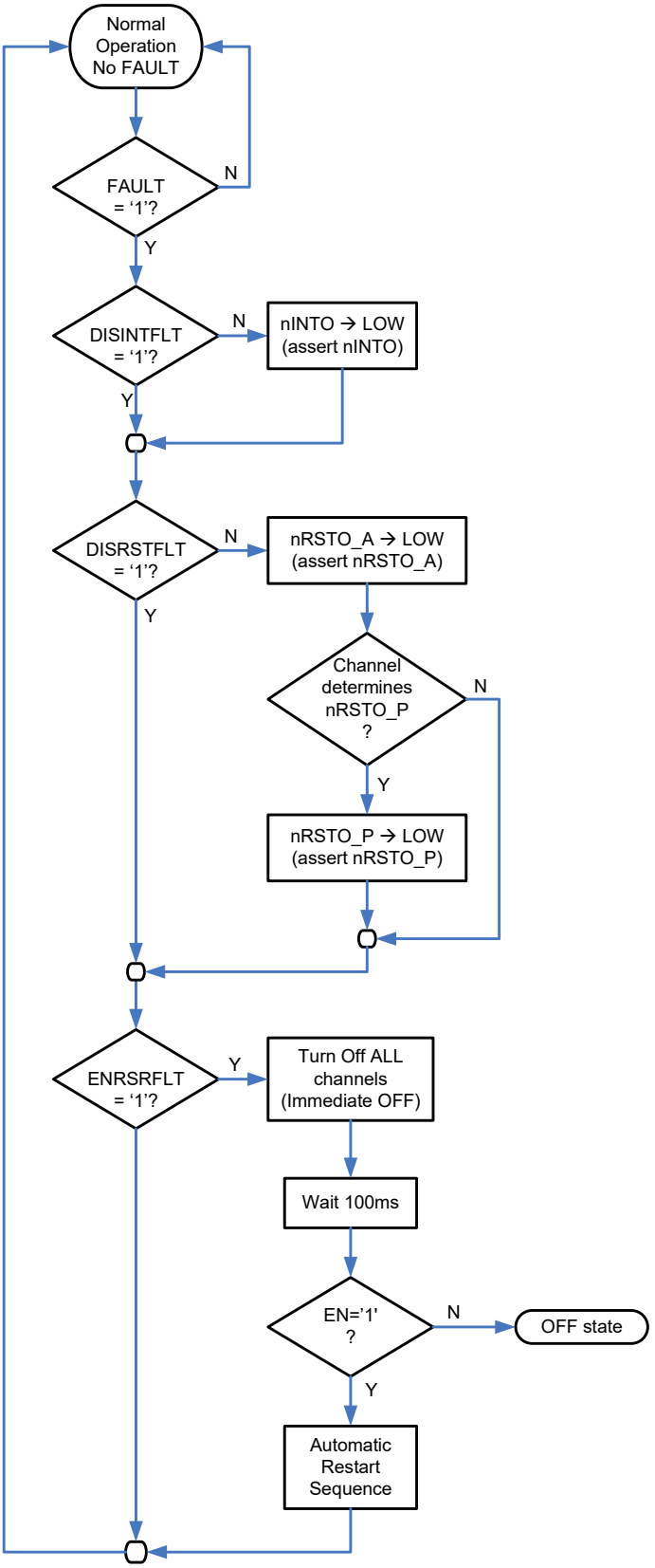
If ENABLE = '0', the channel is not part of the start-up sequence and therefore does not affect the deassertion on nRSTO_P/nRSTO_A.

If a channel having ENABLE = '0' at POR is later turned on through the interface by setting ENABLE = '1' after the deassertion of nRSTO_A/nRSTO_P, and the user wants to prevent assertion of nRSTO_A/nRSTO_P upon FAULT on that channel, it is also necessary to set DISRSTFLT = '1' concurrently. It is relevant only if Mr = '1' for Bucks.

DISINTFLT: Disable Interrupt on FAULT bit. This bit disables automatic nINTO assertion upon channel FAULT during run time. It is relevant only if Mr = '1' for Bucks.

The flowchart below illustrates the actions executed when a FAULT occurs on a certain power channel, depending on the values of bits DISINTFLT, DISRSTFLT and ENRSRFLT. In order to experience a FAULT event, the channel must be enabled (ENABLE = '1') and in the case of Buck converters it must be operating either as a MAIN or in independent mode (Mr = '1').

Figure 5-7. Fault Management Flowchart



5.12 LDO Controller External MOSFET Selection

The LDO Controller is intended to drive an external N-channel MOSFET. Possible external MOSFETs Q1 for the LDO Controller are listed in the table below:

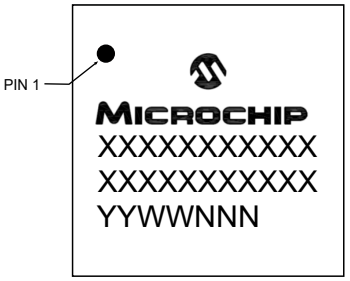
Table 5-3. Discrete MOSFETS for the LDO Controller

Q1 Part Number	Manufacturer	BVdss (V)	Vth (V) MIN-MAX	Rds(ON)_MAX @ Vgs	Rated Id (A)	Rated Vgs (V)	Package	RthJA °C/W
SiUD412ED	Vishay	12	0.35-0.9	0.55Ω @ 1.8V	0.5	±5	0.8 mm x 0.6 mm xQFN	80
Si8806DB	Vishay	12	0.4-1	75 mΩ @ 1.8V	3.2	±8	0.8 mm x 0.8 mm BGA	105
SiA436DJ	Vishay	8	0.35-0.8	12.5 mΩ @ 1.8V	12	±5	2.05 mm x 2.05 mm xQFN	28
SiAA02DJ	Vishay	20	0.6-1.6	16.2 mΩ @ 2.5V	18	+12/-8	2.05 mm x 2.05 mm xQFN	28
SiSH106DN	Vishay	20	0.6-1.5	9.8 mΩ @ 2.5V	19.5	±12	3.3 mm x 3.3 mm xQFN	24

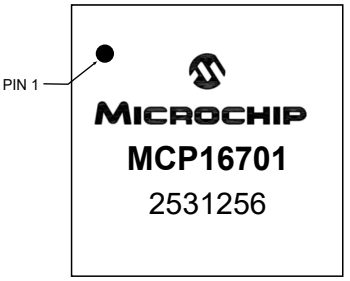
6. Package Information

Package Marking Information

64-Lead VQFN (8x8x0.9 mm)



Example:

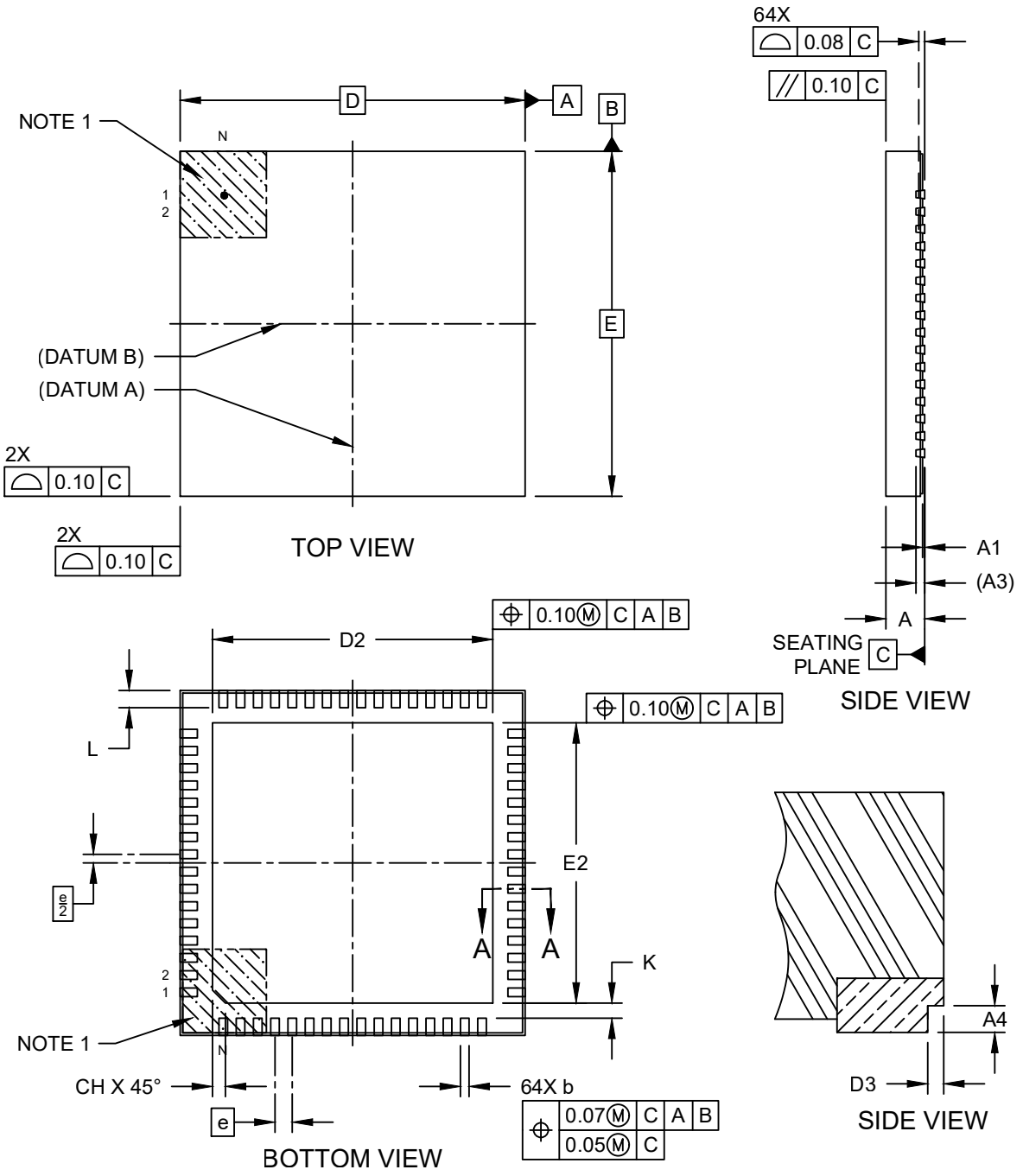


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

64-Lead Very Thin Plastic Quad Flat, No Lead Package (KCX) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

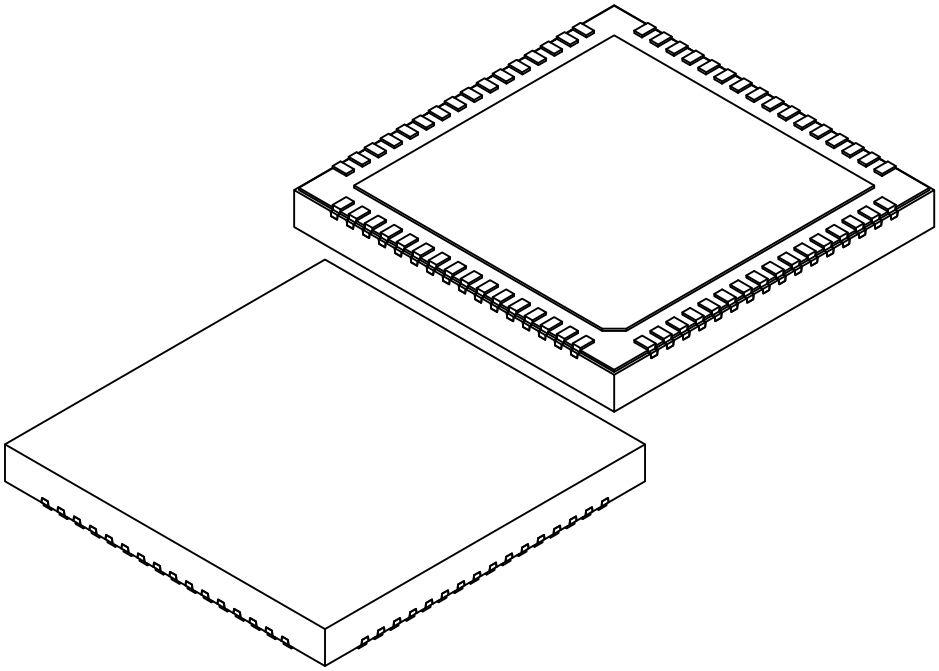
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00479 Rev C Sheet 1 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (KCX) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.40 BSC	
Overall Height	A	–	–	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.40	6.50	6.60
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.40	6.50	6.60
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	–	–
Step Height	A4	0.10	–	0.19
Step Length	D3	–	–	0.085
Index Corner Chamfer	CH	–	0.30	–

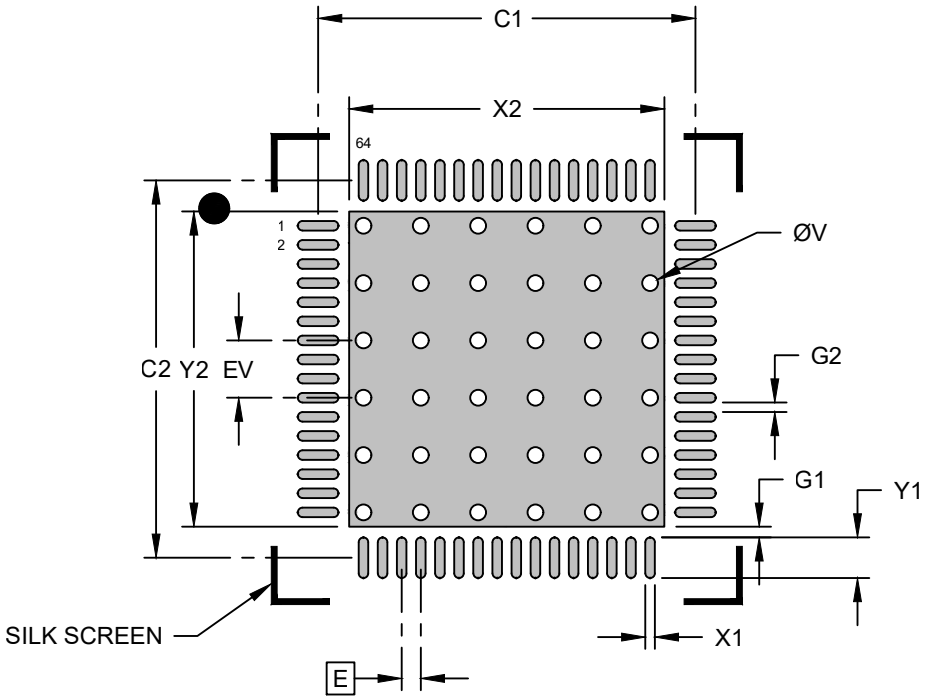
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00479 Rev C Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (KCX) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X64)	X1			0.20
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

Microchip Technology Drawing C04-02479 Rev C

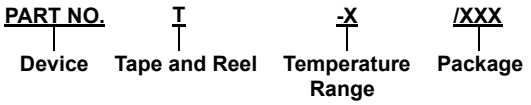
7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	03/2025	Initial release of this document.

8. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	MCP16701: High-performance, High-accuracy PMIC	
Tape & Reel Option:	(Blank)	= Tube
	T	= Tape & Reel (1000/Reel)
Temperature Range:	I	= -40°C to +85°C (Industrial)
Package:	KCX	= VQFN, Very Thin Fine Pitch Quad Flat No Lead, 64-Lead, 8x8x0.9 mm

Examples:

- MCP16701T-I/KCX: High-performance PMIC, Industrial temperature, VQFN package, Tape and Reel

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

9. Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-0791-2

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.