# 200 mA High-Voltage Automotive LDO

## MCP1781

## Description

The MCP1781 is a high-voltage, Low Drop-Out (LDO) regulator, capable of supplying 200 mA of output current. The input voltage range of 4.0V to 55V makes it suitable for 12V to 48V power rails, such as those found in high-voltage battery packs, or automotive applications where it can maintain regulation through large transients, including load dump events.

A low UVLO of 2.3V makes it adequate for cold cranking conditions in automotive applications.

The MCP1781 offers two standard fixed output voltage versions, 3.3V and 5.0V, and an adjustable output option, with a voltage range from 1.3V to 5V. The regulator output is stable with a 3.3 µF ceramic capacitor. The device is protected from short-circuit events by the current foldback function and from overheating by means of thermal shutdown protection.

Two 5-lead packages are available, SOT-223 and TO-252, both with a PWG/ADJ pin (PWG for the fixed version and ADJ for the adjustable version) and a $\overline{\text{SHDN}}$ pin. While in shutdown, the quiescent current drops to 3.5 µA, allowing for lower overall power consumption. The device itself has a ground current of 85 µA (typical) when delivering maximum output current of 200 mA.

## Features

- AEC-Q100 Automotive Qualified (Grade 0, PPAP Capable)
- Wide Input Voltage Range: 4.0V to 55V
  - Undervoltage lock-out (UVLO): 2.7V typical
- Extended Junction Temperature Range: –40°C to +150°C
- Standard Output Regulated Voltages ($V_R$): 3.3V and 5.0V (Note)
  - Tolerance ± 2.0% over temperature
- Adjustable Output Voltage Range: 1.3V to 5V
- Open Drain Power Good Pin
- Low Quiescent Current: 34 µA Typical
- Low Shutdown Current: 3.5 µA Typical
- Output Current Capability: 200 mA Typical
- Short Circuit Current Foldback Protection
- Thermal Shutdown Protection: 169°C Typical
- Stable with Ceramic Output Capacitor: 3.3 µF
- High PSRR for $V_{IN}$ = 14.5V and $I_{OUT}$ = 100 mA:
  - –80 dB @ 100 Hz typical
  - –36 dB @ 100 kHz typical
- Available in 5-Lead TO-252 and 5-Lead SOT-223 Packages

**Note:** For other voltage options, contact your local sales office.

## Applications

- Automotive Electronics:
  - Body control modules
  - Instrument clusters
  - Infotainment systems
  - Always-on battery applications: door modules, remote keyless entry, immobilizer
- High-Voltage Battery Packs for Power Tools, E-Mobility for up to 10S Battery Packs

## Typical Application Circuit

**Figure 1.** Fixed Output Version

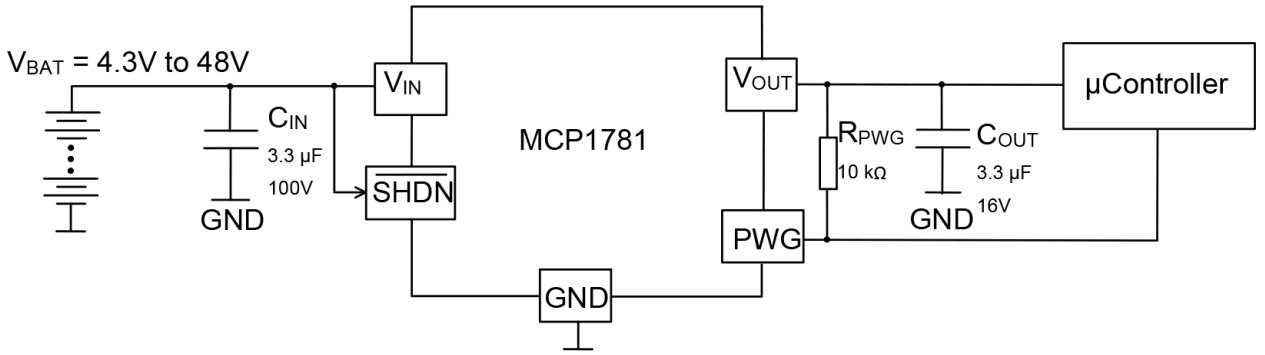
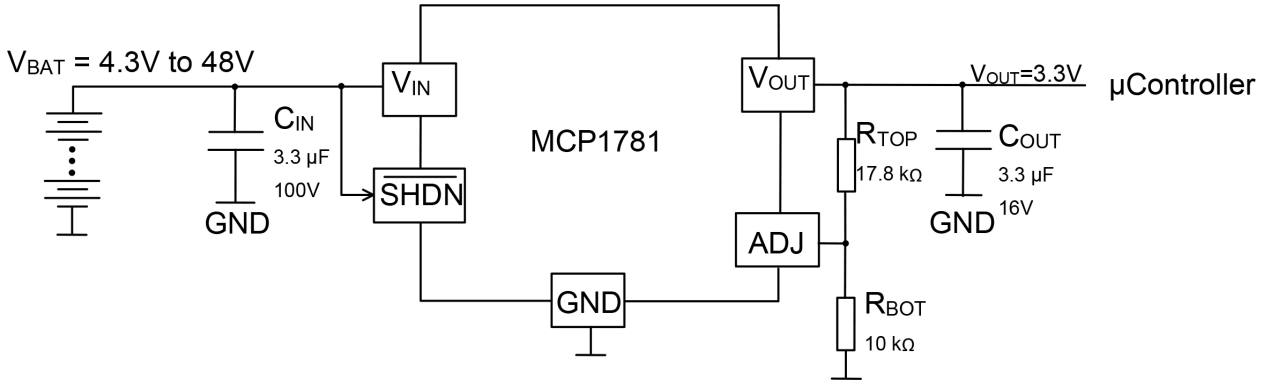



**Figure 2.** Adjustable Output Version



# Functional Block Diagram

**Figure 3.** Fixed Output Version

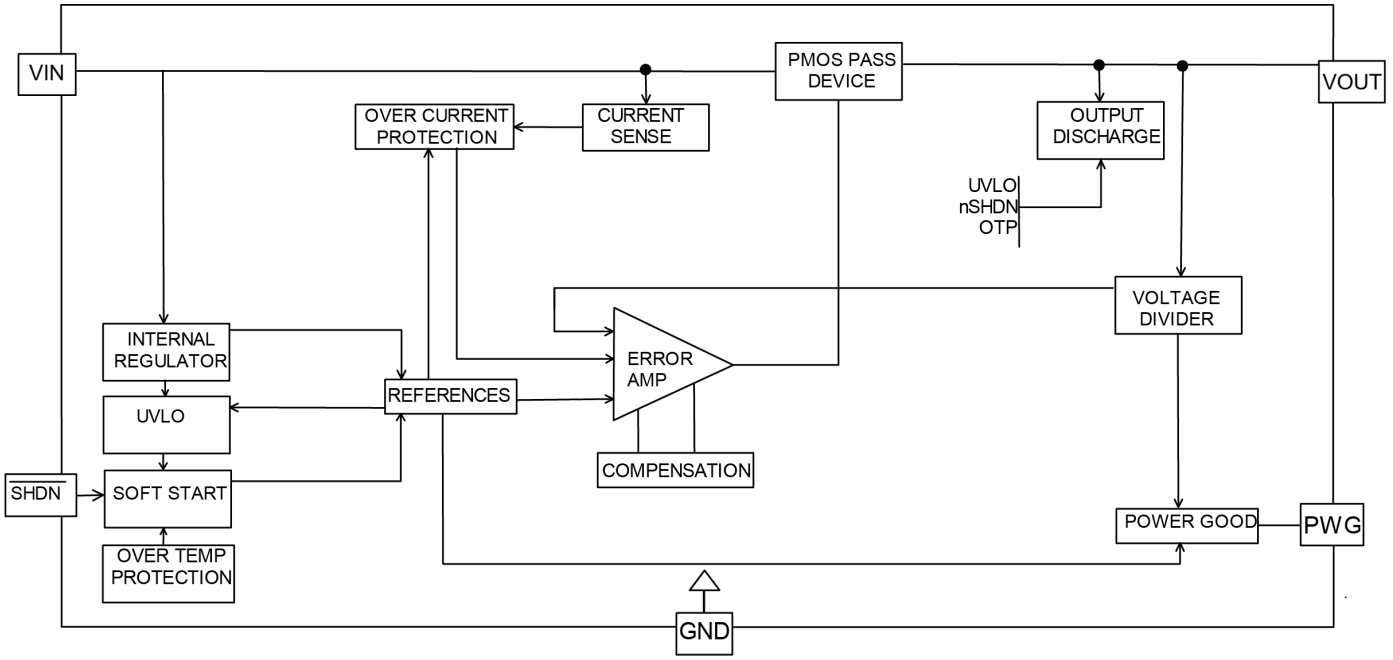
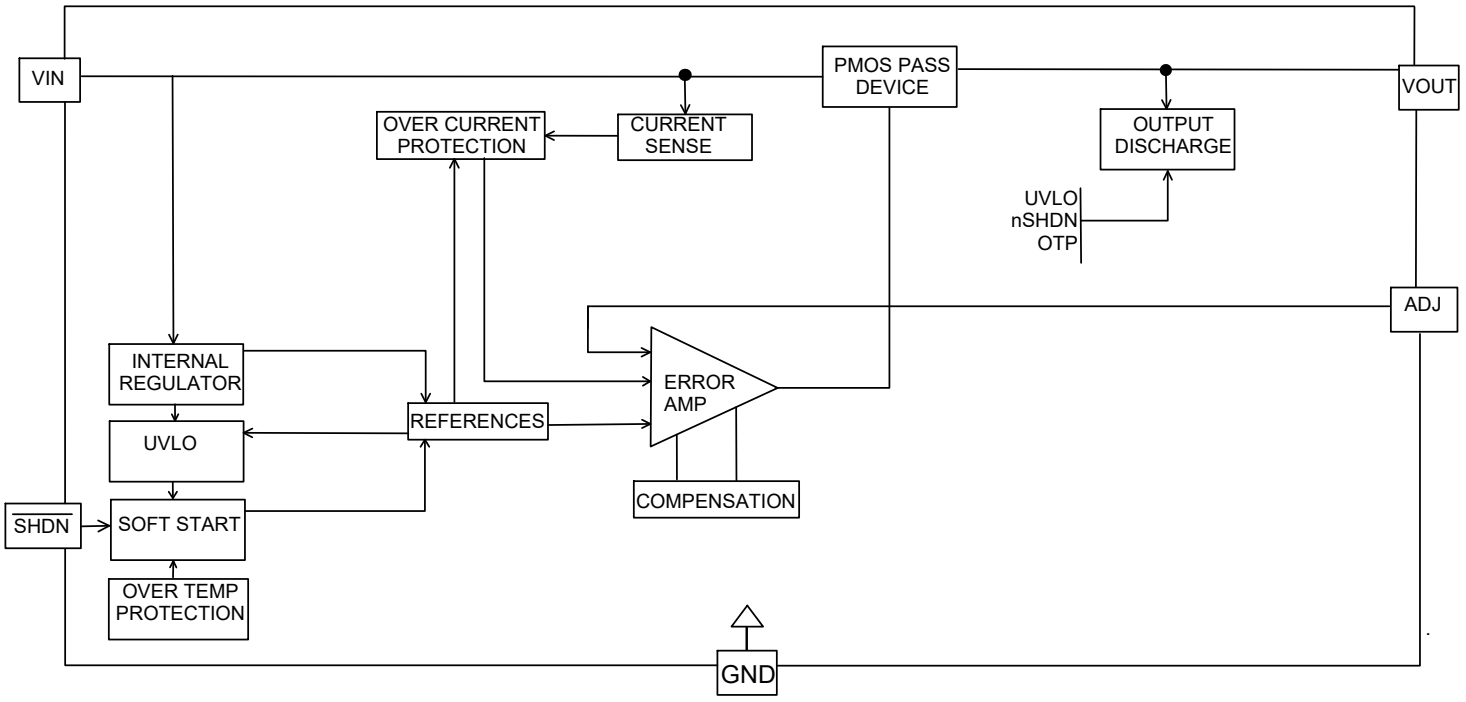



**Figure 4.** Adjustable Output Version



# 1. Pin Configuration

## 1.1. Pin Descriptions

**Table 1-1.** Pin Descriptions Table

| Pin Number (5-Pin SOT-223) | Pin Number (5- Pin TO-252) | Symbol | Description |
|---|---|---|---|
| 1 | 1 | $\overline{SHDN}$ | Shutdown Control Input. Do not leave this pin floating. |
| 2 | 2 | VIN | Input Voltage Supply |
| 3 | 3 | GND | Ground |
| 4 | 4 | VOUT | Regulated Output Voltage |
| 5 | 5 | PWG | Open-drain Power Good; actively pulled low when VOUT is below threshold (fixed output versions only). |
| | | ADJ | Voltage Sense Input (adjustable output version only) |
| 6 | 6 | Tab | Exposed Thermal Pad, connected to GND. |

## 1.2. Package Types

**Figure 1-1.** 5-Lead SOT-223 Package.

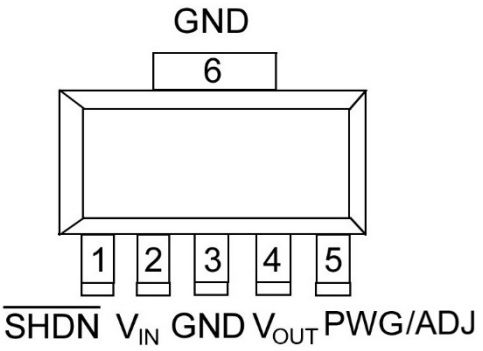
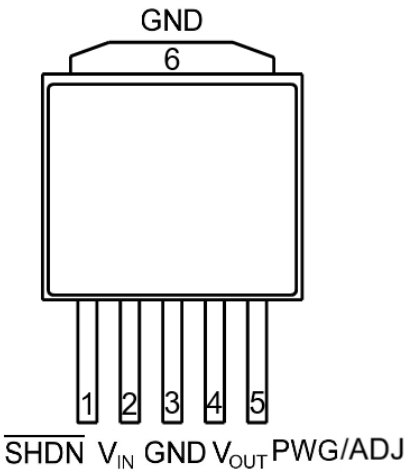



**Figure 1-2.** 5-Lead TO-252 Package.



## 1.3. Pin Details

### 1.3.1. Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically “quiet” circuit ground. This will ensure optimal PSRR and noise performance. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and, as a result, reduce the effect of fast current transients.

### 1.3.2. Regulated Output Voltage Pin (VOUT)

The VOUT pin is the regulated output voltage $V_R$ of the LDO. A minimum output capacitance of 3.3 µF is required for the LDO to ensure the stability in all operating conditions. The MCP1781 is stable with ceramic capacitors. See Section 2.2 “Output Capacitance Requirements” for output capacitor selection guidance.

### 1.3.3. Input Voltage Supply Pin (VIN)

Connect the input voltage source to VIN. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 3.3 µF to 10 µF should be sufficient for most applications. The type of capacitor used is ceramic. The low ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

### 1.3.4. Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage off. When the $\overline{SHDN}$ input is at a logic high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the LDO enters a low-quiescent current shutdown state, where the typical quiescent current is 3.5 µA.

### 1.3.5. Power Good Output (PWG)

PWG is an open drain output that can be connected to either 3.3V or 5V with a pull-up resistor, to monitor the status of the LDO regulated output voltage. When the regulated output voltage is above 94%, typically, the power good pin will indicate a logic high state. Similarly, if the value drops below 94% minus hysteresis, the pin will transition to a logic low state.

### 1.3.6. Adjustable Output Voltage (ADJ)

For adjustable version, the output voltage is connected to the ADJ input through a resistor divider that sets the output voltage regulation value. This provides the user the capability to set the output voltage to any value they desire within the 1.3V to 5.0V range of the device.

# 2. Functional Description

## 2.1. Device Overview

The MCP1781 is an AEC-Q100 qualified LDO capable of supplying 200 mA of current over its operating temperature range, while considering the acceptable power dissipation of the device. The device is offered in two fixed output voltage options, 3.3V and 5V, as well as an adjustable version that supports output voltages ranging from 1.3V to 5V. The part is stable with a minimum 3.3 µF ceramic capacitor and features a high-voltage $\overline{SHDN}$ pin, low voltage Power Good feedback for the regulated output voltage, current foldback protection and extended operating temperature range: –40°C to +150°C. The device also features an adequate PSRR of –80 dB typical for low frequencies and –36 dB for high frequencies.

An innovative adaptive bias circuitry is used to lower the power consumption at no load and light loads, without compromising the dynamic response.

The internal discharge transistor is useful when powering microcontrollers and other applications that require fast supply disconnect.

## 2.2. Output Capacitance Requirements

The MCP1781 requires a minimum output capacitance of 3.3 µF for output voltage stability. The output capacitor should be located as close to the LDO output as possible. The device is designed to work with low ESR ceramic capacitors. Ceramic materials X8R\L or X7R have low temperature coefficients and are well within the acceptable ESR range required. A typical 3.3 µF X8R 0805 capacitor has an ESR of 50 mΩ. A higher output capacitance can help with better transient response.

## 2.3. Input Capacitance Requirements

Low input-source impedance is necessary for the LDO output to operate properly. When operating using battery power, or in applications with long lead length (> 10 inches) between the input source and the LDO, adding input capacitance is recommended. A minimum of 3.3 µF to 10 µF of capacitance is sufficient for most applications. Given the high input voltage capability of the MCP1781, of up to 55V DC, it is recommended to use an appropriate voltage rating capacitor, and the derating of the capacitance as a function of voltage and temperature needs to be considered. The ceramic capacitor type should be X7R or X8R\L because their dielectrics are rated for use with temperatures between –40°C to +125°C or -55°C to +150°C, respectively.

## 2.4. Circuit Protection

The MCP1781 features current foldback protection during an output short-circuit event that occurs during normal operation. When the current foldback block detects an increase in load current, over the typical value of 450 mA, the output current and output voltage will start to decrease until the output current reaches a value of typically 10 mA (see Figure 4-16 and Figure 4-17).

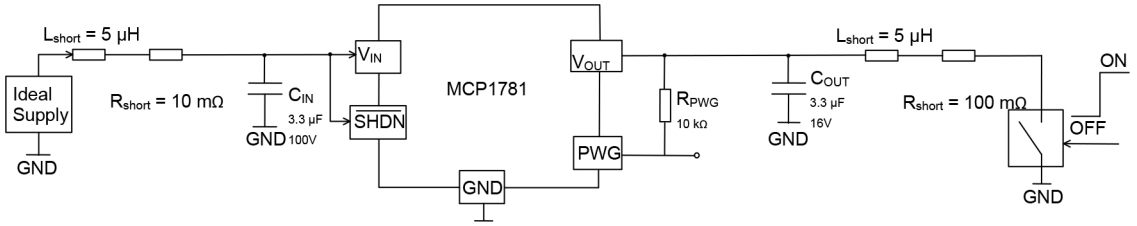
If a short circuit is present during power-up, the part will enter current limit protection and a constant current of 450 mA will be maintained. The part will not enter current foldback.

The MCP1781 was tested using the AEC-Q100 test set-up in Figure 2-1. The testing conditions require the use of very high parasitic inductances on the input and output. For cases like this, it is required to prevent the output voltage going below ground with more than 1V. Note that the VOUT pin can withstand a maximum of –0.3 VDC (see Absolute Maximum Ratings). This can be achieved by placing a diode with the cathode to VOUT and the anode to ground.

Thermal shutdown functionality is present on the device and adds to the protection features of the part. Thermal shutdown is triggered at a typical value of 169°C and has a typical hysteresis of 11°C.

**Figure 2-1.** Short Circuit Test Setup

**Figure 2-2.** Short Circuit Test Setup




## 2.5. Dropout Operation

In automotive applications, depending on the severity of the cold crank, the supply voltage can drop down to 3V and the part can enter dropout in these conditions. It is preferred to ensure that the part does not operate in dropout during DC operation so that the AC performance is maintained.

The device has a dropout voltage of approximately 380 mV at full load and room temperature, but because of the extended temperature range at 150°C, due to increased leakage, it reaches up to 705 mV.

## 2.6. Shutdown Input ($\overline{SHDN}$) and Input UVLO

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO ON or OFF. The $\overline{SHDN}$ threshold has a logic HIGH level of minimum 1.13V and a logic LOW level of maximum 0.79V.

The $\overline{SHDN}$ pin ignores low-going pulses that are up to 10 µs. This blanking window helps to reject any system noise spikes on the $\overline{SHDN}$ input signal. Then, on the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry adds 600 µs delay before allowing the regulator output to turn ON. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the (10 + 600) µs delay, the regulator starts charging the load capacitor as the output rises from 0V to its regulated value. The charging current amplitude will be limited by the short circuit current value of the device. If the $\overline{SHDN}$ input signal is pulled low during the 610 µs delay period, the timer will be reset, and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. Figure 2-2 shows a timing diagram of the $\overline{SHDN}$ input.

The MCP1781 has an internal discharge transistor connected to the VOUT Pin that is enabled when the $\overline{SHDN}$ pin goes low. The discharge occurs through a typical resistance of 105Ω.

The UVLO block helps prevent false start-ups during the power-up sequence, until the input voltage reaches a value of 2.7V. The minimum input voltage required for normal operation needs to take into account the dropout voltage for the specific output voltage and output current conditions.

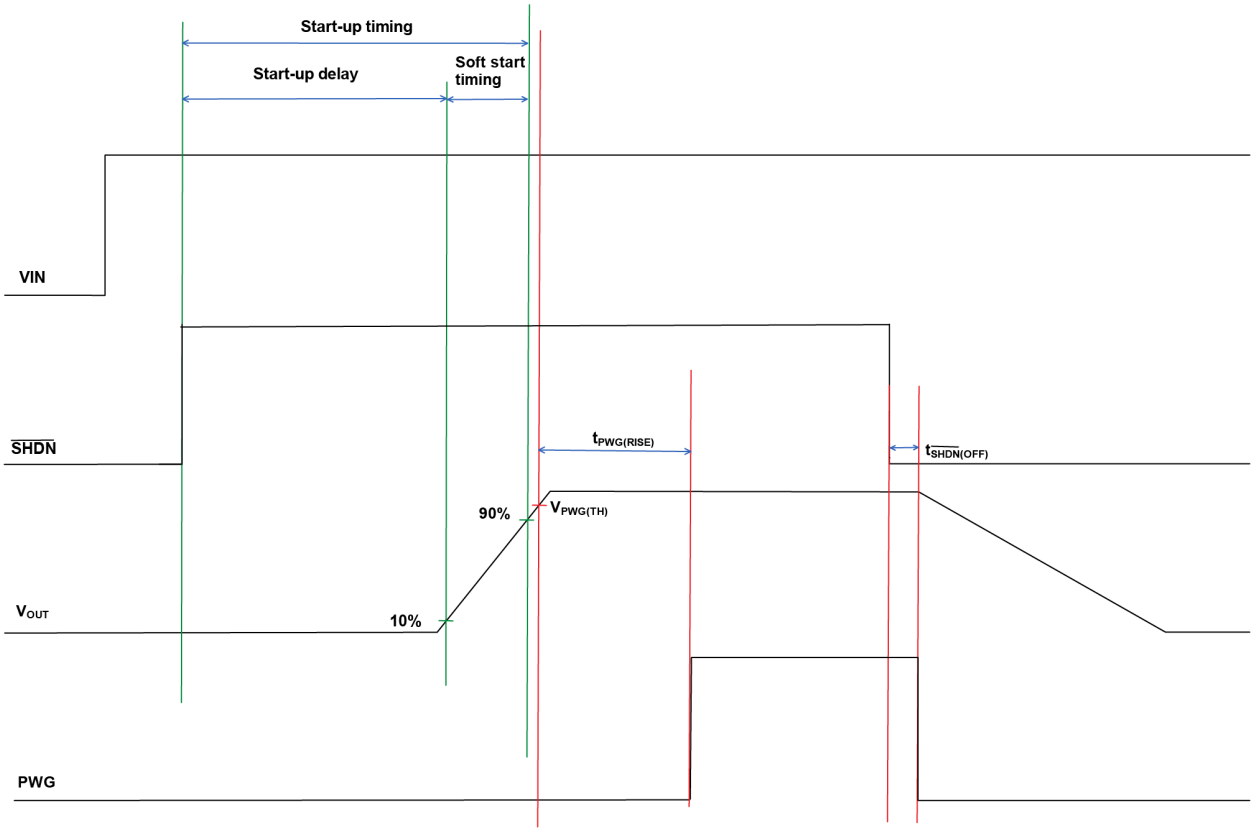
## 2.7. Power Good

The Power Good function is a low voltage open drain output which can be used to monitor the output of the LDO in relation to the Power Good Threshold level ($V_{PWG(TH)}$), which is typically 94% of the output voltage.

During a normal start up sequence the open drain output is held low until the monitored regulated output voltage reaches the value of $V_{PWG(TH)}$. After which the power good time delay ($t_{PWG(RISE)}$) will start, and after 98 µs typically the PWG pin will become inactive and can be pulled high by the external pull up resistor connected to VOUT or a separate supply rail that is below 5.5V.

During transient events, false triggering of the Power Good signal is prevented by means of time delay ($t_{PWG(FALL)}$), typically, of 105 µs. After the internal circuitry detects the regulated output falling below the $V_{PWG(TH)}$minus $V_{PWG(HYS)}$, the open drain output won't be pulled low until the time delay passes. When the $\overline{SHDN}$ is pulled low, if the requirements for a valid signal are met, then the Power Good open drain will be pulled low. The output will be discharged by the output discharge block by means of 105Ω resistor pulled down to GND.

**Figure 2-3.** Shutdown Input Timing Diagram




## 2.8. LDO Output Voltage

The MCP1781 LDO is available with either two fixed output voltages (3.3V and 5V) or an adjustable output voltage. The output voltage range for the adjustable version is from 1.3V to 5.0V .

The adjustable version of the MCP1781 uses the ADJ pin (pin 5) to get the output voltage feedback for output voltage regulation. This allows the user to set the output voltage of the device with two external resistors. The reference voltage for ADJ is 1.21V typical value.

Figure 2-3 shows the adjustable version of the MCP1781. Resistors $R_{TOP}$ and $R_{BOT}$ form the resistor divider network necessary to set the output voltage. With this configuration, the equation for setting VOUT is:

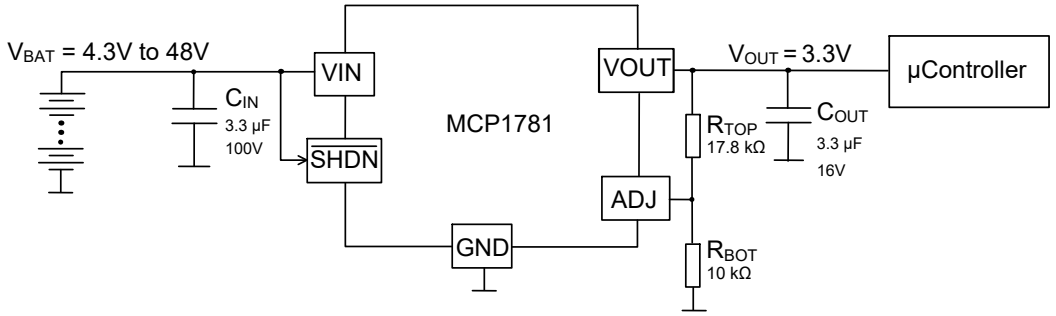
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Where:

- VOUT = LDO's Output Voltage
- $V_{REF}$ = ADJ Pin Voltage (typically 1.21V)

The allowable resistance value range for resistor $R_{BOT}$ is from 10 kΩ to 200 kΩ.

**Figure 2-4.** MCP1781 Adjustable Output Version Typical Application



# 3. Electrical Characteristics

## 3.1. Absolute Maximum Ratings

| | |
|---|---|
| Input Voltage | +70.0V |
| Maximum Voltage on $\overline{SHDN}$ | (GND – 0.3V) to ($V_{IN}$ + 0.3V) |
| Maximum Voltage on VOUT | (GND – 0.3V) to 5.5V |
| Maximum Voltage on PWG | (GND – 0.3V) to 5.5V |
| Maximum Voltage on ADJ | (GND – 0.3V) to 5.5V |
| Output Short-Circuit Duration | Unlimited (Note 2) |
| Storage Temperature | -55°C to +175°C |
| Maximum Junction Temperature, $T_J$ | +185°C |
| Operating Junction Temperature, $T_J$ | –40°C to +150°C |
| ESD Protection on All Pins: | |
| HBM | ≥ ±2 kV |
| CDM | ≥ ±750V |

**Attention:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 3.2. DC/AC Characteristics

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = V_R + 1V$ (Note 1), $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 3.3 µF ceramic (X7R), $T_J$ = +25°C, $\overline{SHDN}$ > 2.4V. **Boldface** type applies for junction temperatures $T_J$ of –40°C to +150°C (Note 2).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | |
| Input Operating Voltage | $V_{IN}$ | **4.3** | — | **55** | V | $V_{OUT}$ = 3.3V |
| | | **6** | — | **55** | V | $V_{OUT}$ = 5.0V |
| | | **4** | — | **55** | V | $V_{OUT}$ = Adjustable (ADJ) |
| ADJ Nominal Reference Value | $V_{REF}$ | **1.18** | 1.21 | **1.24** | V | Adjustable output version |
| ADJ Leakage Current | $I_{ADJ(LKG)}$ | — | — | **100** | nA | Adjustable output version |
| Output Voltage Accuracy | $V_{OUT}$ | **$V_R$ – 2%** | $V_R$ | **$V_R$ + 2%** | % | Fixed output versions |
| | | **$V_R$ – 3%** | $V_R$ | **$V_R$ + 3%** | | Adjustable output version. Assumes perfect external divider. |
| Input Quiescent Current | $I_Q$ | — | 34 | **57** | µA | $V_{IN(MIN)} \leq V_{IN} \leq 55V$; $I_{OUT}$ = 0 mA |
| Input Quiescent Current for $\overline{SHDN}$ Mode | $I_{\overline{SHDN}}$ | — | 3.5 | **15** | µA | $\overline{SHDN}$ = GND, $V_{IN}$ = 55V |
| Ground Current | $I_{GND}$ | — | 85 | **122** | µA | $I_{GND} = I_{IN} - I_{OUT}$ $I_{OUT}$ = 200 mA |
| Maximum Output Current | $I_{OUT}$ | **200** | — | — | mA | (Note 2) |
| Line Regulation | $\Delta V_{OUT} / (V_{OUT} \times \Delta V_{IN})$ | **-0.005** | ±0.002 | **+0.005** | %/V | $V_{IN(MIN)} \leq V_{IN} \leq 55V$ |

**DC/AC Characteristics** (continued)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Load Regulation | $\Delta V_{OUT}/V_{OUT}$ | **-0.1** | ±0.06 | **+0.1** | % | $I_{OUT}$ =1 mA to 200 mA |
| Dropout Voltage | $V_{DROPOUT}$ | — | 380 | **705** | mV | $I_{OUT}$ =200 mA (Note 3) |
| **AC Performance** | | | | | | |
| Output Noise | $e_N$ | — | 300 | — | µVrms | f = 10 Hz to 10 MHz, $V_{IN}$ = 16V, $I_{OUT}$ = 100 mA (Note 5) |
| Power Supply Rejection Ratio | PSRR | — | –80 | — | dB | f = 100 Hz (Note 4) (Note 5) |
| | | — | –65 | — | | f = 1 kHz (Note 4) (Note 5) |
| | | — | –36 | — | | f = 100 kHz (Note 4) (Note 5) |
| **Current Limit** | | | | | | |
| Foldback Current Limit | $I_{CL}$ | — | 450 | — | mA | (Note 5) |
| Foldback Current | $I_{FOLDBACK}$ | — | 10 | — | mA | $V_{OUT}$ ≈ 0V (Note 5) |
| **Undervoltage Lock Out** | | | | | | |
| Input Voltage to Turn-on Output | $V_{UVLO(HI)}$ | — | 2.7 | — | V | Rising $V_{IN}$ |
| Input Voltage to Turn-off Output | $V_{UVLO(LO)}$ | — | 2.3 | — | V | Falling $V_{IN}$ |
| **Shutdown** | | | | | | |
| Logic High Input | $V_{\overline{SHDN}(HI)}$ | **1.13** | — | — | V | |
| Logic Low Input | $V_{\overline{SHDN}(LO)}$ | — | — | **0.79** | V | |
| $\overline{SHDN}$ Input Leakage Current | $I_{\overline{SHDN}(LK)}$ | — | — | **0.22** | µA | $V_{\overline{SHDN}}$ = 55V |
| Turn-off delay | $t_{\overline{SHDN}(OFF)}$ | — | 22 | — | µs | $V_{\overline{SHDN}}$ Falling (Note 5) |
| **Soft Start** | | | | | | |
| Soft Start Timing | $t_{ss}$ | — | 450 | **720** | µs | From 10% of $V_R$ to 90% of $V_R$ |
| Start-up Delay | $t_{DELAY}$ | — | 600 | — | µs | From $V_{IN}$ = $V_{SHDN}$ = 0V to VR + 1V, until $V_{OUT}$ = 10% of $V_R$ (See Note 5) |
| **Power Good** | | | | | | |
| Power Good Threshold | $V_{PWG(TH)}$ | **90** | 94 | **97** | % VOUT | Rising $V_{OUT}$ |
| Power Good Hysteresis | $V_{PWG(HYS)}$ | **1** | 3 | **6** | % VOUT | Falling $V_{OUT}$ |
| Power Good Sink Capability | $I_{PWG(SINK)}$ | **5** | — | — | mA | |
| Power Good Output Voltage Low | $V_{PWG(VOL)}$ | — | 36 | **66** | mV | $I_{PWGSINK}$ = 5 mA; $V_{OUT}$ = 0V |
| Power Good Leakage | $I_{PWG(LKG)}$ | — | — | **20** | nA | $V_{PWG}$ = 5.5V |
| Power Good Delay Rising | $t_{PWG(RISE)}$ | — | 98 | — | µs | Delay after $V_{OUT}$ crosses Power Good Threshold (Note 5) |
| Power Good Delay Falling | $t_{PWG(FALL)}$ | — | 105 | — | µs | Delay after $V_{OUT}$ crosses Power Good Threshold minus Hysteresis (Note 5) |
| **Output Discharge Transistor** | | | | | | |
| Discharge Resistance | $R_{DS(ON)}$ | — | 105 | — | Ω | (Note 5) |

**DC/AC Characteristics** (continued)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|

**Notes:**

1. VR is the nominal output voltage. The minimum input voltage is 4.3V for $V_R$ = 3.3V and 6V for $V_R$ = 5V.
2. The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). See the Temperature Specifications table and Section 5. Application Information. Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.
3. Dropout voltage is defined as the input to output voltage differential at which the output voltage drops 2% below its nominal value.
4. PSRR measurement is carried out with $C_{IN}$ =0 µF, $V_{IN}$ = 14.5V, $I_{OUT}$ = 100 mA, $V_{INAC}$ = 0.4 $V_{pkpk}$.
5. Not production tested.

## 3.3. Temperature Specifications

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Thermal Shutdown | $T_{SD}$ | — | 169 | — | °C | Rising Temperature (not production tested) |
| Thermal Shutdown Hysteresis | $\Delta_{TSD}$ | — | 11 | — | °C | Falling Temperature (not production tested) |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, SOT-223-5LD | $\theta_{JA}$ | — | 68.3 | — | °C/W | JEDEC® standard 4-layer FR4 board with 1 oz. copper |
| | $\theta_{JB}$ | — | 18.3 | — | °C/W | |
| | $\Psi_{JT}$ | — | 6.6 | — | °C/W | |
| Thermal Resistance, TO-252-5LD | $\theta_{JA}$ | — | 32.7 | — | °C/W | |
| | $\theta_{JB}$ | — | 8.3 | — | °C/W | |
| | $\Psi_{JT}$ | — | 3.8 | — | °C/W | |

# 4. Typical Performance Curves

**Important:** The graphs provided in this section are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Figure 4-1.** Output Voltage vs. Input Voltage (3.3V)

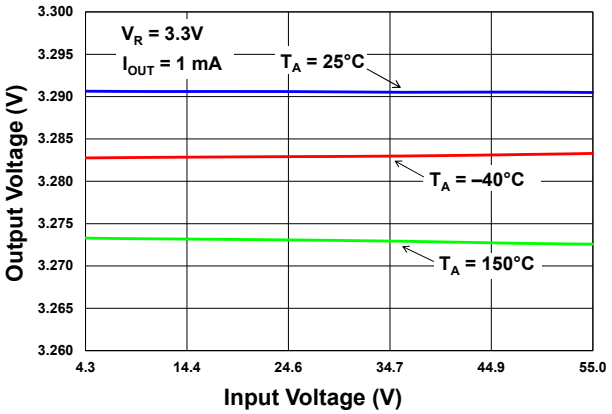



**Figure 4-2.** Output voltage vs. Input Voltage (5V)

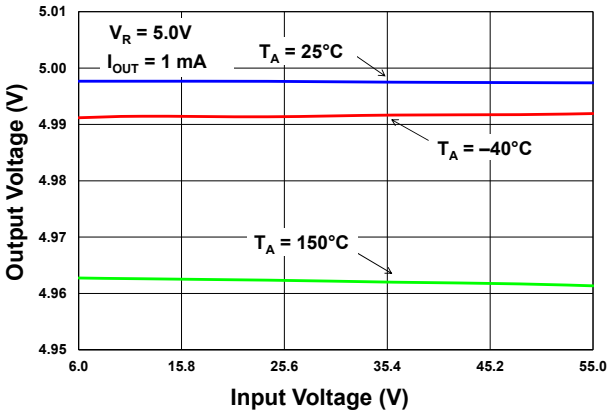



**Figure 4-3.** Output Voltage vs. Output Current (3.3V)

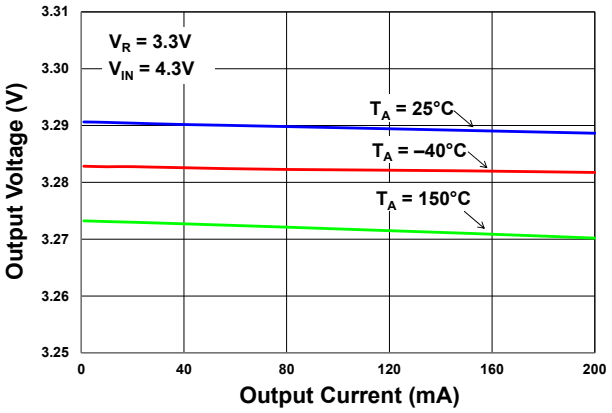



**Figure 4-4.** Output Voltage vs. Output Current (5V)

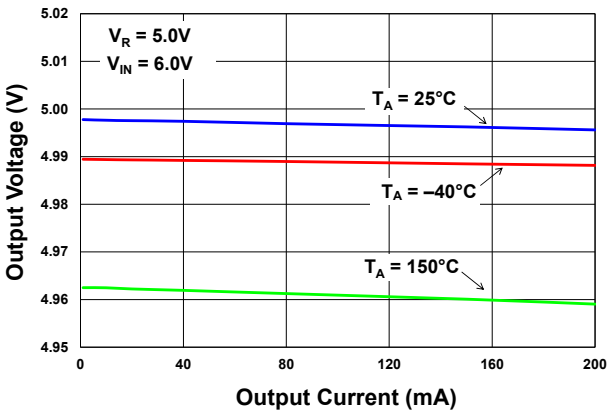


**Figure 4-5.** Dropout Voltage vs. Load Current (5V)

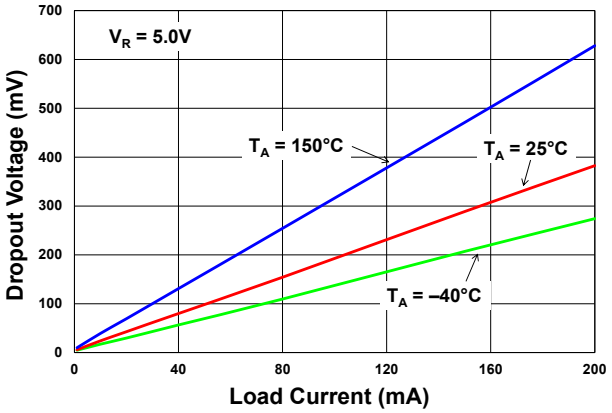



**Figure 4-6.** Load Regulation vs. Ambient Temperature (3.3V)

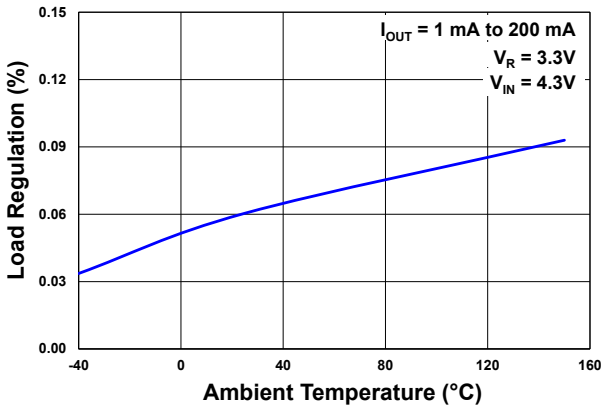



**Figure 4-7.** Load Regulation vs. Ambient Temperature (5V)

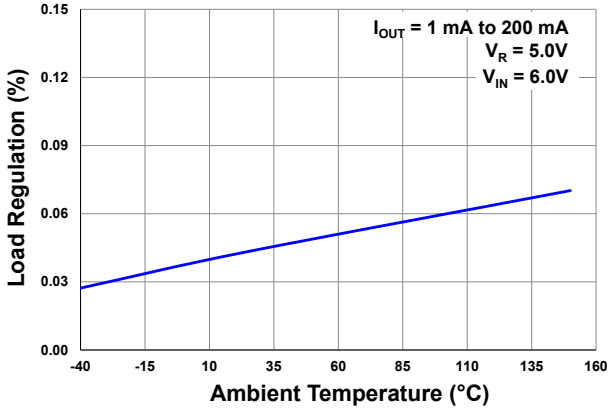



**Figure 4-8.** Line Regulation vs. Ambient Temperature (3.3V)

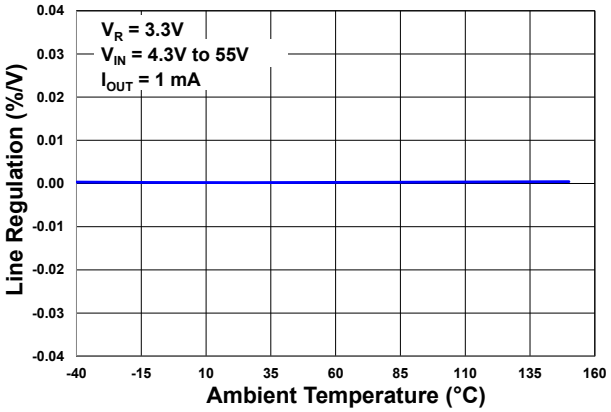



**Figure 4-9.** Line Regulation vs. Ambient Temperature (5V)

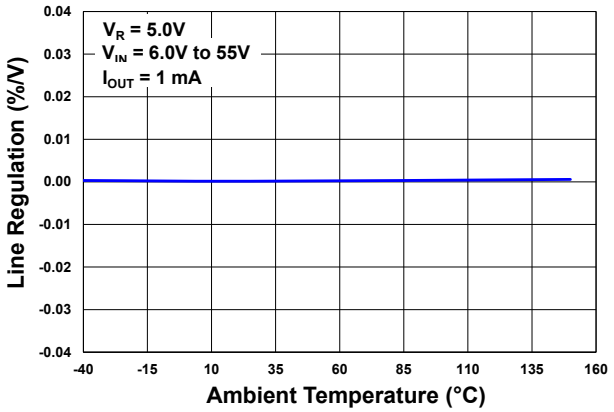


**Figure 4-10.** Quiescent Current vs. Input Voltage (3.3V)

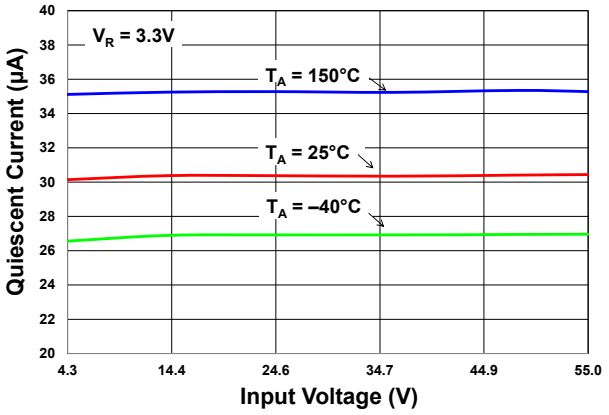



**Figure 4-11.** Quiescent Current vs. Input Voltage (5V)

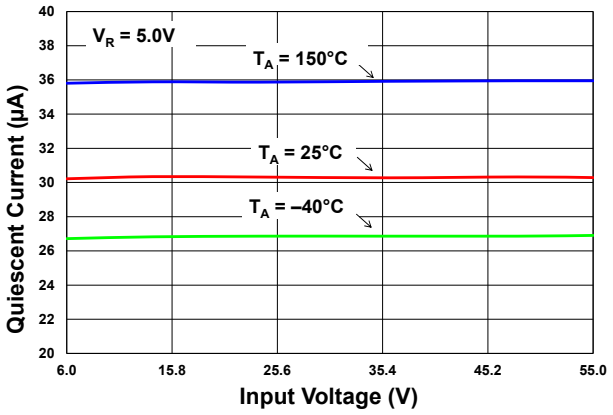



**Figure 4-12.** Shutdown Current vs. Input Voltage (3.3V)

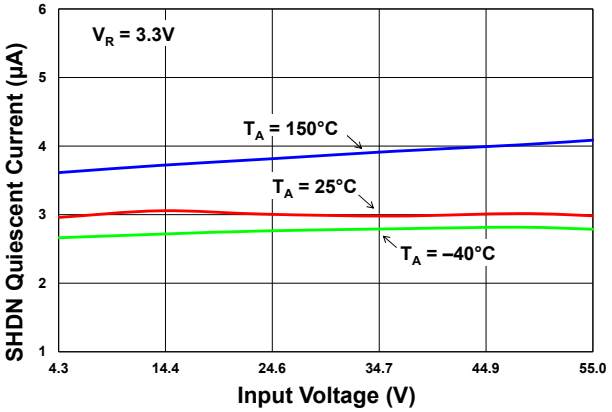



**Figure 4-13.** Shutdown Current vs. Input Voltage (5V)

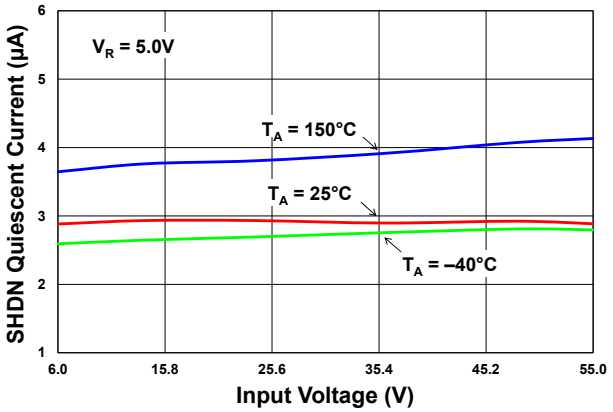



**Figure 4-14.** Ground Current vs. Output Current (3.3V)

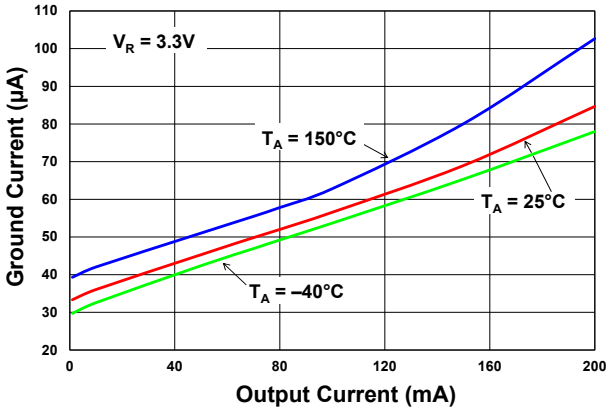



**Figure 4-15.** Ground Current vs. Output Current (5V)

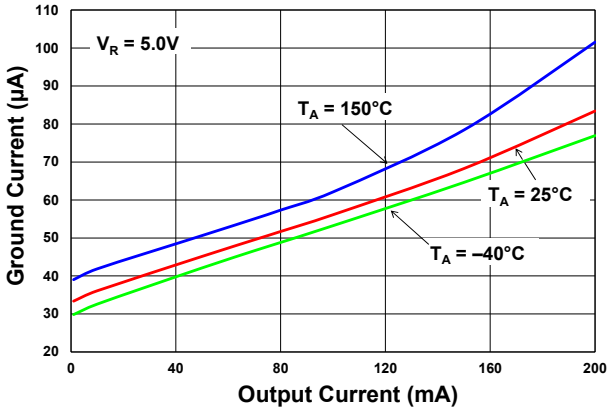


**Figure 4-16.** Current Foldback (3.3V)

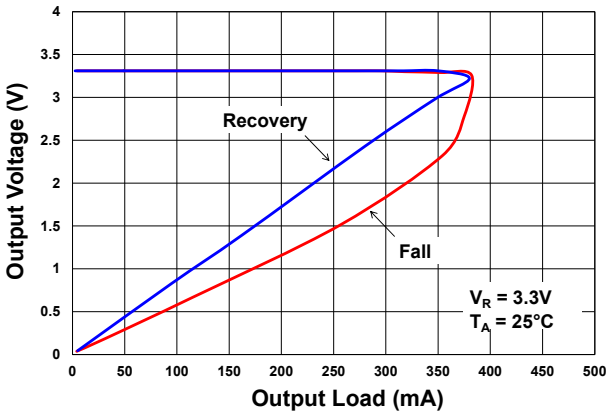



**Figure 4-17.** Current Foldback (5V)

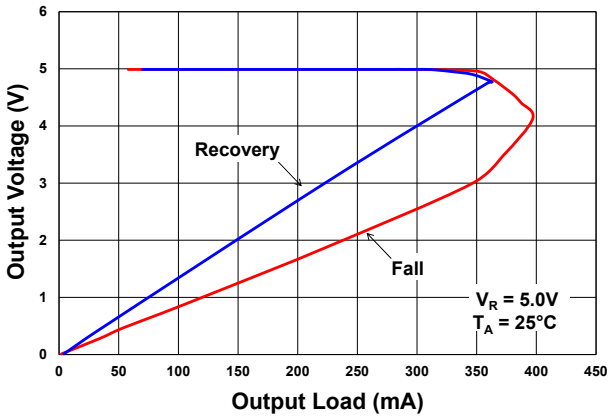



**Figure 4-18.** UVLO (3.3V)

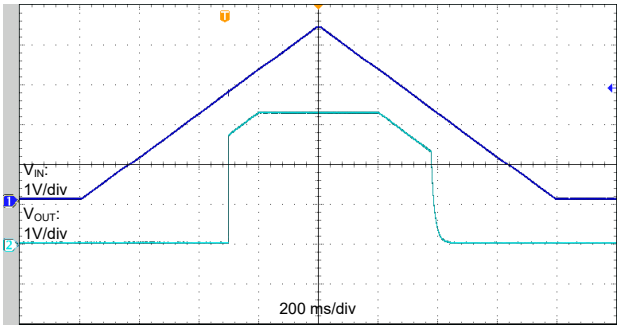



**Figure 4-19.** UVLO (5V)

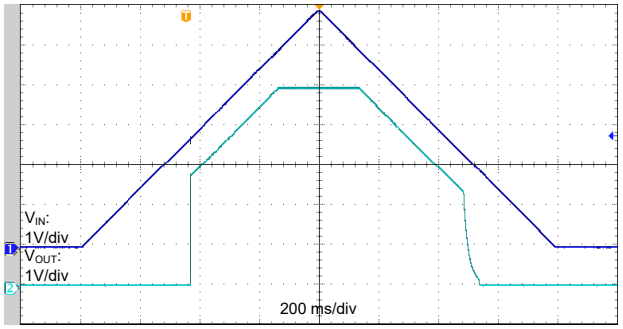



**Figure 4-20.** Noise vs. Frequency (1.3V – ADJ Output)

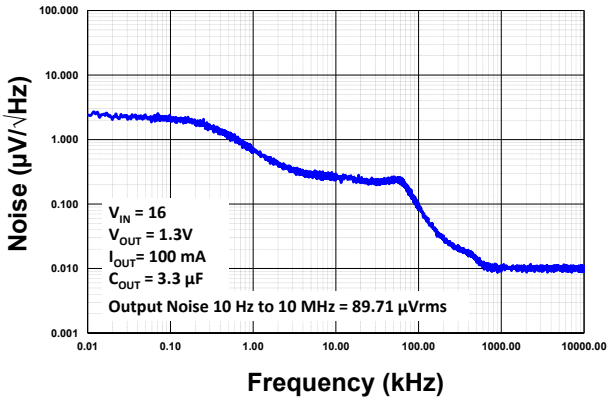



**Figure 4-21.** Noise vs. Frequency (3.3V)

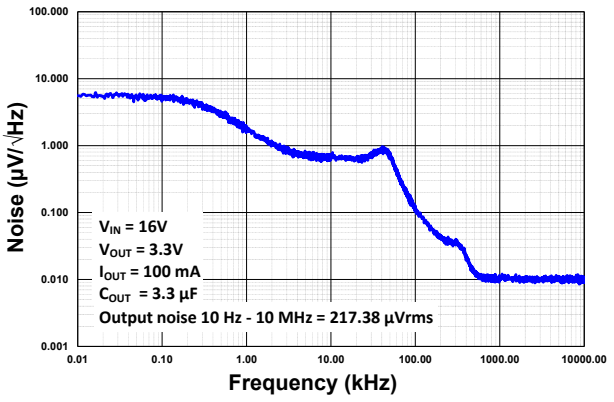


**Figure 4-22.** Noise vs. Frequency (5V)

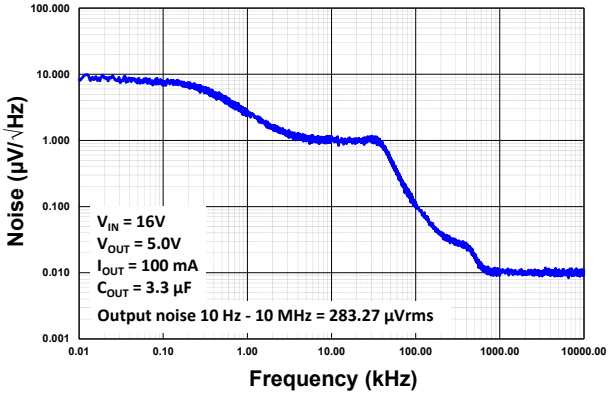



**Figure 4-23.** PSRR vs. Frequency (1.3V – ADJ Output)

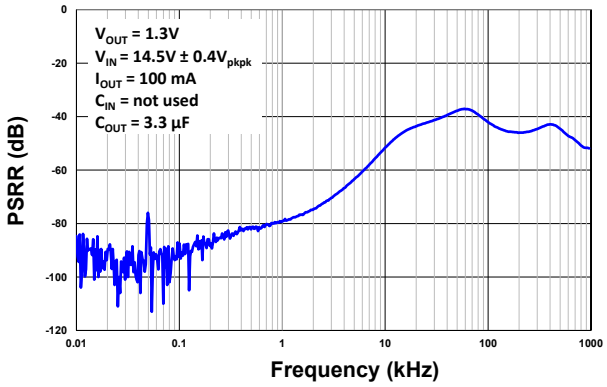



**Figure 4-24.** PSRR vs. Frequency (3.3V)

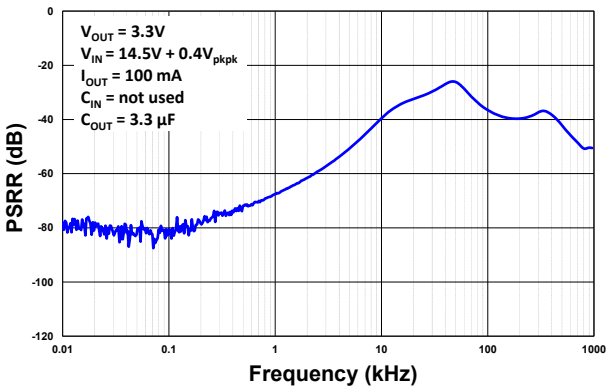



**Figure 4-25.** PSRR vs. Frequency (5V)

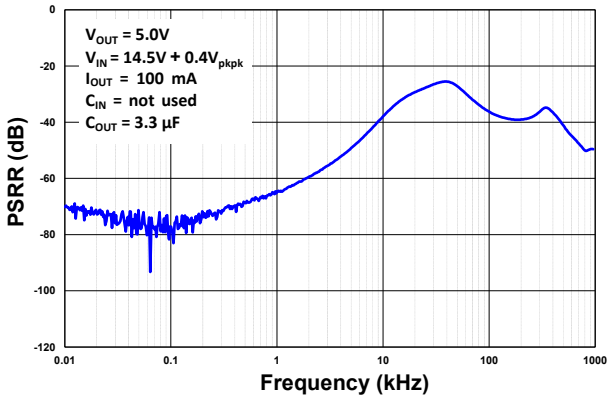



**Figure 4-26.** Dynamic Load Step (3.3V)

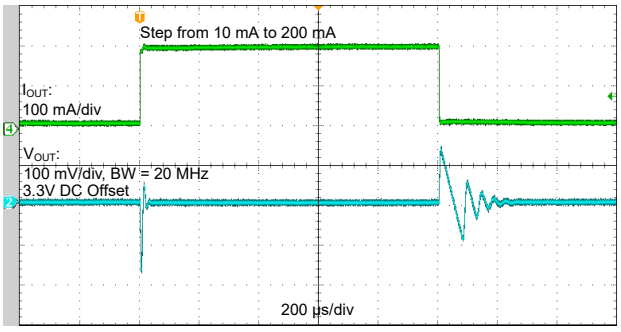



**Figure 4-27.** Dynamic Load Step (5V)

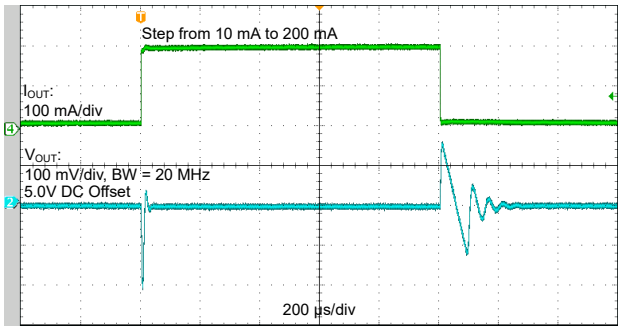


**Figure 4-28.** Dynamic Line Step 4.3V to 14V (3.3V)

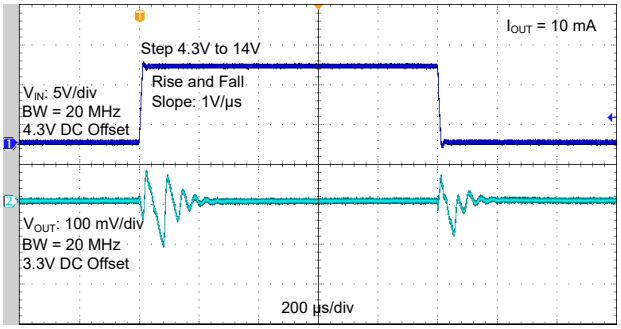



**Figure 4-29.** Dynamic Line Step 6V to 14V (5V)

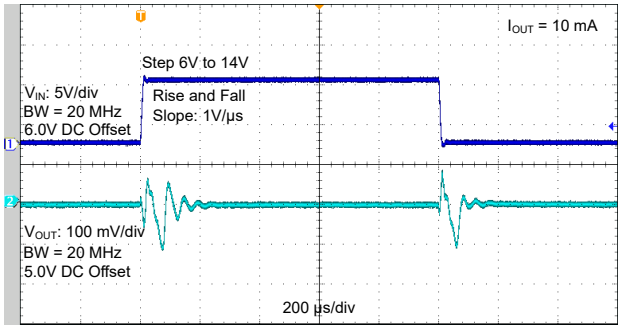



**Figure 4-30.** Dynamic Line Step (12V to 48V, 3.3V)

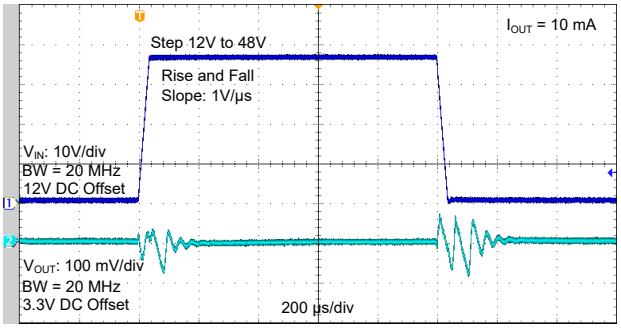



**Figure 4-31.** Dynamic Line Step (12V to 48V, 5V)

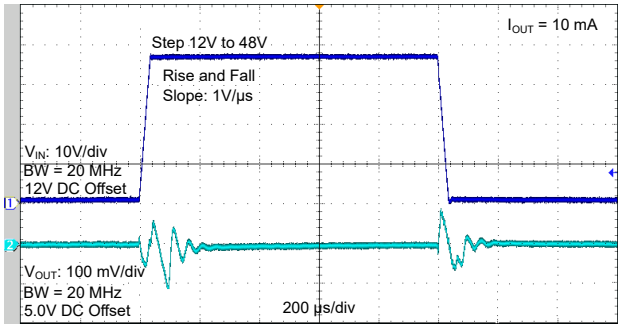



**Figure 4-32.** Start-up from VIN (0V to 14V, 3.3V)

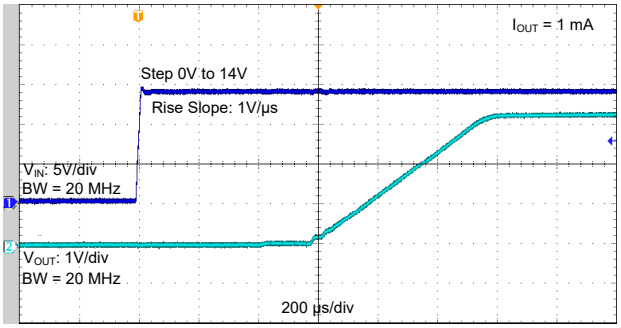



**Figure 4-33.** Start-up from VIN (0V to 14V, 5V)

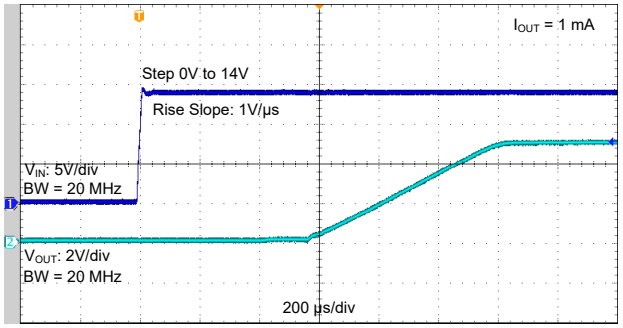



**Figure 4-34.** Start-up from VIN (0V to 48V, 3.3V)

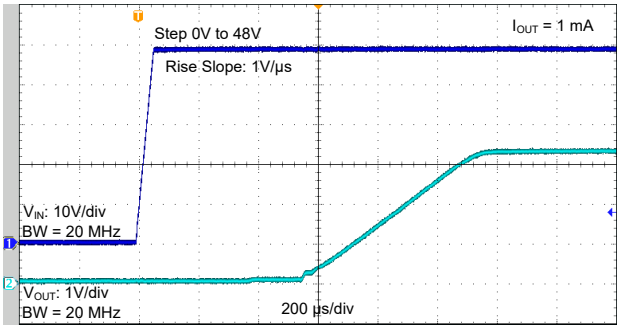



**Figure 4-35.** Start-up from VIN (0V to 48V, 5V)

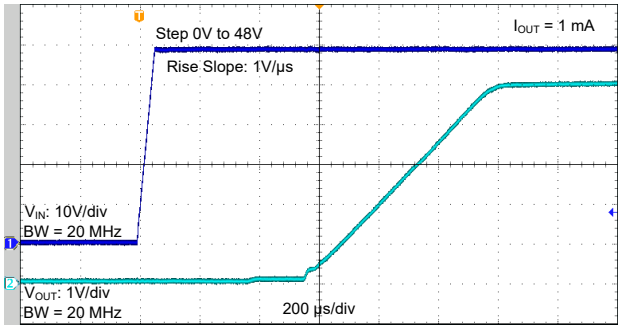


**Figure 4-36.** Start-up from $\overline{SHDN}$ (0V to 5V, 3.3V)

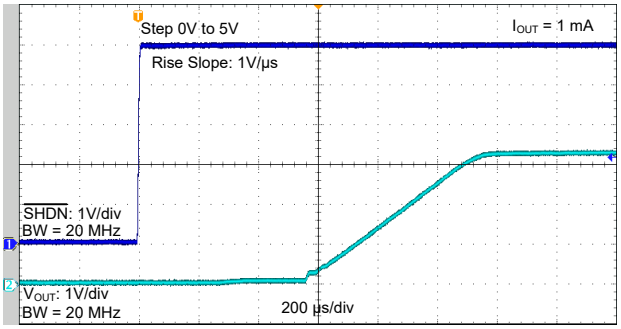



**Figure 4-37.** Start-up from $\overline{SHDN}$ (0V to 5V, 5V)

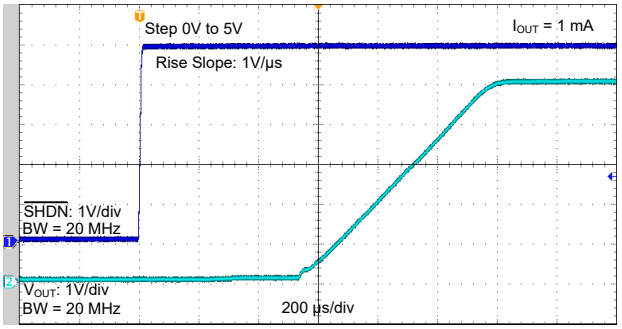



**Figure 4-38.** Power Good Transitions (3.3V)

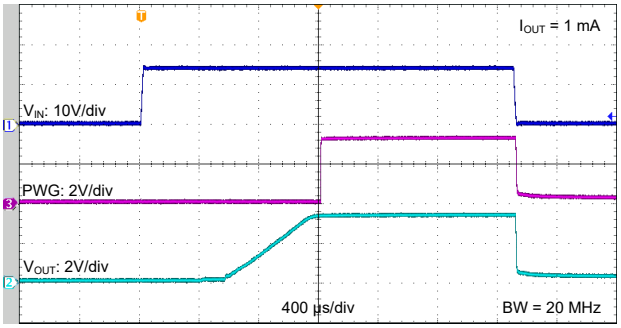
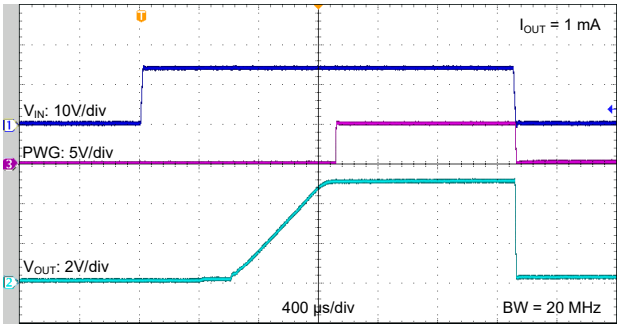



**Figure 4-39.** Power Good Transitions (5V)



# 5. Application Information

## 5.1. Typical Application

The MCP1781 is used for applications that require high input voltage and are prone to high transient voltages on the input (see Typical Application Circuit).

### 5.1.1. Power Dissipation Calculations

The internal power dissipation within the MCP1781 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

**Equation 5-1.** Internal Power Dissipation

$$P_{LDO} = \left(V_{IN(MAX)} - V_{OUT(MAX)}\right) \times I_{OUT(MAX)}$$

Where:

$P_{LDO}$ = Internal power dissipation of the LDO pass device

$V_{IN(MAX)}$ = Maximum input voltage in the application

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current in the application

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1781 because of quiescent or ground current. The power dissipation as a result of ground current can be calculated by applying Equation 5-2:

**Equation 5-2.** Ground Current Power Dissipation

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the ground current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage in the application

$I_{GND}$ = Current flowing into the GND pin

The total power dissipated within the MCP1781 is the sum of the power dissipated in the LDO pass device and the ground current power dissipation term. Because of the CMOS construction, the $I_{GND}$ for the MCP1781 is typically 85µA at full load. Operating at a maximum $V_{IN}$ of 55V results in a power dissipation of 4.675 mW. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1781 is +150°C. To estimate the internal junction temperature of the MCP1781, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient ($\theta_{JA}$) of the device. For example, the thermal resistance from junction-to-ambient for the 5-Lead SOT-223 package is estimated at 68.3°C/W.

**Equation 5-3.** Maximum Continuous Junction Temperature

$$T_{J(MAX)} = P_{LDO} \times \theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

$P_{LDO}$ = Total power dissipation of the device

$\theta_{JA}$ = Thermal resistance from junction-to-ambient

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The equation below can be used to determine the package maximum internal power dissipation.

**Equation 5-4.** Package Maximum Internal Power Dissipation

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

$T_{J(MAX)}$ = Maximum continuous junction temperature

$T_{A(MAX)}$ = Maximum ambient temperature

$\theta_{JA}$ = Thermal resistance from junction-to-ambient

**Equation 5-5.** Device Junction Temperature Increase

$$T_{J(RISE)} = P_{D(MAX)} \times \theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$P_{D(MAX)}$ = Maximum power dissipation of the device

$\theta_{JA}$ = Thermal resistance from junction-to-ambient

**Equation 5-6.** Device Junction Temperature

$$T_J = T_{J(RISE)} + T_A$$

Where:

$T_J$ = Junction temperature

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$T_A$ = Ambient temperature

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance from junction-to-ambient for the application. The thermal resistance from junction-to-ambient ($\theta_{JA}$) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction-to-ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to Application Note AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), for more information regarding this subject.

### 5.1.2. Typical Application Examples

#### 5.1.2.1. Internal Power Dissipation

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

**Equation 5-7.** Power Dissipation Example

**Package:**

Package Type = 5-Lead SOT-223

**Input Voltage:**

$V_{IN}$ = 14V±5%

**LDO Output Voltage and Current:**

$V_{OUT}$ = 5V

$I_{OUT}$ = 100 mA

**Maximum Ambient Temperature:**

$T_{A(MAX)}$ = +60°C

**Internal Power Dissipation:**

$$P_{\mathrm{LDO(MAX)}} = \left(V_{IN(MAX)} - V_{OUT(MIN)}\right) \times I_{OUT(MAX)}$$

$$P_{LDO} = (14.7 - 4.9) \times 100\ \mathrm{mA}$$

$$P_{LDO} = 0.98\ \mathrm{Watts}$$

#### 5.1.2.2. Device Junction Temperature Rise

**Equation 5-8.** Device Junction Temperature Increase Example

$$T_{J(RISE)} = P_{TOTAL} \times \theta_{JA}$$

$$T_{J(RISE)} = 0.98\mathrm{W} \times 68.3°\mathrm{C/W}$$

$$T_{J(RISE)} = 66.934°\mathrm{C}$$

#### 5.1.2.3. Junction Temperature Estimate

**Equation 5-9.** Device Junction Estimate Example

$$T_J = T_{J(RISE)} + T_A$$

$$T_J = 66.934°C + 60°C$$

$$T_{J(RISE)} = 126.934°C$$

#### 5.1.2.4. Maximum Package Power

Dissipation at +60°C Ambient Temperature.

**Equation 5-10.** Maximum Allowable Dissipation at +60°C Ambient Temperature

5-Lead SOT-223 ($\theta_{JA}$ = 68.3°C/W):

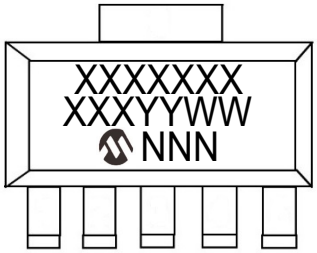
$$P_{D(MAX)} = \frac{150°C - 60°C}{68.3°C/W}$$

$$P_{D(MAX)} = 1.317W$$

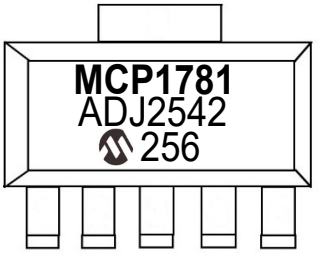
# 6. Package Information

## 6.1. Package Marking Information

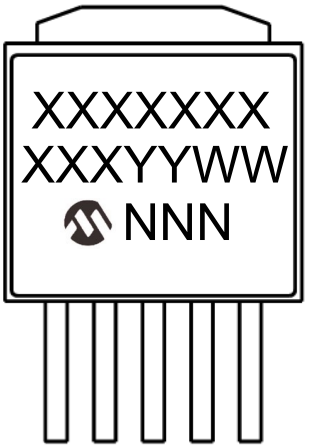
5-Pin SOT-223:



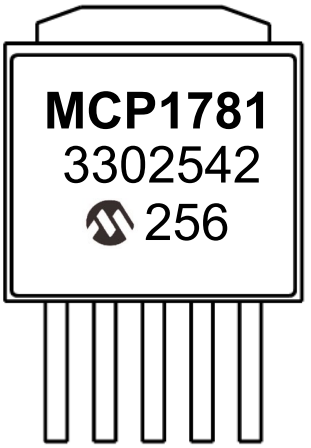

Example:




5-Pin TO-252:




Example:



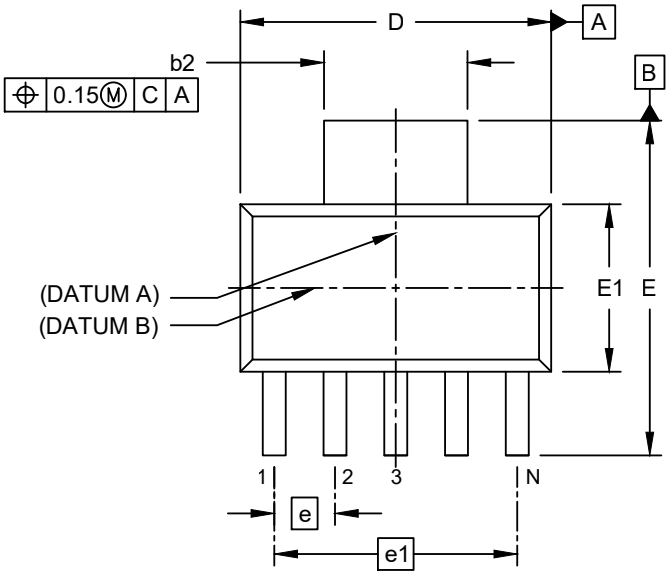

| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

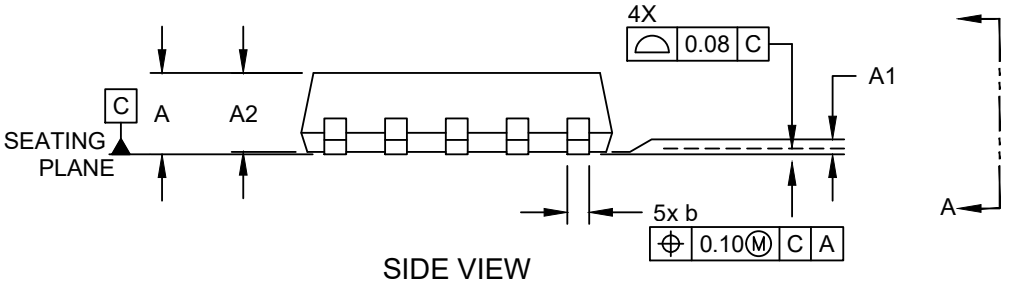
## 6.2. Package Outline Drawings

### 5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

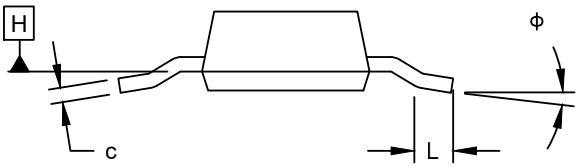
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

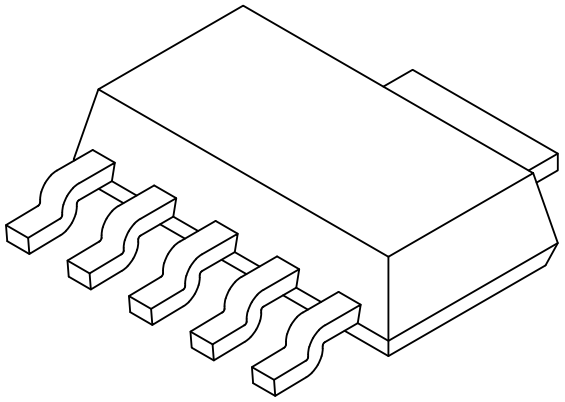



VIEW A-A

Microchip Technology Drawing C04-00137-N7X Rev E Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 5 | |
| Lead Pitch | e | | 1.27 BSC | |
| Outside lead pitch | e1 | | 5.08 BSC | |
| Overall Height | A | - | - | 1.80 |
| Standoff | A1 | 0.02 | 0.06 | 0.10 |
| Molded Package Height | A2 | 1.55 | 1.60 | 1.65 |
| Overall Width | E | 6.86 | 7.00 | 7.26 |
| Molded Package Width | E1 | 3.45 | 3.50 | 3.55 |
| Overall Length | D | 6.45 | 6.50 | 6.55 |
| Lead Thickness | c | 0.24 | 0.28 | 0.32 |
| Lead Width | b | 0.41 | 0.46 | 0.51 |
| Tab Lead Width | b2 | 2.95 | 3.00 | 3.05 |
| Foot Length | L | 0.91 | - | - |
| Lead Angle | ϕ | 0° | - | 10° |

Notes:

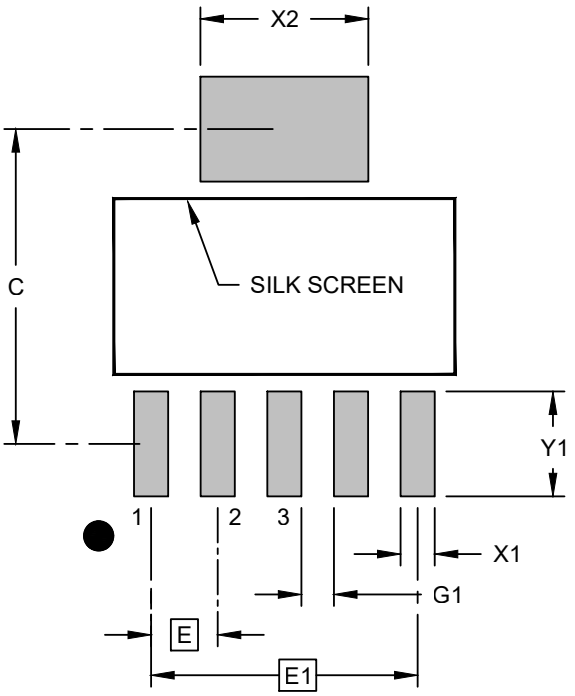
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00137-N7X Rev E Sheet 2 of 2

## 5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pitch | E1 | | 5.08 BSC | |
| Contact Pad Spacing | C | | 6.10 | |
| Contact Pad Width (X5) | X1 | | | 0.65 |
| Contact Pad Width | X2 | | | 3.20 |
| Contact Pad Length (X6) | Y1 | | | 1.90 |
| Distance Between Pads (X4) | G1 | 0.62 | | |

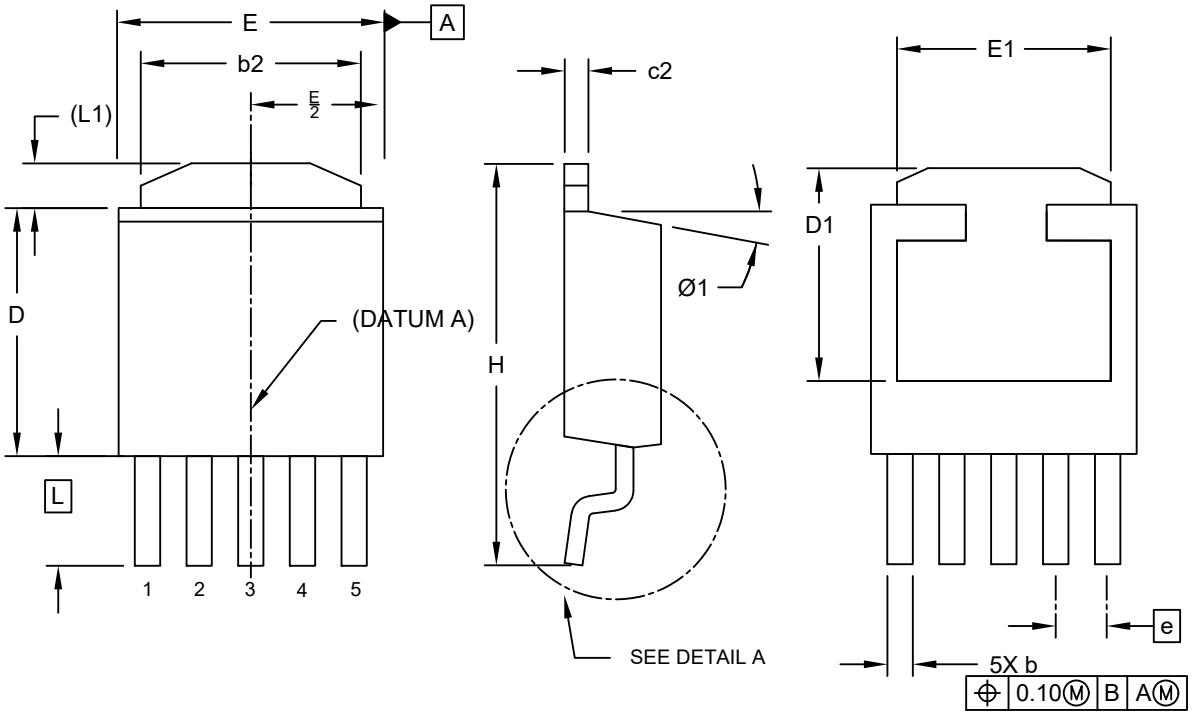
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

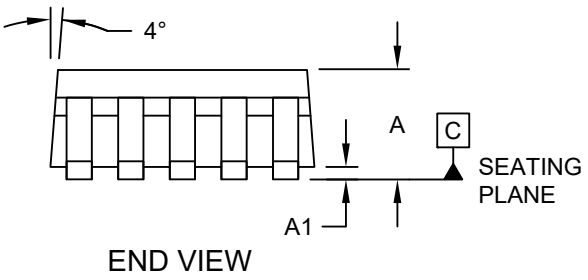
Microchip Technology Drawing C04-02137-N7X Rev E

## 5-Lead Transistor Outline (9EA) - [TO-252]
## Option "A"

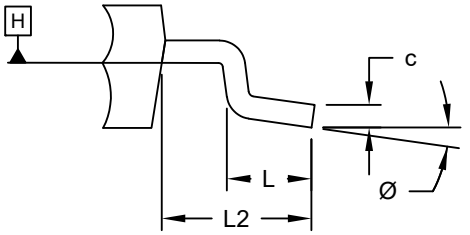
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




TOP VIEW SIDE VIEW BOTTOM VIEW




END VIEW

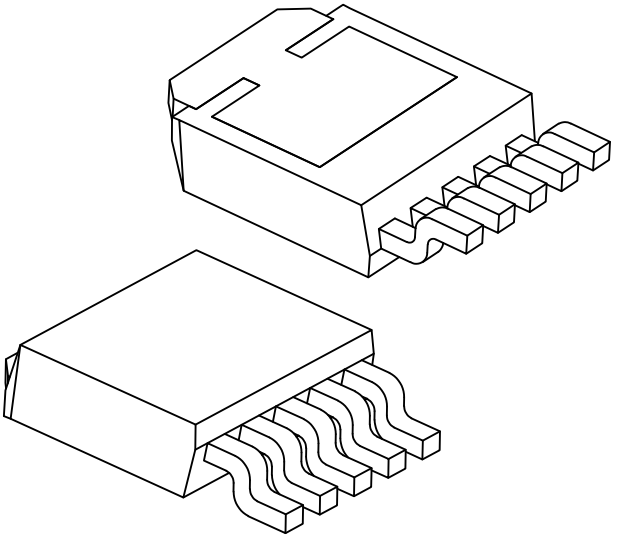



DETAIL A
Rotated 90° CCW

Microchip Technology Drawing C04-1168 Rev A Sheet 1 of 2

## 5-Lead Transistor Outline (9EA) - [TO-252]
## Option "A"

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | Min | Nom | Max |
| Number of Leads | N | | 5 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 2.18 | – | 2.38 |
| Seating Plane Height | A1 | – | – | 0.127 |
| Lead Width | b | 0.508 | – | 0.771 |
| Thermal Pad Width | b2 | 4.95 | – | 5.46 |
| Lead Thickness | c | 0.46 | – | 0.61 |
| Thermal Pad Thickness | c2 | 0.46 | – | 0.89 |
| Molded Body Length | D | 5.97 | – | 6.22 |
| Thermal Pad Length | D1 | 5.21 | – | – |
| Total Width | E | 6.35 | – | 6.73 |
| Thermal Pad Width | E1 | 4.32 | – | – |
| Overall Length | H | 9.39 | – | 10.41 |
| Foot Length | L | 1.39 | – | 1.78 |
| Tab Length | L1 | | 1.067 REF | |
| Lead Length | L2 | | 2.74 BSC | |
| Foot Angle | θ | 0° | – | 10° |
| Mold Draft Angle | θ1 | 0° | – | 15° |

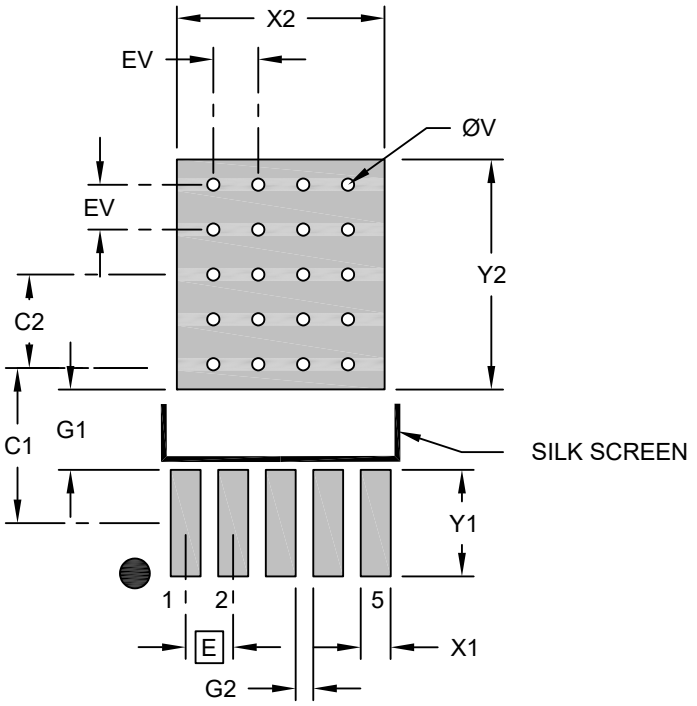
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1168 Rev A Sheet 2 of 2

## 5-Lead Transistor Outline (9EA) - [TO-252]
## Option "A"

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Center Pad Width | X2 | | | 5.55 |
| Center Pad Length | Y2 | | | 6.15 |
| Contact Pad Spacing | C1 | | 4.15 | |
| Contact Pad Spacing | C2 | | 2.50 | |
| Contact Pad Width (X5) | X1 | | | 0.80 |
| Contact Pad Length (X5) | Y1 | | | 2.85 |
| Contact Pad to Center Pad (X5) | G1 | 2.15 | | |
| Contact Pad to Contact Pad (X4) | G2 | 0.47 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3168 Rev A

# 7. Revision History

| Doc. Rev. | Date | Section | Comments |
|---|---|---|---|
| A | September 2025 | — | Initial release of this document. |
| B | January 2026 | Whole document | Added adjustable output version |
| | | Adjustable Output Voltage (ADJ), LDO Output Voltage | Added new sections |

## Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

| PART NO. | [T] | -XX(X) | XX | X | /XX(X) | XXX |
|---|---|---|---|---|---|---|
| Device | Tape and Reel(1) | Voltage | Feature Code | Temperature Range | Package | Qualification |

| | | |
|---|---|---|
| **Device:** | MCP1781: 200 mA High-Voltage Automotive LDO | |
| **Media Type(1):** | (blank) | = Tube (80/Tube – 9EA; 1/Tube – DC) |
| | T | = Tape and Reel (2,500/Reel – 9EA; 4,000/Reel – DC) |
| **Voltage:** | 33 | = 3.3V |
| | 50 | = 5.0V |
| | ADJ | = Adjustable Output Voltage |
| **Feature Code:** | 02 | = Fixed Output Voltage |
| | (blank) | = Adjustable Output Voltage |
| **Temperature Range:** | H | = −40°C to +150°C (High) |
| **Package:** | 9EA | = 5-Pin TO-252 Transistor Outline (Code: 9EA) |
| | DC | = 5-Pin SOT-223 Plastic Small Outline Transistor (Code: N7X) |
| **Qualification:** | (blank) | = Standard Part |
| | VAO | = AEC-Q100 Automotive Qualified |

Examples:

- MCP1781-3302H/9EA: 200 mA High-Voltage Automotive LDO, Tube, 3.3V Fixed Output Voltage, High Temperature Range, TO-252 Package
- MCP1781T-5002H/DC: 200 mA High-Voltage Automotive LDO, Tape and Reel, 5.0V Fixed Output Voltage, High Temperature Range, SOT-223 Package
- MCP1781-ADJH/9EA: 200 mA High-Voltage Automotive LDO, Tube, Adjustable Output Voltage, High Temperature Range, TO-252 Package
- MCP1781-3302H/DCVAO: 200 mA High-Voltage Automotive LDO, Tube, 3.3V Fixed Output Voltage, High Temperature Range, SOT-223 Package, AEC-Q100 Automotive Qualified
- MCP1781-5002H/9EAVAO: 200 mA High-Voltage Automotive LDO, Tube, 5.0V Fixed Output Voltage, High Temperature Range, TO-252 Package, AEC-Q100 Automotive Qualified
- MCP1781T-ADJH/DCVAO: 200 mA High-Voltage Automotive LDO, Tape and Reel, Adjustable Output Voltage, High Temperature Range, SOT-223 Package, AEC-Q100 Automotive Qualified

**Notes:**

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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