

# FQB7N60 / FQI7N60

## N-Channel QFET® MOSFET

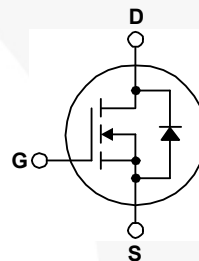
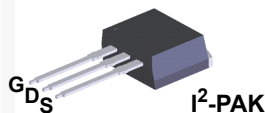
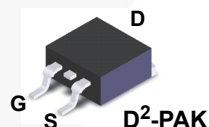
800 V, 3.9 A, 3.6 Ω

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 3.9 A, 800 V,  $R_{DS(on)} = 3.6 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 1.95 A$
- Low Gate Charge (Typ. 19 nC)
- Low  $C_{rss}$  (Typ. 8.6 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQB7N60TM FQB7N60TM_WS FQI7N60TU	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	7.4	A
		4.7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	29.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	580	mJ
$I_{AR}$	Avalanche Current (Note 1)	7.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	14.2	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ C$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ C$ ) - Derate above $25^\circ C$	142	W
		1.14	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FQB7N60TM FQB7N60TM_WS FQI7N60TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB7N60TM	FQB7N60	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units
FQB7N60TM_WS	FQB7N60S	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units
FQI7N60TU	FQI7N60	I <sup>2</sup> -PAK	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.67	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.7 A	--	0.8	1.0	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3.7 A	--	6.4	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	1100	1430	pF
C <sub>oss</sub>	Output Capacitance		--	135	175	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	16	21	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 7.4 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	30	70	ns
t <sub>r</sub>	Turn-On Rise Time		--	80	170	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	65	140	ns
t <sub>f</sub>	Turn-Off Fall Time		--	60	130	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 7.4 A, V <sub>GS</sub> = 10 V  (Note 4)	--	29	38	nC
Q <sub>gs</sub>	Gate-Source Charge		--	7	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	14.5	--	nC

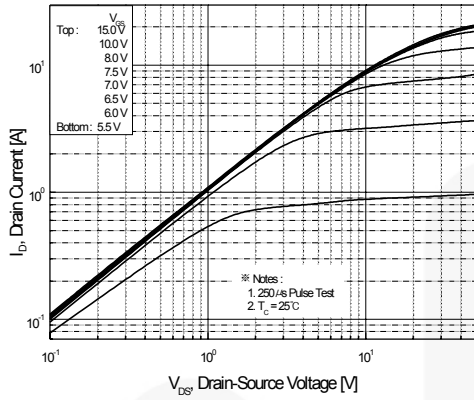
### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	7.4	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	29.6	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.4 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.4 A, di <sub>F</sub> / dt = 100 A/μs	--	320	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.4	--	μC

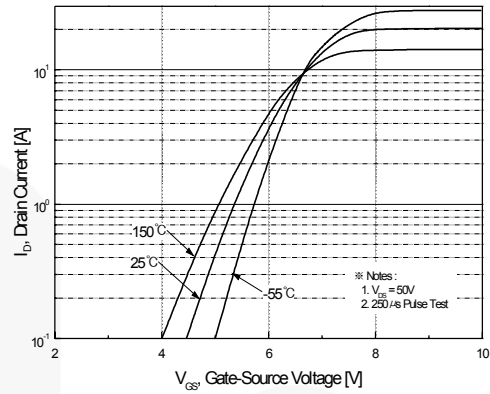
#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 19.5 mH, I<sub>AS</sub> = 7.4 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 7.4 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

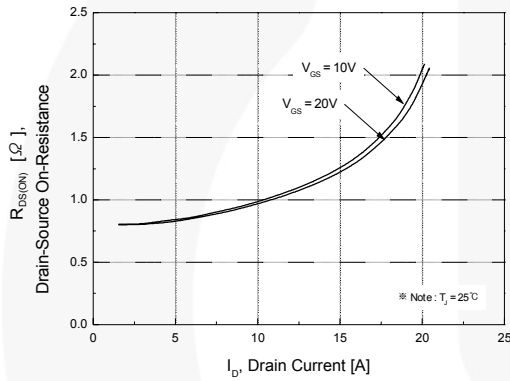
## Typical Characteristics



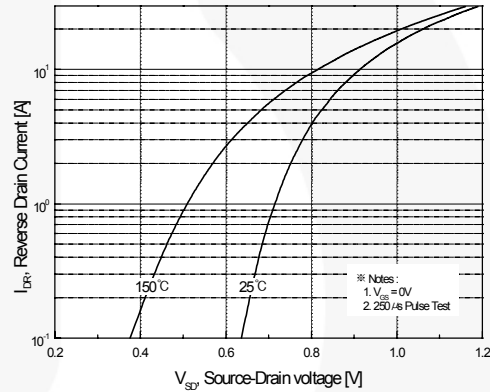
**Figure 1. On-Region Characteristics**



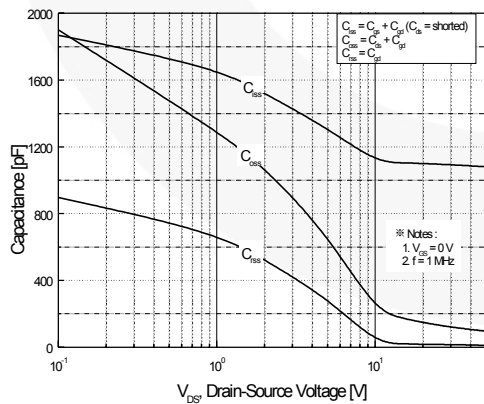
**Figure 2. Transfer Characteristics**



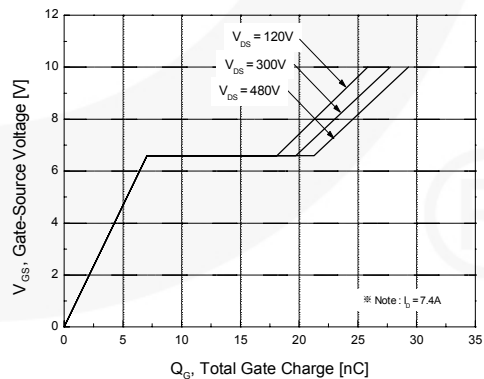
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

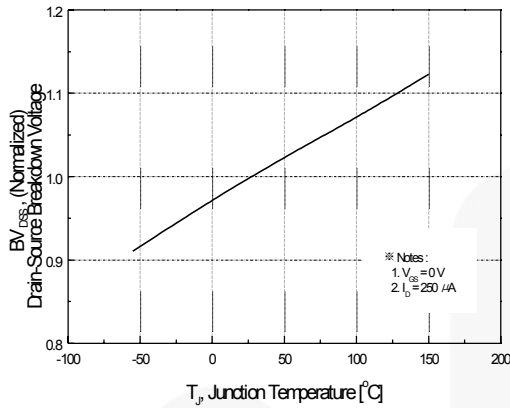


**Figure 5. Capacitance Characteristics**

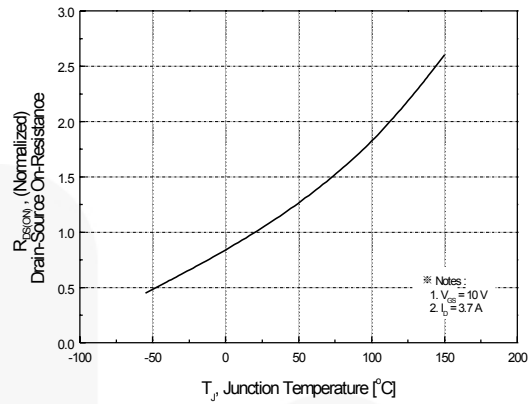


**Figure 6. Gate Charge Characteristics**

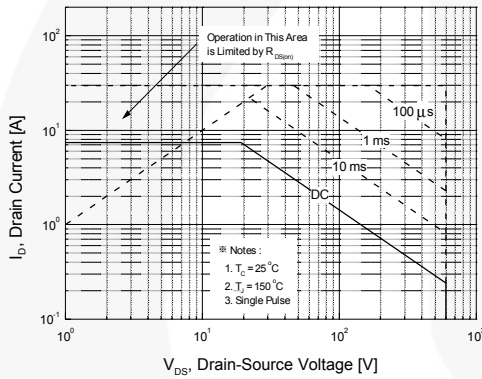
**Typical Characteristics** (Continued)



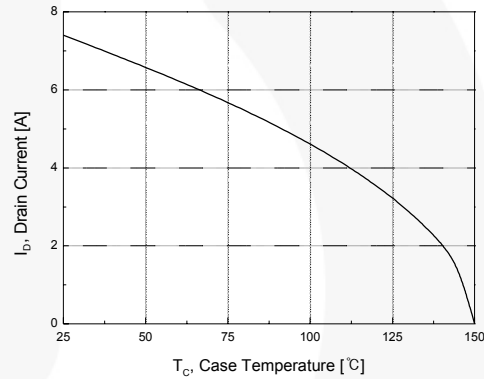
**Figure 7. Breakdown Voltage Variation vs. Temperature**



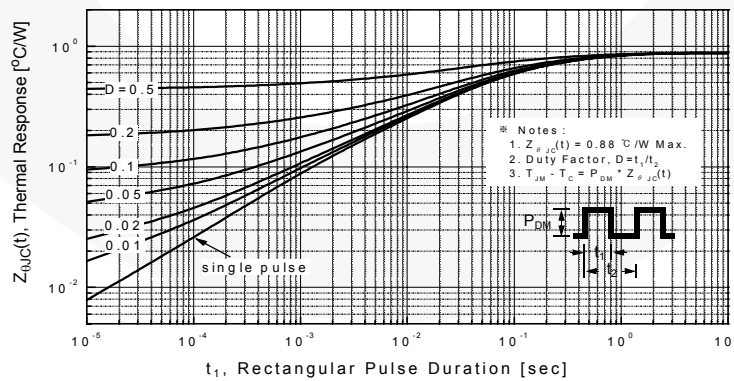
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

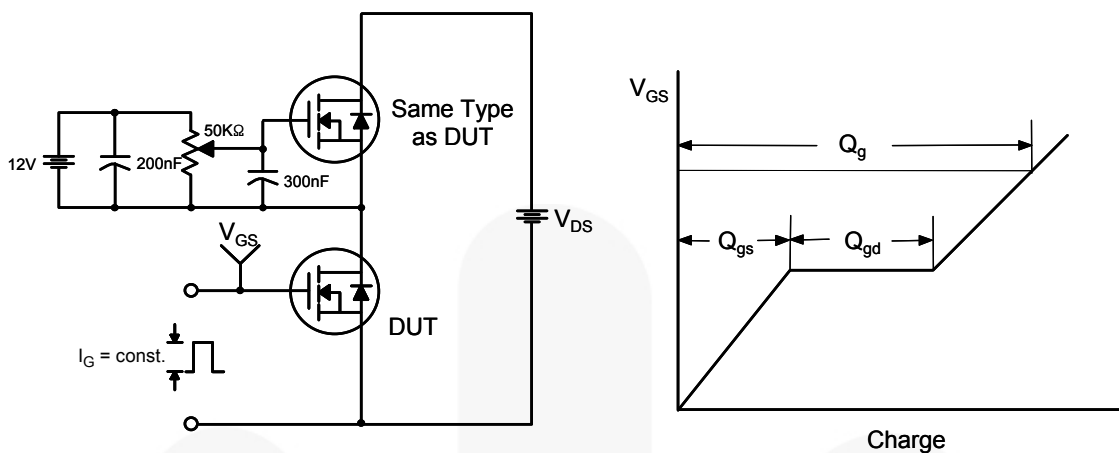


Figure 12. Gate Charge Test Circuit & Waveform

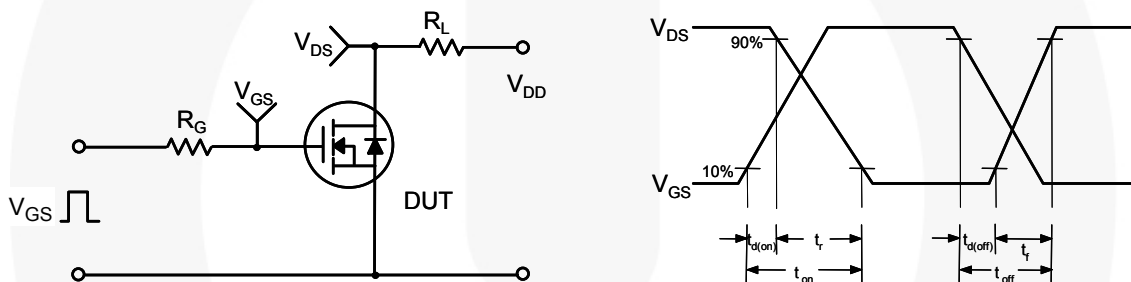


Figure 13. Resistive Switching Test Circuit & Waveforms

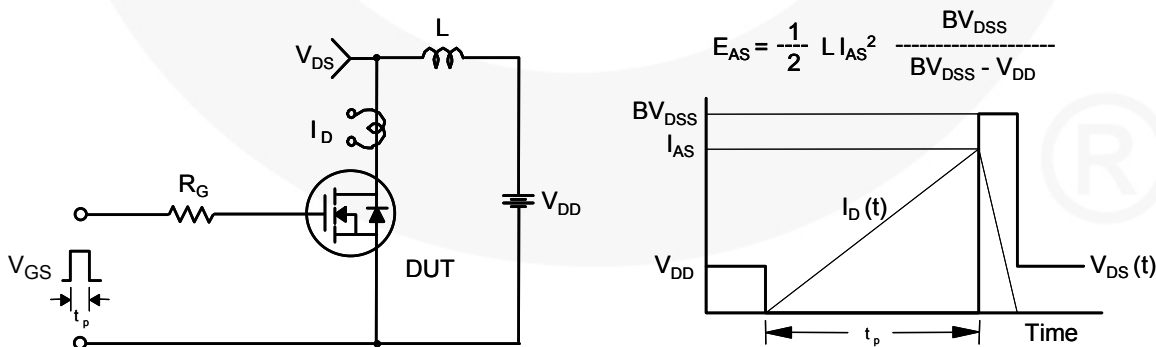


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

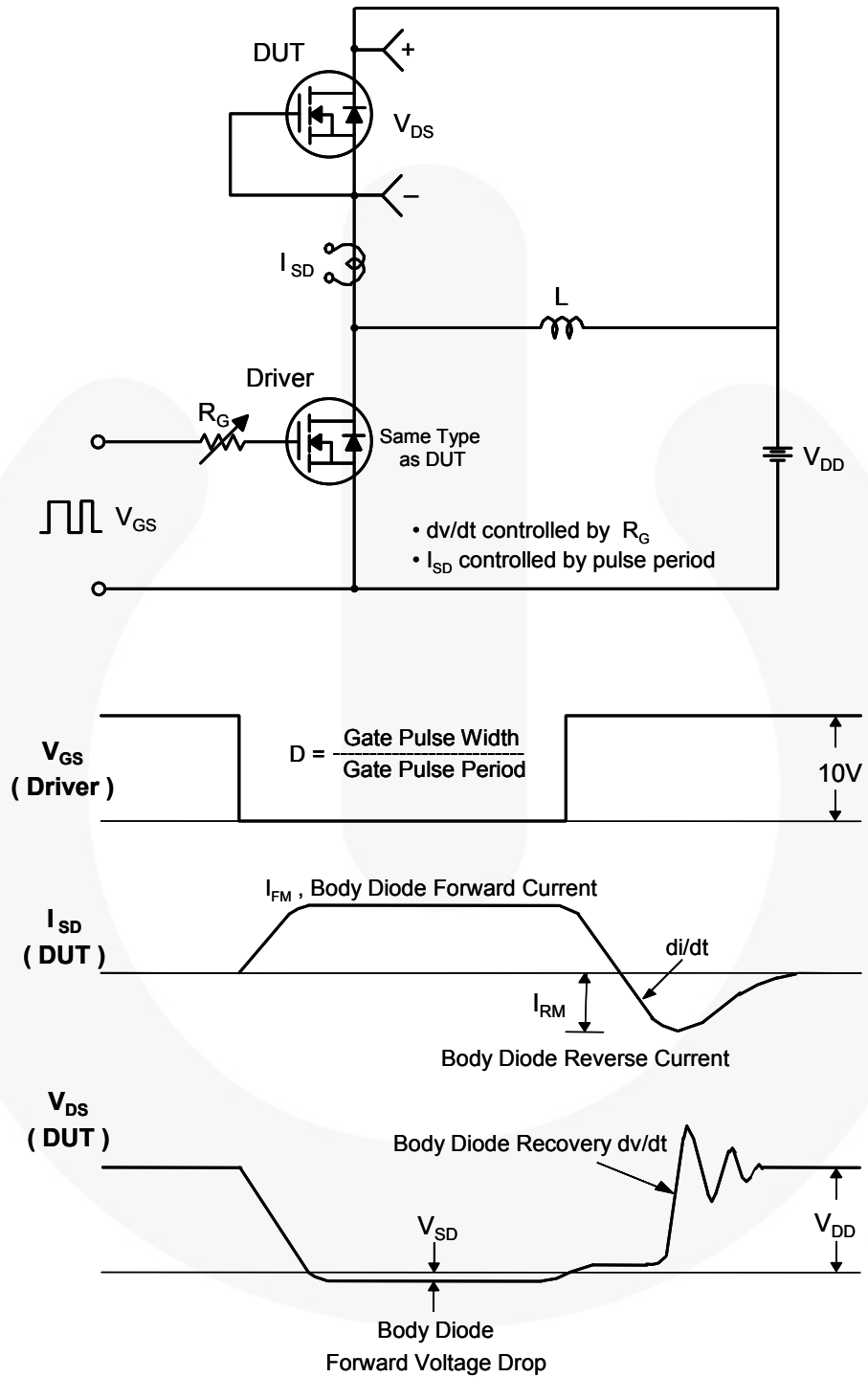
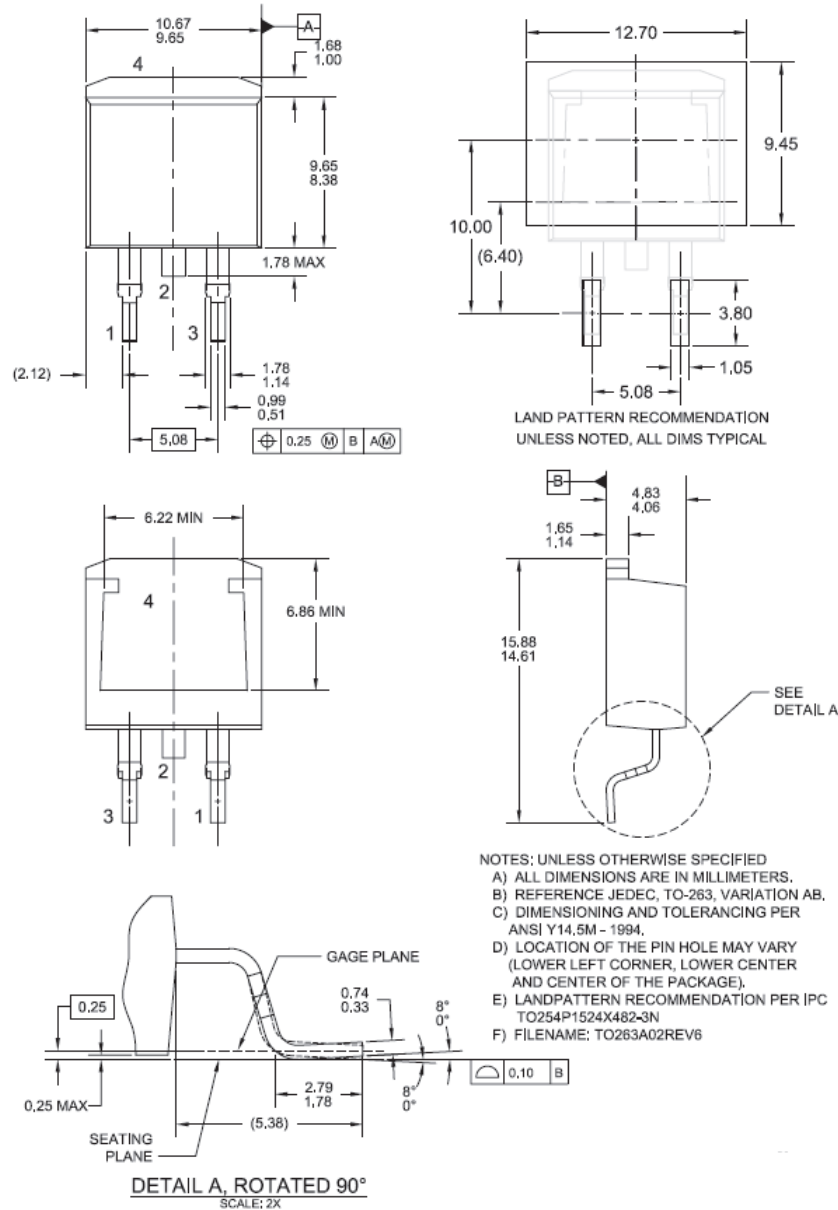


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## Mechanical Dimensions



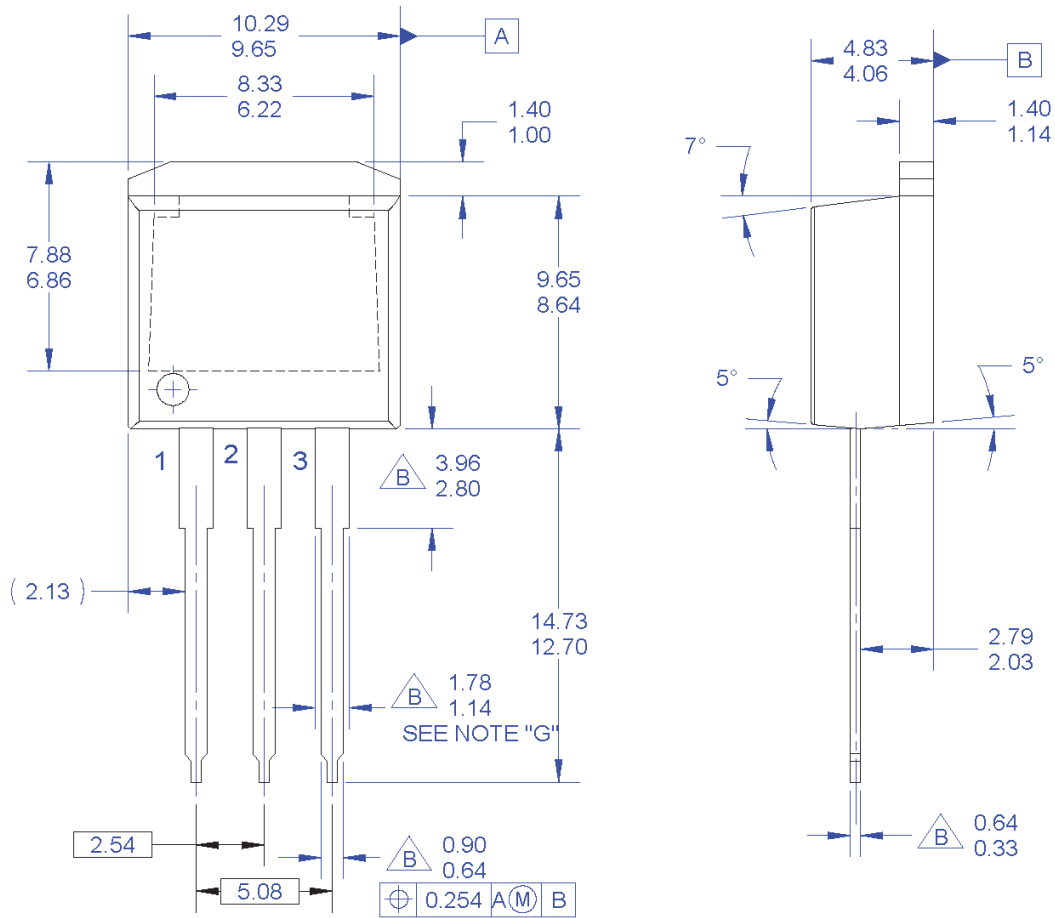
**Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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## Mechanical Dimensions



### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- $\triangle B$  DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

**Figure 17. TO262 (I<sup>2</sup>PAK), Molded, 3-Lead, Jedec Variation AA**

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| FAST®                    | SPM®                    | SuperSOT™-8                                     | VoltagePlus™     |
| FastvCore™               | SPM®                    | SupreMOS®                                       | XS™              |
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| FPS™                     | SPM®                    |   |                  |

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**Definition of Terms**

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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