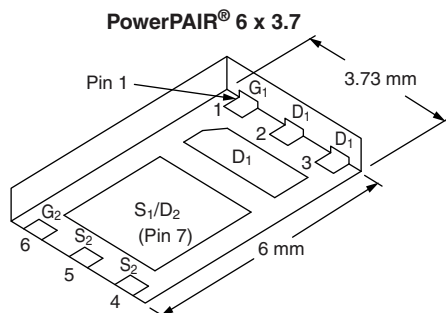




N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1 and Channel-2	30	0.0120 at V _{GS} = 10 V	16 ^a	6.8 nC
		0.0145 at V _{GS} = 4.5 V	16 ^a	



Ordering Information:

SiZ702DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

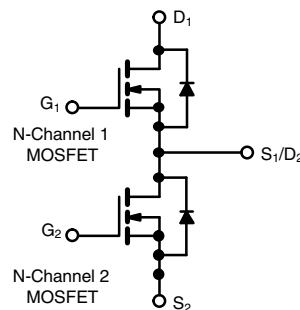
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Notebook System Power
- POL
- Low Current DC/DC



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V _{DS}	30		V
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	16 ^a		A
		16 ^a		
		13.8 ^{b, c}	14 ^{b, c}	
		11 ^{b, c}	11.2 ^{b, c}	
Pulsed Drain Current	I _{DM}	50		
Source Drain Current Diode Current	I _S	16 ^a	16 ^a	
		3.2 ^{b, c}	3.7 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	18		
Single Pulse Avalanche Energy	E _{AS}	16		mJ
Maximum Power Dissipation	P _D	27	30	W
		17.4	19	
		3.9 ^{b, c}	4.5 ^{b, c}	
		2.5 ^{b, c}	2.9 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	24	32	21	28	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	3.5	4.6	3.2	4.2	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 67 °C/W for channel-1 and for channel-2.

SiZ702DT

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1 Ch-2	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	Ch-1 Ch-2		33		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1 Ch-2		- 5		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1 Ch-2	1		2.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	Ch-1 Ch-2			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	Ch-1 Ch-2			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1 Ch-2			5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1 Ch-2	20			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 13.8 A	Ch-1 Ch-2		0.010	0.012	Ω
		V _{GS} = 4.5 V, I _D = 12.6 A	Ch-1 Ch-2		0.012	0.0145	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 13.8 A	Ch-1 Ch-2		47		S
Dynamic ^a							
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1 Ch-2		790		pF
Output Capacitance	C _{oss}		Ch-1 Ch-2		190		
Reverse Transfer Capacitance	C _{rss}		Ch-1 Ch-2		76		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 13.8 A	Ch-1 Ch-2		14	21	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 13.8 A	Ch-1 Ch-2		6.8	11	
Gate-Source Charge	Q _{gs}		Ch-1 Ch-2		2.6		
Gate-Drain Charge	Q _{gd}		Ch-1 Ch-2		1.9		
Gate Resistance	R _g	f = 1 MHz	Ch-1 Ch-2	0.4	2	4	Ω

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≡ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1 Ch-2		15	25	ns
Rise Time	t _r		Ch-1 Ch-2		12	20	
Turn-Off Delay Time	t _{d(off)}		Ch-1 Ch-2		20	30	
Fall Time	t _f		Ch-1 Ch-2		10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≡ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1 Ch-2		10	15	
Rise Time	t _r		Ch-1 Ch-2		12	20	
Turn-Off Delay Time	t _{d(off)}		Ch-1 Ch-2		20	30	
Fall Time	t _f		Ch-1 Ch-2		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1 Ch-2			16	A
Pulse Diode Forward Current ^a	I _{SM}		Ch-1 Ch-2			50	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1 Ch-2		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1 Ch-2		20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}		Ch-1 Ch-2		10	20	nC
Reverse Recovery Fall Time	t _a		Ch-1 Ch-2		11		ns
Reverse Recovery Rise Time	t _b		Ch-1 Ch-2		9		

Notes:

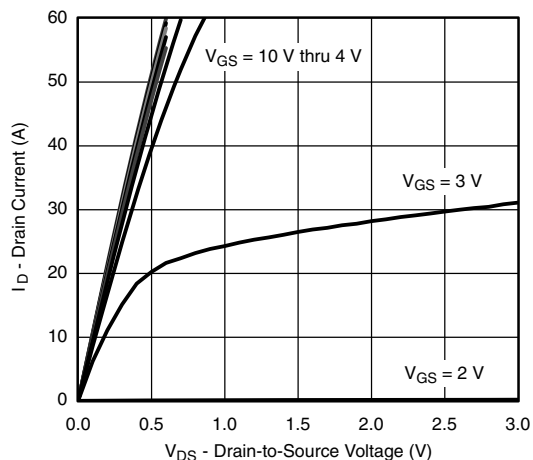
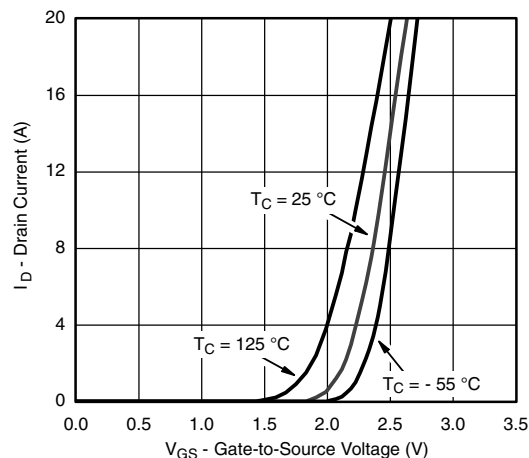
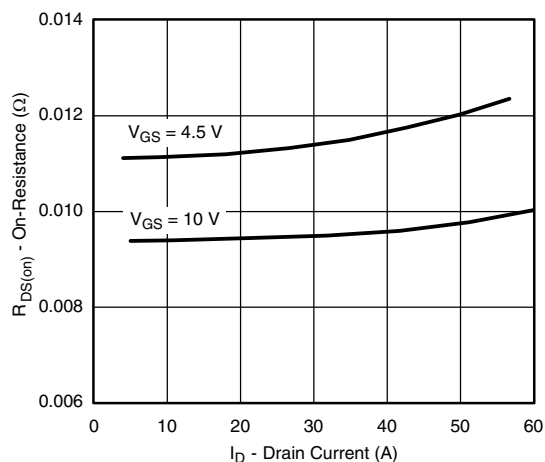
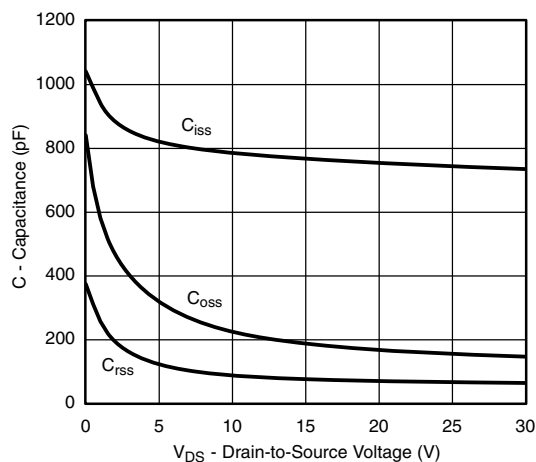
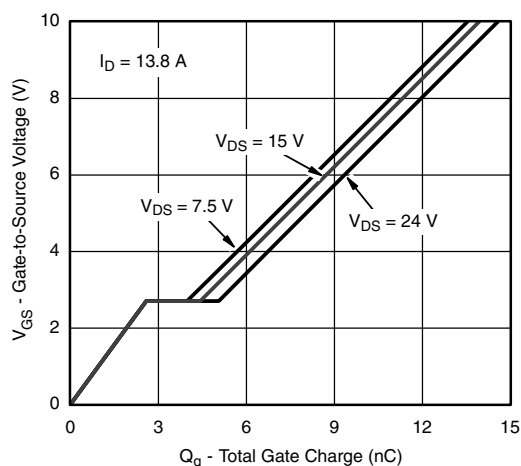
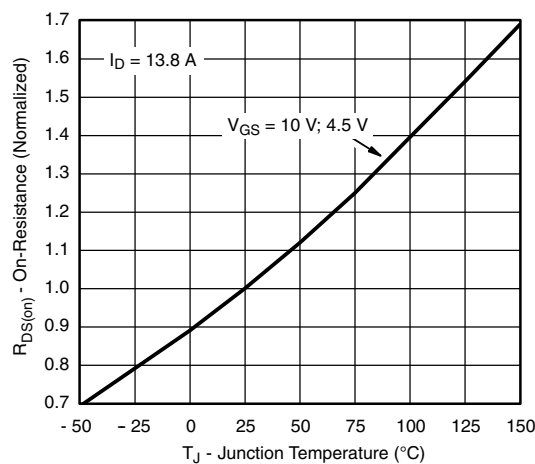
a. Guaranteed by design, not subject to production testing.

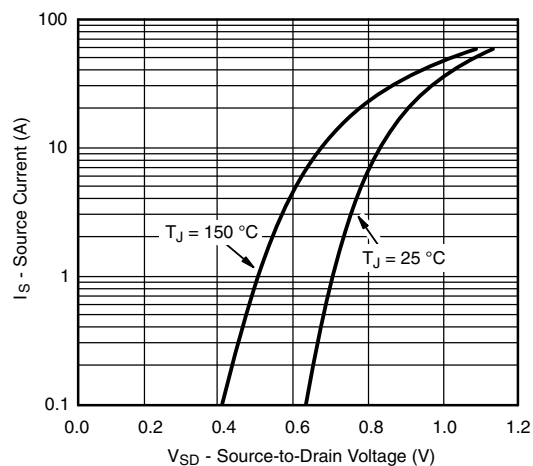
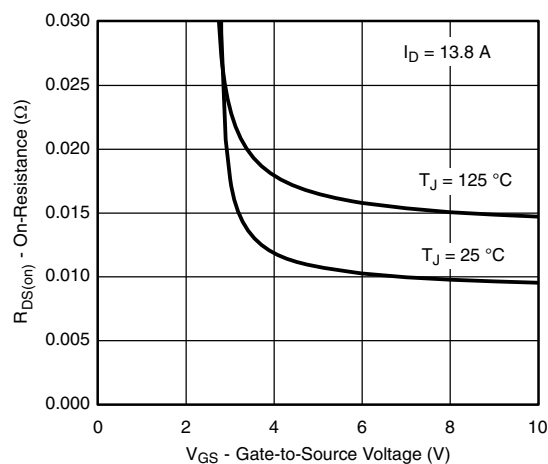
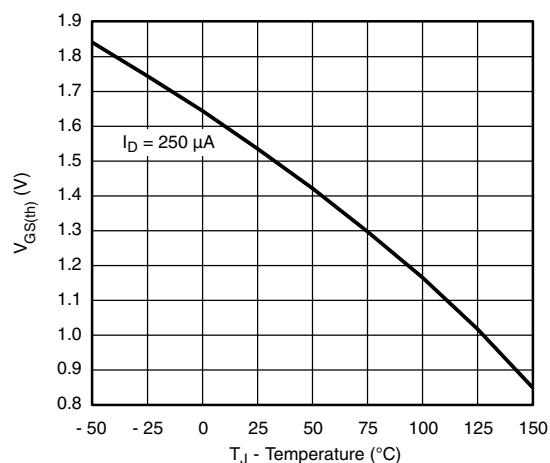
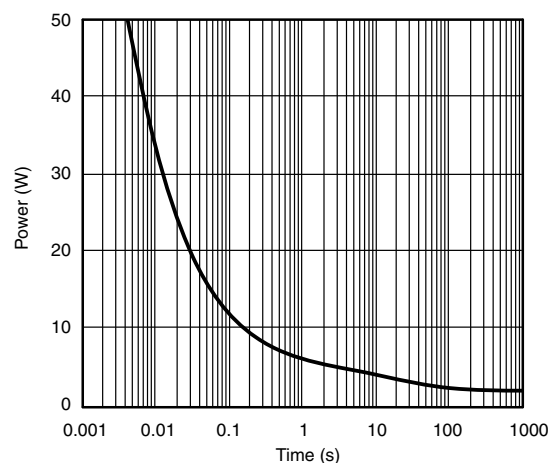
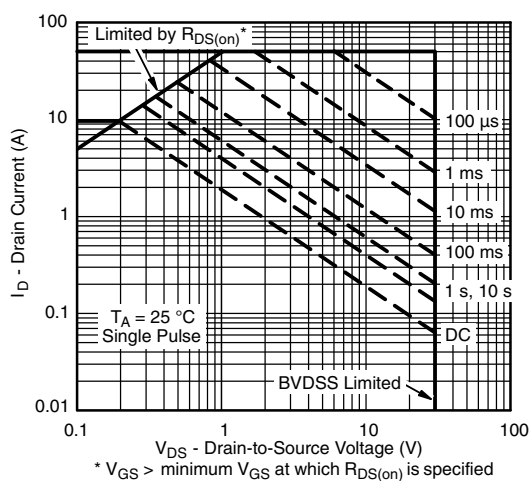
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Si702DT

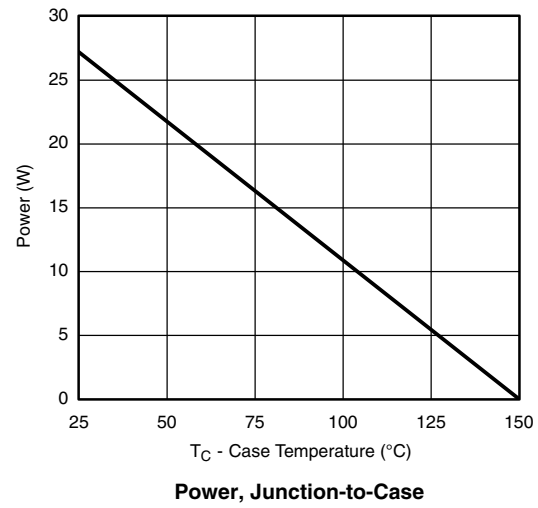
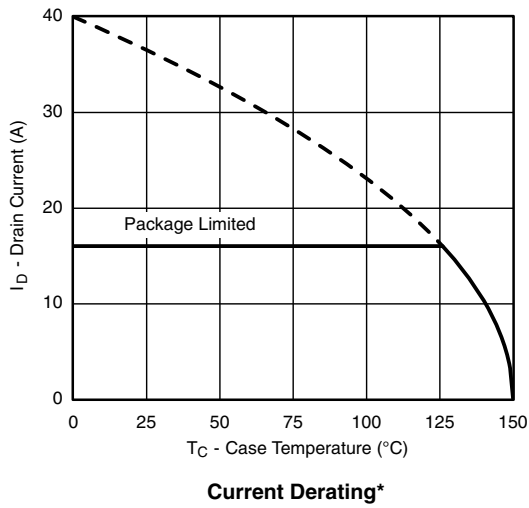
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**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

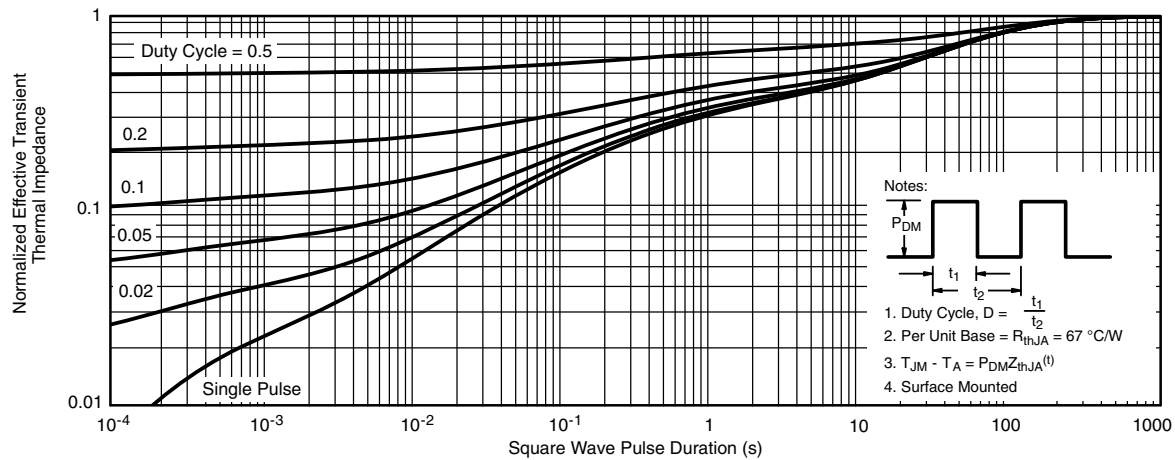

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

SiZ702DT

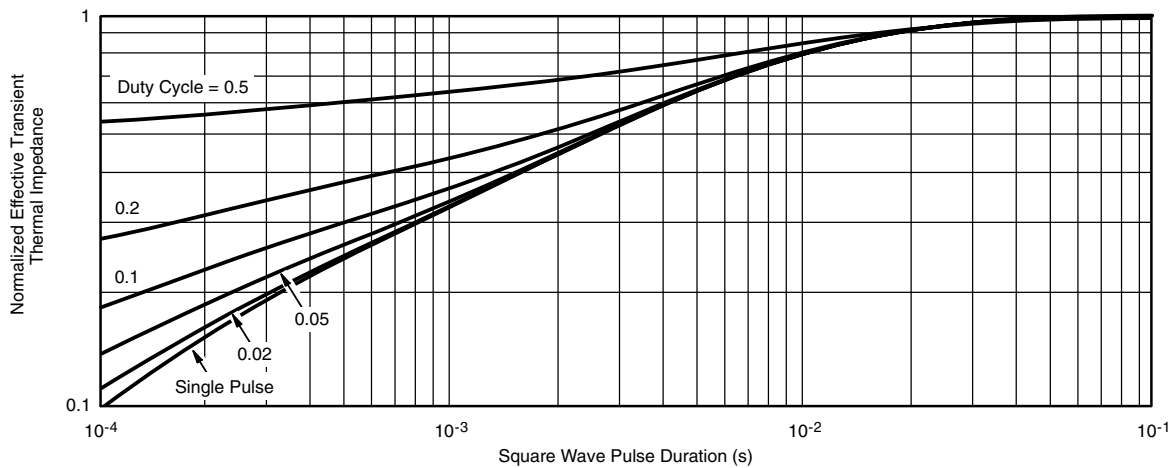
Vishay Siliconix

**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


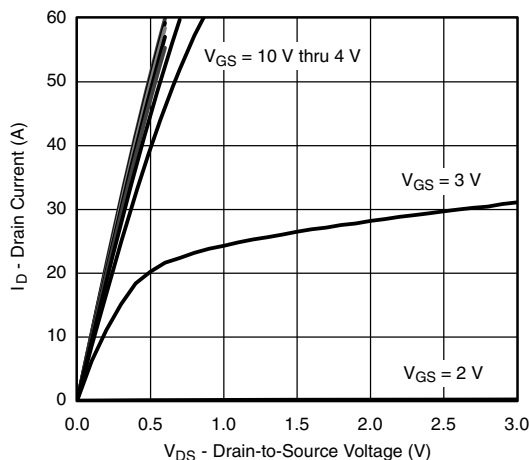
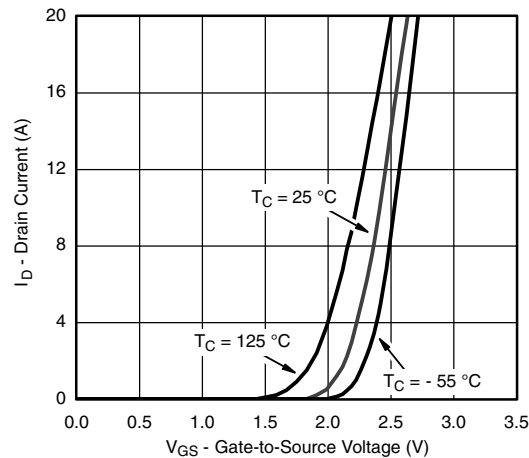
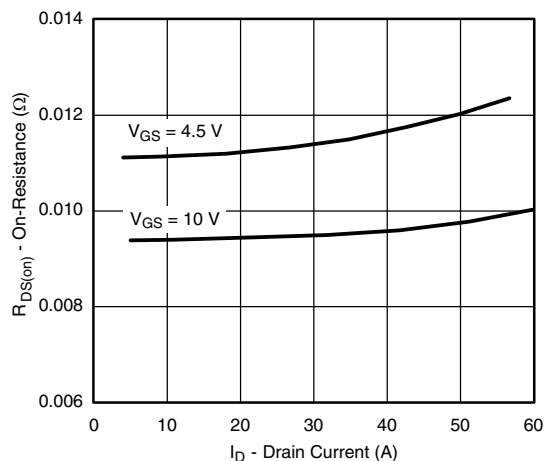
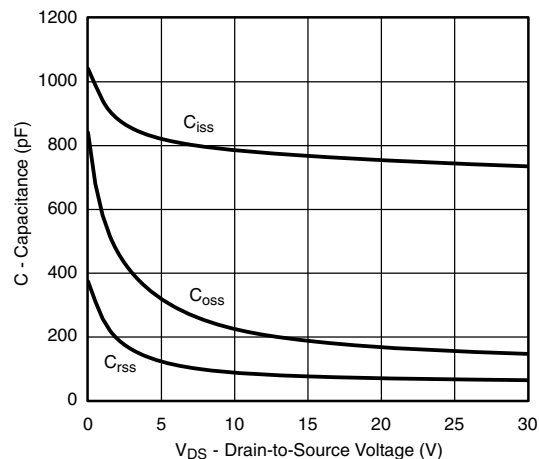
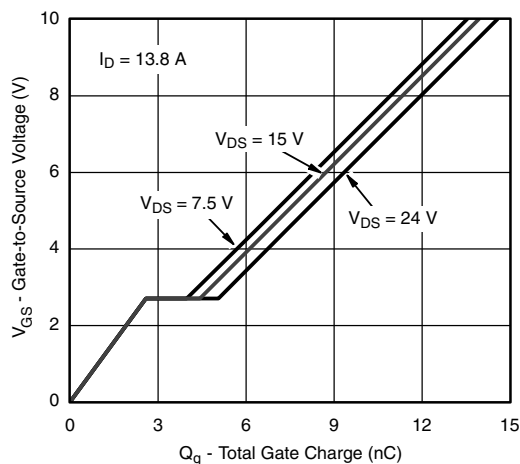
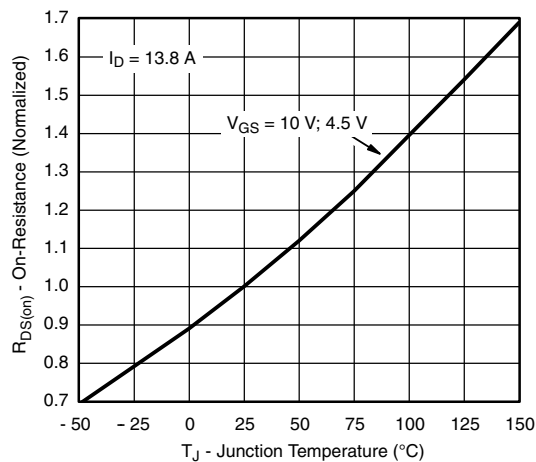
Normalized Thermal Transient Impedance, Junction-to-Ambient

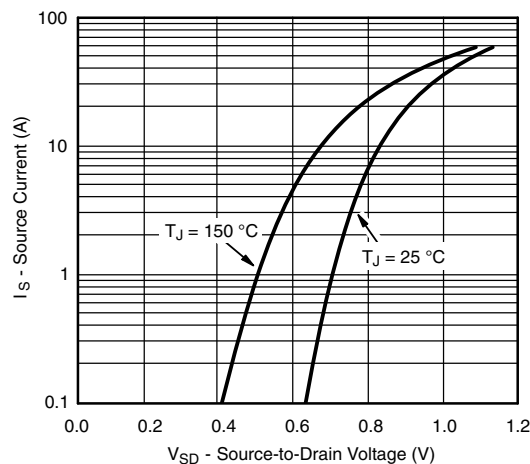
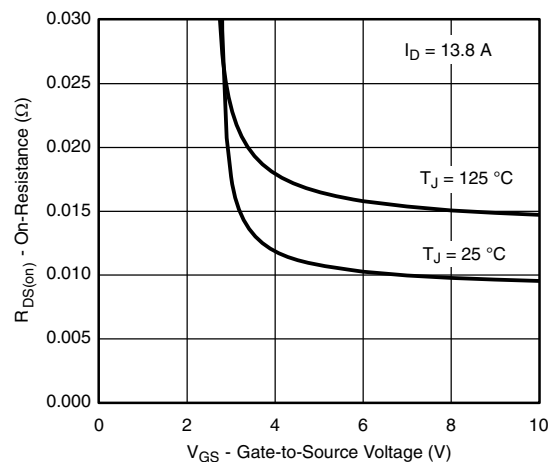
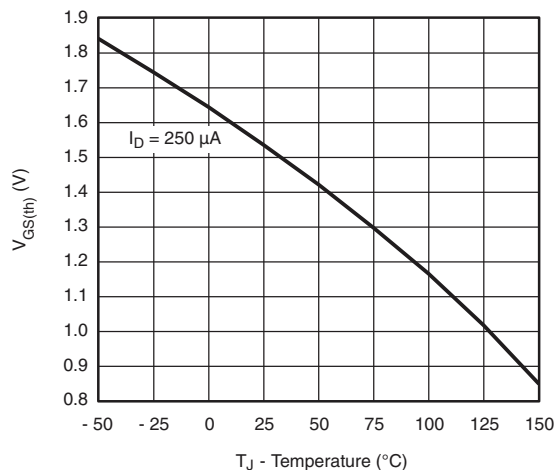
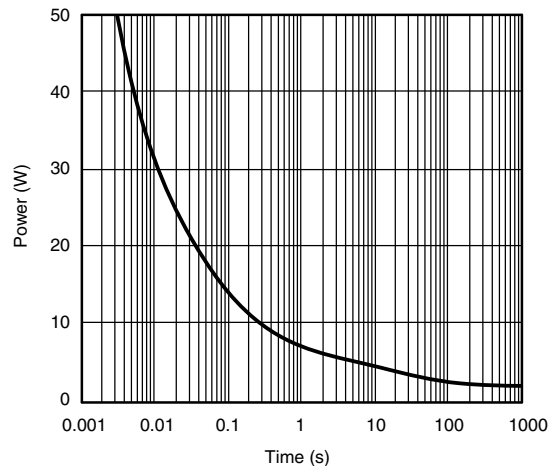
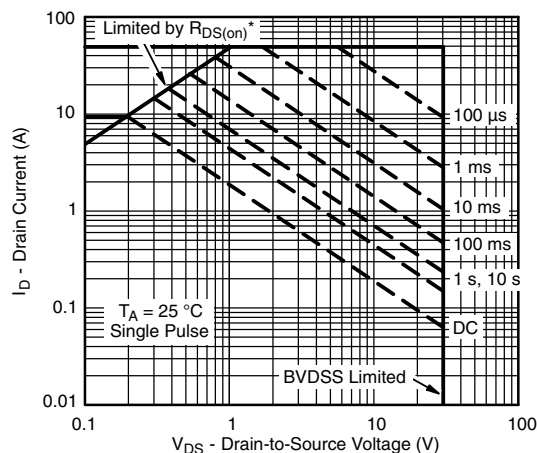


Normalized Thermal Transient Impedance, Junction-to-Case

SiZ702DT

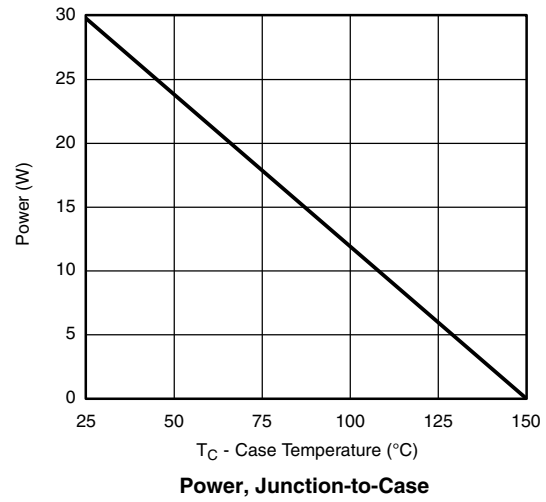
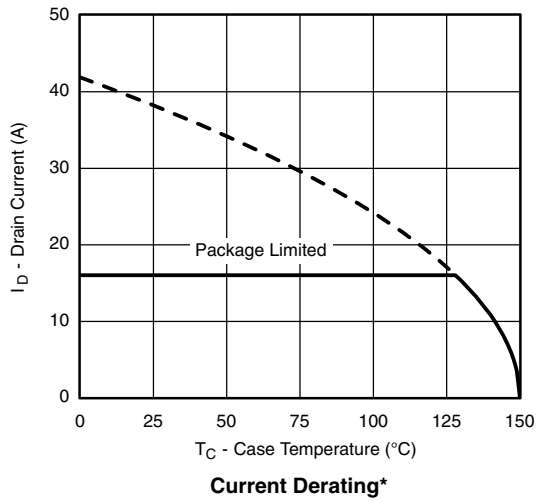
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**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

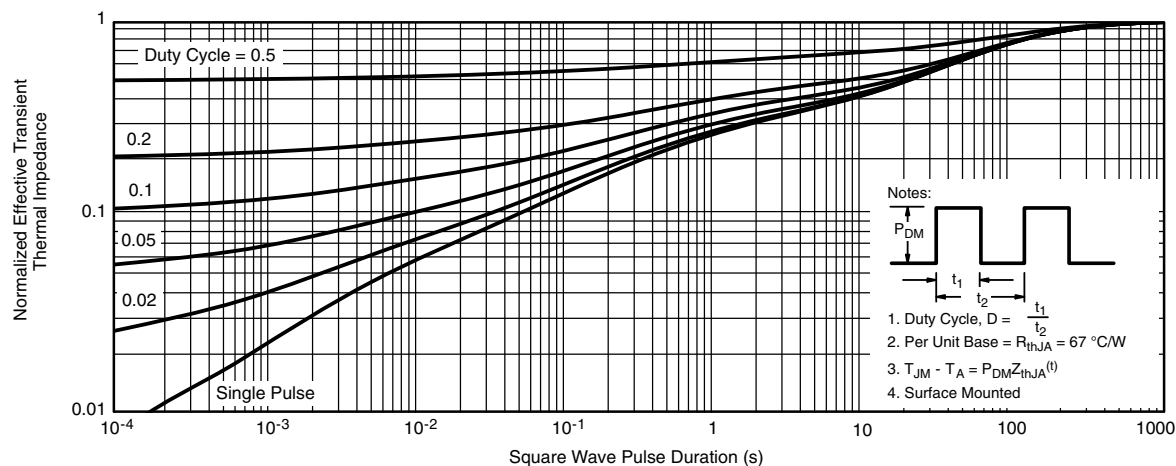
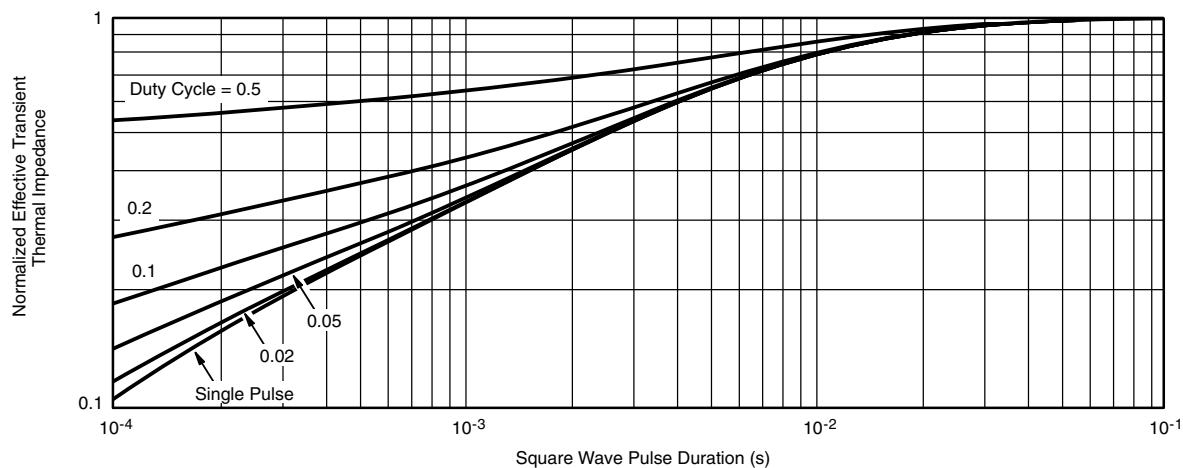

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient
 * $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

SiZ702DT

Vishay Siliconix

**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65525.

PowerPAIR™ 6 x 3.7 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08 DWG: 5979						

Technical drawing of a mechanical part, showing dimensions in inches and millimeters. The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 0.3520 (8.941)
- Overall height: 0.4390 (11.151)
- Top edge features:
 - Left to center: 0.0220 (0.559)
 - Center to right: 0.0190 (0.483)
- Central rectangular feature:
 - Width: 0.1040 (2.642)
 - Height: 0.1070 (2.718)
 - Internal horizontal spacing: 0, 0.03
 - Internal vertical spacing: 0, 0
- Bottom edge features:
 - Left to center: 0.0220 (0.559)
 - Center to right: 0.0380 (0.965)
- Bottom edge features (continued):
 - Left to center: 0.0170 (0.432)
 - Center to right: 0.0170 (0.432)

Side View Dimensions:

- Overall width: 0.0500 (1.27)
- Overall height: 0.0380 (0.965)
- Top edge features:
 - Left to center: 0.0170 (0.432)
 - Center to right: 0.0170 (0.432)
- Central rectangular feature:
 - Width: 0.0500 (1.27)
 - Height: 0.0380 (0.965)
 - Internal horizontal spacing: 0, -0.0645
- Bottom edge features:
 - Left to center: -0.05, -0.11
 - Center to right: 0, -0.11

Other Dimensions:

- Top edge feature: 0.0170 (0.432)
- Bottom edge feature: 0.0170 (0.432)

Notes:

- 1

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1



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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.