PIC24FV32KA304 Family Silicon Errata and Data Sheet Clarification

The PIC24FV32KA304 family devices that you have received conform functionally to the current Device Data Sheet (DS30009995**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FV32KA304 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A7**).

Data sheet clarifications and corrections start on Page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value will appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FV32KA304 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A4	A6	A7			A4	A6	A7
PIC24F32KA304	4516h	0004h	0006h	00007h	PIC24FV32KA304	4517h	0004h	0006h	0007h
PIC24F32KA302	4512h				PIC24FV32KA302	4513h			
PIC24F32KA301	4518h				PIC24FV32KA301	4519h			
PIC24F16KA304	4506h				PIC24FV16KA304	4507h			
PIC24F16KA302	4502h				PIC24FV16KA302	4503h			
PIC24F16KA301	4508h				PIC24FV16KA301	4509h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of the configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FXXKA1XX/FVXXKA3XX Family Flash Programming Specifications"* (DS30009919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A4	A6	A7
Core	Low-Voltage Regulator	1.	High-voltage programming entry unavailable in low-voltage Sleep modes.	X		
Reset	BOR	2.	Unexpected BOR events when BOR is disabled in Sleep mode.	X	X	X
A/D	Threshold Detect	3.	Auto-scan feature may not trigger correctly in Sleep mode.	X		
UART	TX Buffer	4.	Out-of-order transmit data when buffer is filled.	X		
UART	Transmit	5.	UTXBF flag may not indicate correctly.	X		
A/D	Threshold Detect	6.	Current in Auto-Scan mode may exceed expected values.	X		
A/D	Threshold Detect	7.	Interrupt may not trigger in certain Auto-Scan modes.	X		
HLVD	DC18 Value Changes	8.	Change in trip points.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A7**).

1. Module: Core (Low-Voltage Regulator)

When operating in Low-Voltage Sleep mode, LVREN = 1 (RCON<12>) and LVRCFG = 0 (FPOR<2>), the device may not be able to enter programming modes using high-voltage entry (V_{IHH} applied to MCLR).

Work around

If entry into a programming mode is required while the device is in Low-Voltage Sleep mode, use low-voltage entry into programming. Verify that MCLR functionality is enabled, MCLRE = 1 (FPOR<7>), before attempting programming.

Affected Silicon Revisions

A4	A6	A7					
X							

2. Module: Reset (BOR)

Under certain conditions, the device may improperly perform a Brown-out Reset upon wake-up from a Sleep mode. This has been observed under two conditions:

1. When the BOR is disabled in Sleep mode, BOREN<1:0> = 10 (FPOR<1:0>), a BOR may occur when the device wakes from Sleep, regardless of the supply voltage.
2. When the BOR is configured for software control (BOREN<1:0> = 01), the device enters and wakes from Sleep normally while the BOR is disabled in software, SBOREN = 0 (RCON<13>). However, if the BOR was disabled prior to entering Sleep mode and is subsequently enabled after waking from Sleep, a BOR may occur, regardless of the supply voltage.

BOR functions normally when it is always enabled or disabled (BOREN<1:0> = 11 or 00).

Work around

Do not use Sleep mode when BOREN<1:0> = 10.

If the BOR is to operate under software control, always enable the HLVD module, HLVDEN = 1 (HLVDCON<15>), before enabling the BOR in software (SBOREN = 1). This procedure activates the internal band gap reference and assures its stability for the BOR circuit.

Affected Silicon Revisions

A4	A6	A7					
X	X	X					

3. Module: A/D (Threshold Detect)

When the auto-scan feature of the Threshold Detect is enabled (AD1CON5<15> = 1), automatic scan may fail when these conditions occur together:

- the Device is in Sleep mode, and
- Timer1 is selected as the sample trigger clock source (AD1CON1<7:4> = 0101).

Timer1 and other timers will function correctly as sample triggers in other power-saving modes, such as Idle mode.

Work around

If auto-scan functionality is required during Sleep, use INT0 as the sample trigger.

Affected Silicon Revisions

A4	A6	A7					
X							

4. Module: UART (TX Buffer)

If the transmit buffer is filled sequentially with four characters, the characters may not be transmitted in the correct order.

Work around

Do not completely fill the buffer before transmitting data; send three characters or less at a time.

Affected Silicon Revisions

A4	A6	A7					
X							

5. Module: UART (Transmit)

The UARTx Transmit Buffer Full flag, UTXBF (UxSTA<9>), may become cleared before data starts moving out of the full buffer. If the flag is used to determine when data can be written to the buffer, new data may not be accepted and data may not be transmitted.

Work around

Poll the Transmit Buffer Empty flag (TRMT, UxSTA<8>) to determine when the transmit buffer is empty and can be written to.

Alternatively, configure the UART to set the UARTx Transmit Interrupt Flag (UxTXIF) whenever a character is shifted into the Transmit Shift Register (UTXISEL<1:0> = 00). When a transmit interrupt occurs, this indicates that at least one buffer position is open and that the buffer can be written to.

Affected Silicon Revisions

A4	A6	A7					
X							

6. Module: A/D (Threshold Detect)

In Auto-Scan mode, with low power enabled (AD1CON5<15> = 1, AD1CON5<14> = 1) and the device in Sleep mode, the ADRC may not turn off between scans, resulting in a higher current draw than anticipated.

Work around

None.

Affected Silicon Revisions

A4	A6	A7					
X							

7. Module: A/D (Threshold Detect)

In Auto-Scan mode (AD1CON5<15> = 1), when the Auto-Scan Interrupt mode bits are set to '11' (AD1CON5<9:8> = 11), the highest number channel selected for scanning in AD1CSSL or AD1CSSH may not trigger an interrupt on a valid comparison.

Work around

Add a dummy channel to the scanning sequence. For example, when scanning AN0 and AN1, set AD1CSSL to 0x0007 or 0x8003, or whatever is practical given the implementation.

Also, if the highest number channel needs to be scanned, the AD1CHITH register can be polled to observe a valid comparison.

Affected Silicon Revisions

A4	A6	A7					
X							

8. Module: HLVD (DC18 Value Changes)

The maximum and minimum values of the High/Low-Voltage Detect Characteristics (DC18), shown in Table 29-4 of the data sheet, have changed for this revision. The new values are shown in Table 3.

Affected Silicon Revisions

A4	A6	A7					
X	X	X					

TABLE 3: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions:		**1.8V to 3.6V PIC24F32KA3XX** **2.0V to 5.5V PIC24FV32KA3XX**					
Operating temperature		-40°C ≤ TA ≤ +85°C for Industrial					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000(2)	—	—	2.01	V	
			HLVDL<3:0> = 0001	1.91	—	2.25	V	
			HLVDL<3:0> = 0010	2.12	—	2.48	V	
			HLVDL<3:0> = 0011	2.27	—	2.67	V	
			HLVDL<3:0> = 0100	2.36	—	2.76	V	
			HLVDL<3:0> = 0101	2.55	—	2.99	V	
			HLVDL<3:0> = 0110	2.79	—	3.27	V	
			HLVDL<3:0> = 0111	2.93	—	3.43	V	
			HLVDL<3:0> = 1000	3.06	—	3.60	V	
			HLVDL<3:0> = 1001(1)	3.23	—	3.79	V	
			HLVDL<3:0> = 1010(1)	3.40	—	4.00	V	
			HLVDL<3:0> = 1011(1)	3.61	—	4.23	V	
			HLVDL<3:0> = 1100(1)	3.83	—	4.49	V	
			HLVDL<3:0> = 1101(1)	4.08	—	4.80	V	
			HLVDL<3:0> = 1110(1)	4.38	—	5.14	V	

Note 1: These trip points should not be used on PIC24FXXKA30X devices.

2: This trip point should not be used on PIC24FVXXKA30X devices.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30009995**E**):

1. Module: Electrical Characteristics

Adds LPRC specifications at +125ºC, as shown in Table 29-21 below in **bold**.

TABLE 29-21: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
F20	Internal FRC Accuracy @ 8 MHz(1)						
	FRC	-2	—	+2	%	+25°C	3.0V ≤ VDD ≤ 3.6V, F device 3.2V ≤ VDD ≤ 5.5V, FV device
		-6	—	+6	%	-40°C ≤ TA ≤ +85°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device
F21	LPRC @ 31 kHz(2)	-15	—	15	%	-40°C ≤ TA ≤ +85°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device
		-30	**—**	**+30**	**%**	**-40°C ≤ TA ≤ +125°C**	

Note 1: Frequency is calibrated at +25°C and 3.3V. The OSCTUN bits can be used to compensate for temperature drift.

2: The change of LPRC frequency as VDD changes.

2. Module: CTMU

Adds the following note to **25.1 Measuring Capacitance**:

Note:	The ADC must be configured for 12-bit operation when used with the CTMU. 10-bit is not supported.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (3/2011)

Initial release of this document; issued for revision A4. Includes silicon issues 1 (Core, Low-Voltage Regulator) and 2 (Reset, BOR).

Rev B Document (5/2011)

Adds silicon issue 3 (A/D, Threshold Detect) to silicon revision A4.

Adds data sheet clarifications 1 (Overview and Other Locations), 2 (Overview) and 3 (A/D, Threshold Detect) for data sheet revision B.

Rev C Document (9/2011)

Adds silicon issues 4 (UART, TX Buffer), 5 (UART, Transmit), 6 (A/D, Threshold Detect), 7 (A/D, Threshold Detect) and 8 (HLVD, DC18 Value Changes) to silicon revision A4. Typographical correction in issue 1 (Core, Low-Voltage Regulator).

Adds data sheet clarifications 4 through 7 (A/D Converter), 8 and 9 (Comparator), 10 (Flash Program Memory), 11 (Electrical Specifications), 12 (A/D Converter) and 13 (Pin Diagrams) to data sheet revision B.

Rev D Document (8/2012)

Adds latest silicon revision (A6) and shows that both silicon issues 2 (Reset, BOR) and 8 (HLVD, DC18 Value Changes) are affected. Removes all data sheet clarifications that were addressed in the latest release of the data sheet.

Rev E Document (11/2013)

Adds data sheet clarification 1 (Electrical Characteristics).

Rev F Document (7/2015)

Adds current silicon revision A7.

Rev G Document (8/2017)

Adds Note 1 to HLVDL<3:0> = 1001 in silicon revision 8 (HLVD, DC18 Value Changes).

Rev H Document (10/2017)

Updates the data sheet reference to the latest revision (DS30009995**E**).

Removes data sheet data sheet clarification 1 (Electrical Characteristics) since this has been addressed in the latest revision of the data sheet.

Rev J Document (3/2018)

Adds data sheet clarification 1 (Electrical Characteristics).

Rev K Document (11/2025)

Adds data sheet clarification 2 (CTMU).

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