MIC3808/9

Push-Pull PWM Controller

Features

- Dual Output Drive Stages in Push-Pull Configuration
- Leading Edge Current-Sense Blanking
- 130 µA Typical Start-Up Current
- 1 mA Typical Run Current
- Operation to 1 MHz
- Internal Soft Start
- On-Chip Error Amplifier with 4 MHz Gain Bandwidth Product
- On-Chip V_{DD} Clamping
- Output Drive Stages Capable of 500 mA Peak Source Current, 1A Peak Sink Current

Applications

- High Efficiency “Brick” Power Supply Modules
  - Half Bridge Converters
  - Full Bridge Converters
  - Push-Pull Converters
  - Voltage-Fed Push-Pull Converters
- Telecom Equipment and Power Supplies
- Networking Power Supplies
- Industrial Power Supplies
- 42V Automotive Power Supplies
- Base Stations

General Description

The MIC3808 and MIC3809 are a family of complementary output push-pull PWM control ICs that feature high speed and low power consumption. The MIC3808/9 are ideal for telecom level (36V to 75V) isolated step down DC/DC conversion applications where high output current, small size, and high efficiency are required.

The dual-ended push-pull architecture of the MIC3808/9 allows more efficient utilization of the transformer than single-ended topologies, allowing smaller size DC/DC solutions.

Additionally, the out-of-phase push-pull topology allows a higher effective duty cycle, reducing input and output ripple as well as stress on the external components. The dead-time between the two outputs is adjustable between 60 ns to 200 ns, limiting the duty cycle of each output stage to less than 50%.

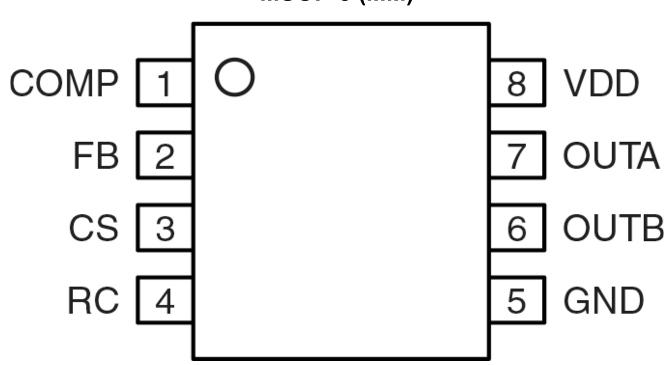
The MIC3808/9 are built on a low-power, high-speed BiCMOS process. The 130 µA start-up current and 1 mA run-current reduce the size of the start-up circuitry and allow high efficiency even at light loads. The high-speed internal 4 MHz error amplifier allows MIC3808/9 operation up to 1 MHz.

The MIC3808 has a turn-on threshold of 12.5V whereas the MIC3809 has a lower turn-on threshold of 4.3V. Both devices are available in SOP-8 and MSOP-8 package options with an operating range of –40°C to +85°C with –3.0V, –4.1V, –5.0V, and adjustable outputs.

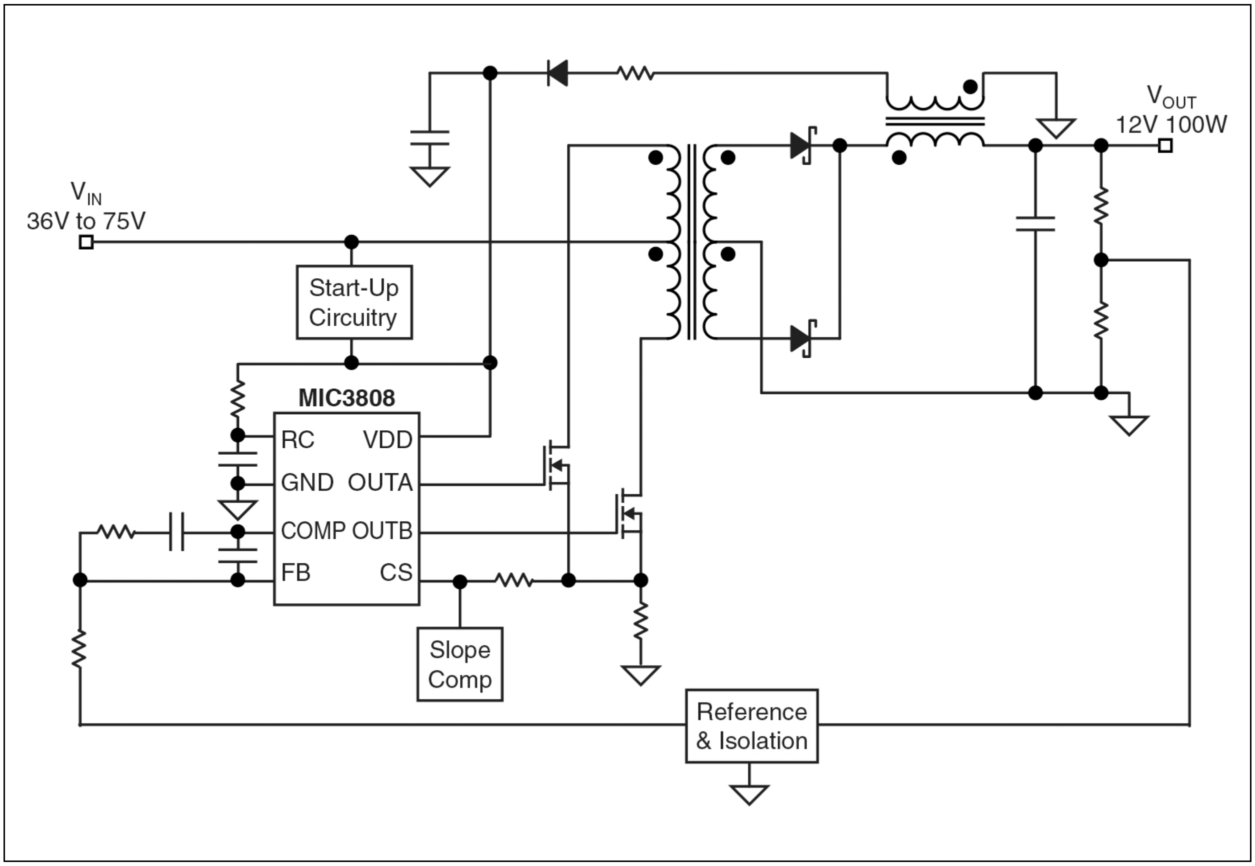
Package Types

SOIC-8 (M)

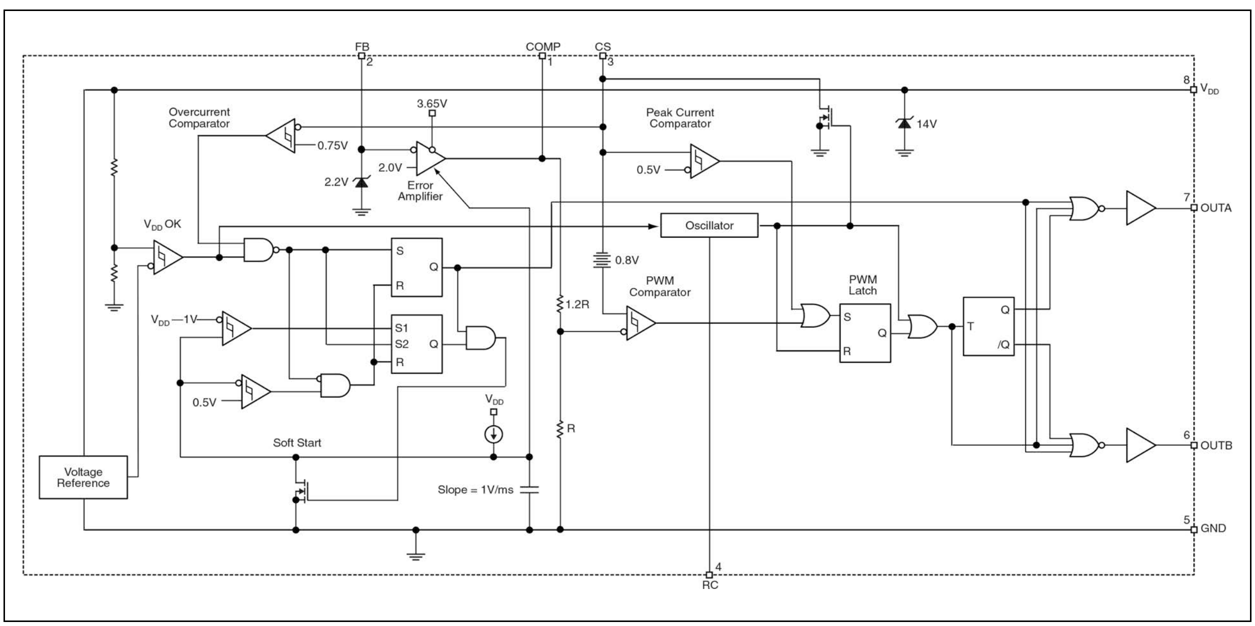
MSOP-8 (MM)



Typical Application Circuits



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (I_{DD} ≤ 10 mA) .... +15V
Supply Current .... 20 mA
OUT A/OUT B Source Current (peak) .... –0.5A
OUT A/OUT B Sink Current (peak) 1.0A
Comp Pin .... VDD
Analog Inputs (FB, CS) .... –0.3V to VDD +0.3V (NOT TO EXCEED 6V)
ESD Rating, Note 1 .... 2 kV

Operating Ratings ‡

V_{DD} Input Voltage (V_{DD}) .... Note 2
Oscillator Frequency (f_{OSC}) .... 10 kHz to 1 MHz

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100 pF.

2: Maximum operating voltage is equal to the V_{DD} [zener] shunt voltage. When operating at or near the shunt voltage, care must be taken to limit the VDD pin current to less than the 20 mA V_{DD} maximum supply current rating.

ELECTRICAL CHARACTERISTICS

$T_A = T_J$ = –40°C to +85°C, V_{DD} = 10V (Note 5), 1 µF capacitor from VDD to GND, R = 22 KΩ, C = 330 pF.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Oscillator Section						
Oscillator Frequency		180	200	220	kHz	—
Oscillator Amplitude/VDD		0.44	0.5	0.56	V/V	Note 1
Error Amp Section						
Input Voltage		1.95	2	2.05	V	COMP = 2V
Input Bias Current		–1	—	1	µA	—
Open Loop Voltage Gain		60	80	—	dB	(Guaranteed by design)
COMP Sink Current		0.3	2.5	—	mA	FB = 2.2V, COMP = 1V
COMP Source Current		–0.15	—0.5	—	mA	FB = 1.3V, COMP = 3V, Note 2
COMP Clamp Voltage		3.1	3.6	4.0	V	VFB = 0V
PWM Section						
Maximum Duty Cycle		48	49	50	%	Measured at OUT A or OUT B
Minimum Duty Cycle		—	—	0	%	COMP = 0V
Current Sense Section						
Gain		1.9	2.2	2.5	V/V	Note 3 (Guaranteed by design)
Maximum Input Signal		0.45	0.5	0.55	V	Note 4
CS to Output Delay		—	70	200	ns	COMP = 3V, CS from 0 to 600 mV
CS Source Current		–200	—	—	nA	—
CS Sink Current		5	10	—	mA	CS = 0.5V, RC = 5.5V, Note 5
Over Current Threshold		0.7	0.75	0.8	V	—
COMP to CS Offset		0.35	0.8	1.2	V	CS = 0V
Output Section						
OUT Low Level		—	0.5	1	V	I = 100 mA
OUT High Level		—	0.5	1	V	I = –50 mA, V_{DD} - OUT
Rise Time		—	25	60	ns	C_L = 1 nF
Fall Time		—	25	60	ns	C_L = 1 nF
Undervoltage Lockout Section						
Start Threshold		11.5	12.5	13.5	V	MIC3808, Note 6
		4.1	4.3	4.5	V	MIC3809
Minimum Operating Voltage After Start		7.6	8.3	9	V	MIC3808
		3.9	4.1	4.3	V	MIC3809
Hysteresis		3.5	4.2	5.1	V	MIC3808
		0.1	0.2	0.3	V	MIC3809
Soft Start Section						
COMP Rise Time		—	2.5	20	ms	FB = 1.8V, Rise from 0.5V to 3V

ELECTRICAL CHARACTERISTICS (CONTINUED)

$T_A = T_J$ = –40°C to +85°C, V_{DD} = 10V (Note 5), 1 µF capacitor from VDD to GND, R = 22 KΩ, C = 330 pF.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Overall Section						
Startup Current		—	130	260	µA	V_{DD} < Start Threshold
Operating Supply Current		—	1	2	mA	FB = 0V, CS = 0V, Note 6 and Note 7
VDD Zener Shunt Voltage		13	14	15	V	I_{DD} = 10 mA, Note 8

Note 1: Measured at RC. Signal amplitude tracks V_{DD}.

2: The COMP pin is internally clamped to 3.65V(typ). The COMP pin source current is tested at V_{COMP} = 3.0V to avoid interfering with this clamp voltage. The minimum source current increases as V_{COMP} approaches V_{CLAMP}.

3: Gain is defined by this formula:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}, 0 \le V_{CS} \le 0.4V$$

4: Parameter measured at trip point of latch with FB at 0V.

5: The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a DC sink path.

6: For MIC3808, set V_{DD} above the start threshold before setting at 10V.

7: Does not include current in the external oscillator network.

8: Start threshold and Zener Shunt threshold track one another.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–55	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10 seconds
Storage Temperature	T_S	–65	—	+150	°C	—
Ambient Temperature	T_A	–40	—	+85	°C	—
Package Thermal Resistance (Note 2)						
Thermal Resistance, SOIC-8	θ_{JA}	—	160	—	°C/W	—
Thermal Resistance, MSOP-8	θ_{JA}	—	206	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum rating. Sustained junction temperatures above that maximum can impact device reliability.

2: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)} – T_A) \div \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. See the “Thermal Considerations” section for details.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

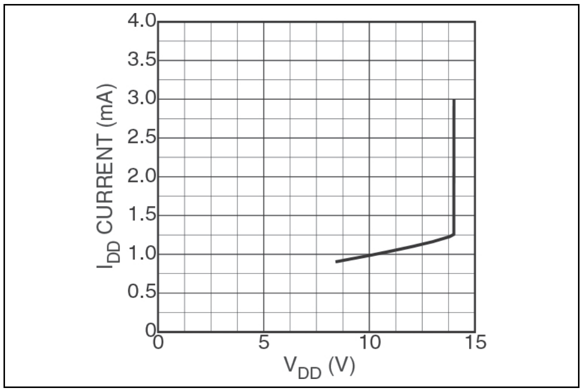


FIGURE 2-1: *MIC3808 V_{DD} vs. I_{DD}.*

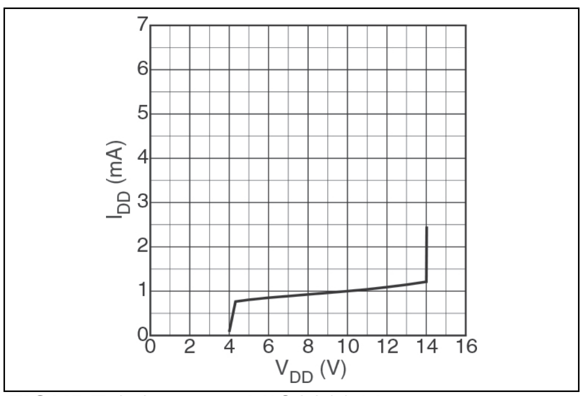


FIGURE 2-2: *MIC3809 V_{DD} vs. I_{DD}.*

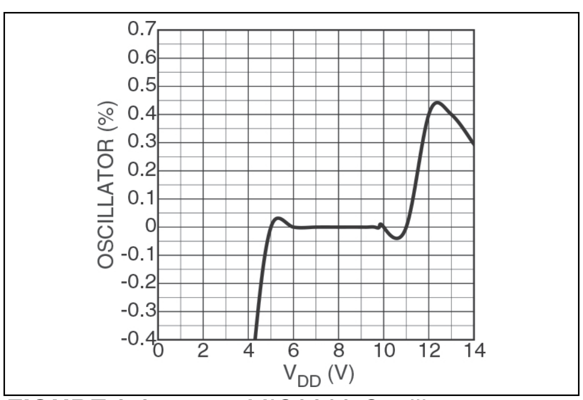


FIGURE 2-3: *MIC3809 Oscillator Variation vs. V_{DD}.*

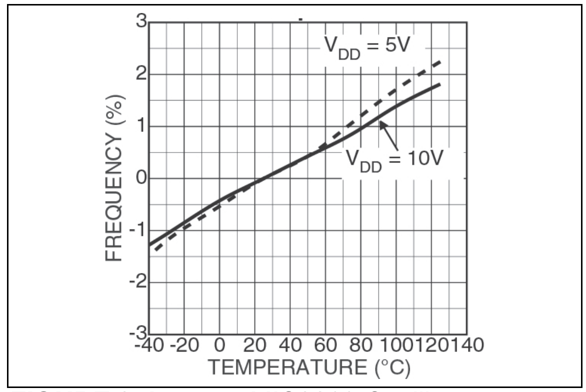


FIGURE 2-4: *MIC3809 Oscillator Frequency Variation vs. Temperature.*

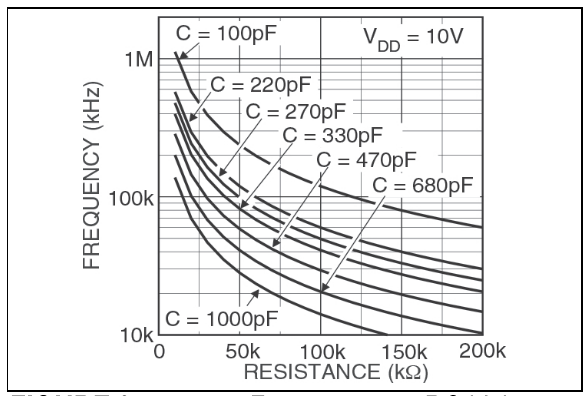


FIGURE 2-5: *Frequency vs. RC Values.*

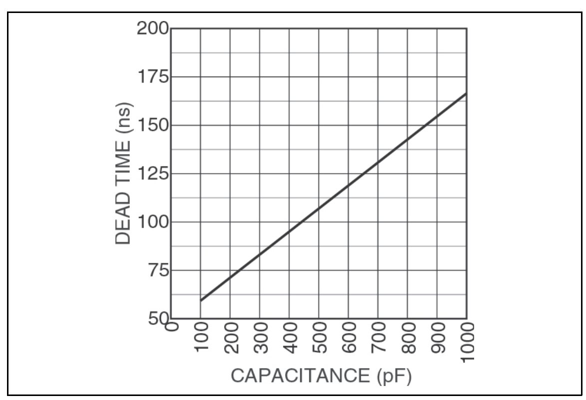


FIGURE 2-6: *RC Pin Capacitance vs. Dead Time.*

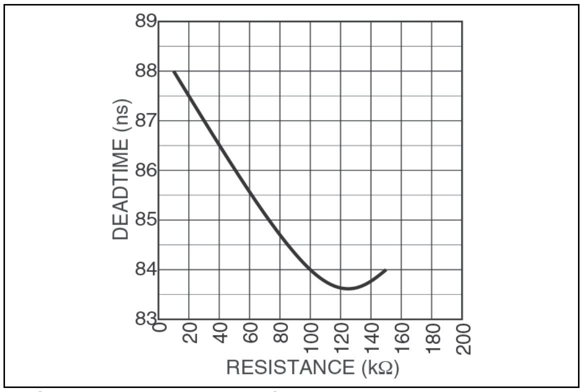


FIGURE 2-7: *RC Pin Resistance vs. Dead Time.*

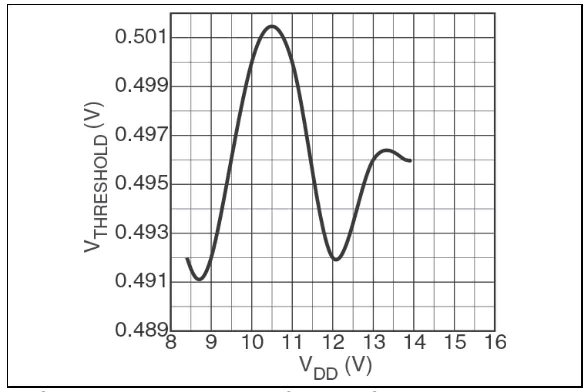


FIGURE 2-10: *MIC3808 Current Limit Threshold vs.* V_{DD}.

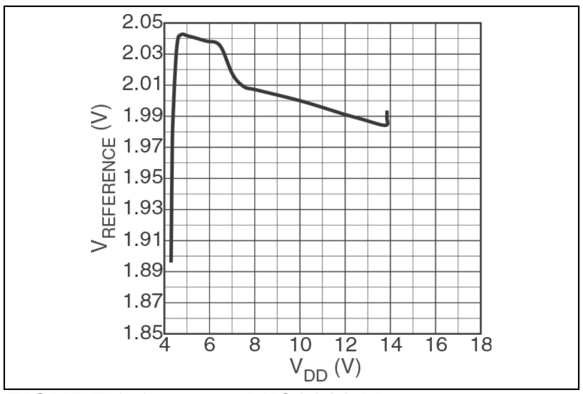


FIGURE 2-8: *MIC3809* $V_{REFERENCE}$ *vs.* V_{DD}.

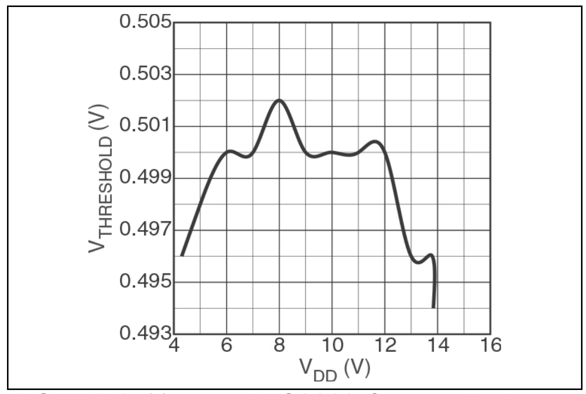


FIGURE 2-11: *MIC3809 Current Limit Threshold vs.* V_{DD}.

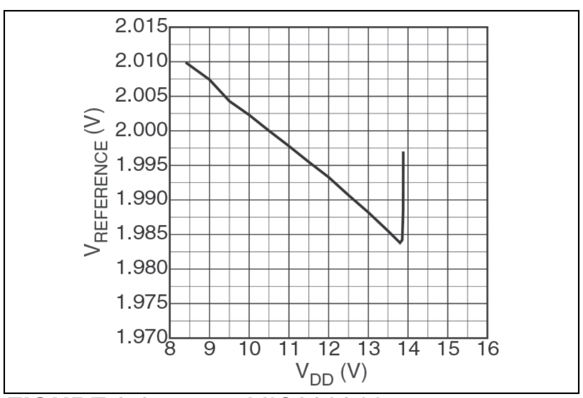


FIGURE 2-9: *MIC3808* $V_{REFERENCE}$ *vs.* V_{DD}.

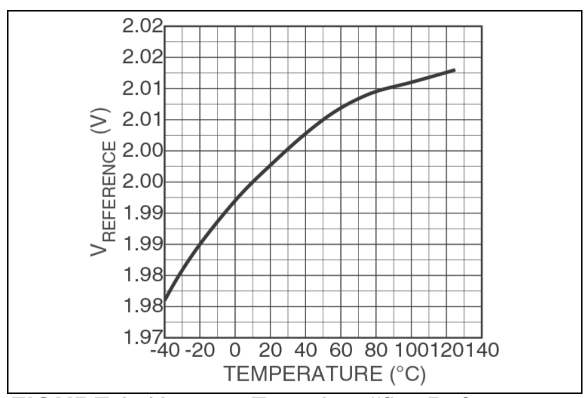


FIGURE 2-12: *Error Amplifier Reference Voltage vs. Temperature.*

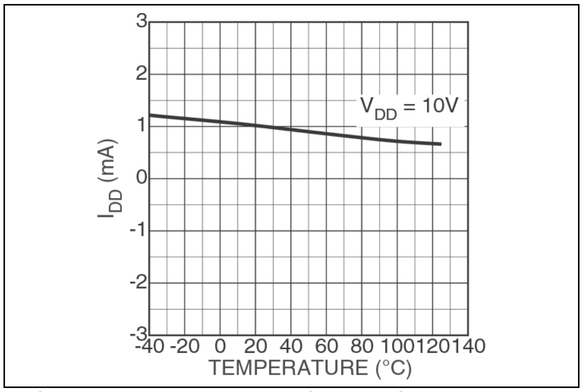


FIGURE 2-13: *V_{DD} Supply Current vs. Temperature.*

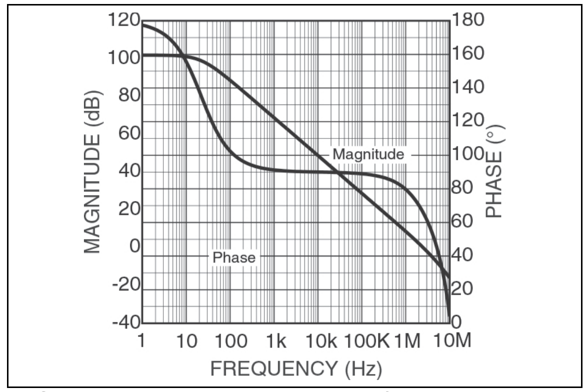


FIGURE 2-14: *Error Amplifier.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	COMP	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the MIC3808 is a true low-output impedance, 4 MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND. The MIC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
2	FB	The inverting input to the error amplifier. For best stability, keep the FB lead length as short as possible and the FB stray capacitance as small as possible.
3	CS	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
4	RC	The oscillator programming pin. The MIC3808's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Only two components are required to program the oscillator, a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula: $$F_{OSCILLATOR} = \frac{1.41}{RC}$$ Where frequency is in Hertz, resistance in Ohms, and capacitance in Farads. The recommended range of timing resistors is between 7 kΩ and 200 kΩ. The recommended range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 7 kΩ should be avoided. For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.
5	GND	Ground.
6	OUT B	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500 mA peak source current, and 1A peak sink current. The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This "dead time" between the two outputs, along with a slower output rise time than fall time, ensures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.
7	OUT A	
8	VDD	The power input connection for this device. Although quiescent V_{DD} current is very low, the total supply current will be higher, depending on OUT B and OUT A current, as well as the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from I_{OUT} = Qg × F, where F is frequency. To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible. A 1 µF decoupling capacitor is recommended.

4.0 APPLICATION INFORMATION

The MIC3808/9 is a high-speed power supply controller with push-pull output drive capability. MIC3808 has a higher V_{DD} turn-on threshold and more hysteresis between V_{DD} turn-on and turn-off than the MIC3809. The outputs of the controller operate in a push-pull fashion with a guaranteed dead time between them. A block diagram of the MIC3808/9 controller is shown in Figure 1.

4.1 VDD and Turn-on Sequence

The oscillator and output gate drive signals are disabled when V_{DD} is lower than the turn on threshold. Circuitry in the output drivers eliminates glitching or random pulsing during the start-up sequence. The oscillator is enabled when V_{DD} is applied and reaches the turn-on threshold. The V_{DD} comparator also turns off the internal soft-start discharge FET, slowly bringing up the COMP pin voltage.

The VDD pin is internally clamped. As V_{DD} approaches this clamp voltage, the V_{DD} current will increase over the normal current draw of the IC. Exceeding the V_{DD} zener shunt voltage may cause excessive power dissipation in the MIC3808/9.

4.2 Soft-Start

The soft start feature helps reduce surge currents at the power supply input source. An internal current source and capacitor ramp up from 0V to near V_{DD} at a typical rate of 1 V/ms. The soft start feature limits the output voltage of the error amplifier at the COMP pin. As the soft start voltage rises, it allows the COMP pin voltage to rise, which in turn allows the duty cycle of the output drivers to increase. The internal soft start voltage is discharged and remains discharged during the following conditions:

1. The V_{DD} voltage drops below the turn-off threshold
2. The voltage on the CS pin exceeds the overcurrent comparator threshold

Once the internal soft start discharge FET is turned on, it cannot be turned off until the internal soft start voltage drops down below 0.5V. This insures a clean restart.

4.3 Oscillator

The oscillator operates at twice the switching frequency of either OUT A or OUT B. The oscillator generates a sawtooth waveform on the RC pin. The rising edge of the waveform is controlled by the external resistor/capacitor combination.

The fall time is set by the on-resistance of the discharge FET (see Figure 2). The fall time sets the delay (dead time) between the turn-off of one output driver and the turn-on of the other driver. A toggle flip-flop insures that drive signals to OUT A and OUT B are alternated and therefore insures a maximum duty cycle of less than 50% for each output driver.

Graphs of component values vs. oscillator frequency and dead time are shown in the typical characteristic section of this specification.

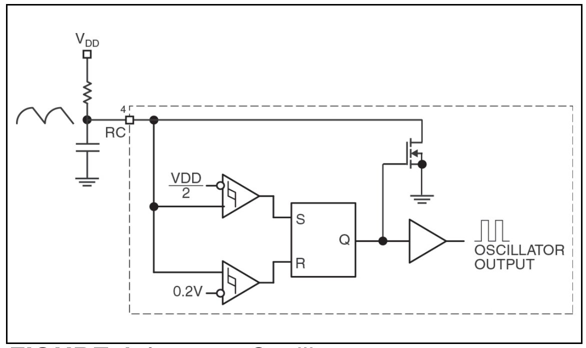


FIGURE 4-1: *Oscillator.*

The voltage source to the resistor/capacitor timing components is V_{DD}. The internal turn-off comparator threshold in the oscillator circuit is $V_{DD}/2$. This allows the oscillator to track changes in V_{DD} and minimize frequency variations in the oscillator. The oscillator frequency can be roughly approximated using the following formula:

EQUATION 4-1:

$$F_{OSCILLATOR} = \frac{1.41}{RC}$$

Where:

Frequency is in Hz

Resistance is in Ohms

Capacitance is in Farads.

Graphs of oscillator frequency and dead time vs component values are shown in the Typical Characteristic section of this specification. The recommended range of timing resistors and capacitors is 10 kΩ to 200 kΩ and 100 pF to 1000 pF. To minimize oscillator noise and insure a stable waveform the following layout rules should be followed:

1. The higher impedance of capacitor values less than 100 pF may causes the oscillator circuit to become more susceptible to noise. Parasitic pin and etch trace capacitances become a larger part of the total RC capacitance and may influence the desired switching frequency.

2. The circuit board etch between the timing resistor, capacitor, RC pin and ground must be kept as short as possible to minimize noise pickup and insure a stable oscillator waveform.
3. The ground lead of the capacitor must be routed close to the ground lead of the MIC3808/9.

4.4 Current Sensing and Overcurrent Protection

The CS pin features are:

1. Peak current limit
2. Overcurrent limit
3. Internal current sense discharge
4. Front edge blanking

In current mode control, a PWM comparator uses the inductor current signal and the error amplifier signal to determine the operating duty cycle. In the MIC3808/9 the signal at the CS pin is level shifted up before it reaches the PWM comparator as shown in Figure 1. This allows operation of the error amplifier and PWM comparator in a linear region.

There are two current limit thresholds in the MIC3808/9; peak current limit and overcurrent limit. The normal operating voltage at the CS pin is designed less than these thresholds.

A pulse-by-pulse current limit occurs when the inductor current signal at the CS pin exceeds the peak current limit threshold. The on-time is terminated for the remainder of the switching cycle, regardless of whether OUT A or OUT B is active.

If the signal at the CS pin goes past the peak threshold and exceeds the overcurrent limit threshold, the overcurrent limit comparator forces the soft start node to discharge and initiates a soft start reset.

An internal FET discharges the CS pin at the end of the oscillator charge time. The FET turns on when the voltage on the RC pin reaches the upper threshold (V_{DD}/2) and remains on for the duration of the RC pin discharge time and for typically 100 ns after the start of the next on-time period. The 100 ns period at the beginning of the on-time implements a front edge blanking feature that prevents false triggering of the PWM comparator due to noise spikes on the leading edge of the current turn-on signal. The front edge blanking also sets the minimum on-time for OUT A and OUT B. The timing diagram for the CS pin is shown in Figure 3.

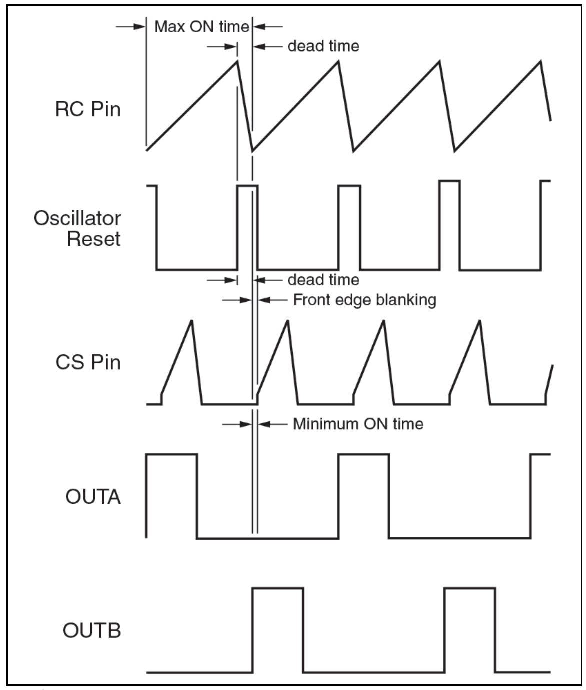


FIGURE 4-2: *Timing Diagram.*

4.5 Error Amplifier

The error amplifier is part of the voltage control loop of the power supply. The FB pin is the inverting input to the error amplifier. The non-inverting input is internally connected to a reference voltage. The output of the error amplifier, COMP, is connected to the PWM comparator. A voltage divider between the error amplifier output (COMP pin) and the PWM comparator allows the error amplifier to operate in a linear region for better transient response. The output of the error amplifier (COMP pin) is limited to typically 3.65V to prevent the COMP pin from rising up too high during startup or during a transient condition. This feature improves the transient response of the power supply.

4.6 Output Drivers

OUT A and OUT B are alternating output stages, which switch at half the oscillator frequency. A toggle flip-flop in the MIC3808/9 guarantee both outputs will not be on at the same time. The RC discharge time is the dead time, where both outputs are off. This provides an adjustable non-overlap time to prevent shoot through currents and transformer saturation in the power supply.

The output drivers are inhibited when V_{DD} is below the undervoltage threshold. Internal circuitry prevents the output drivers from glitching high when V_{DD} is first applied to the MIC3808/9 controller.

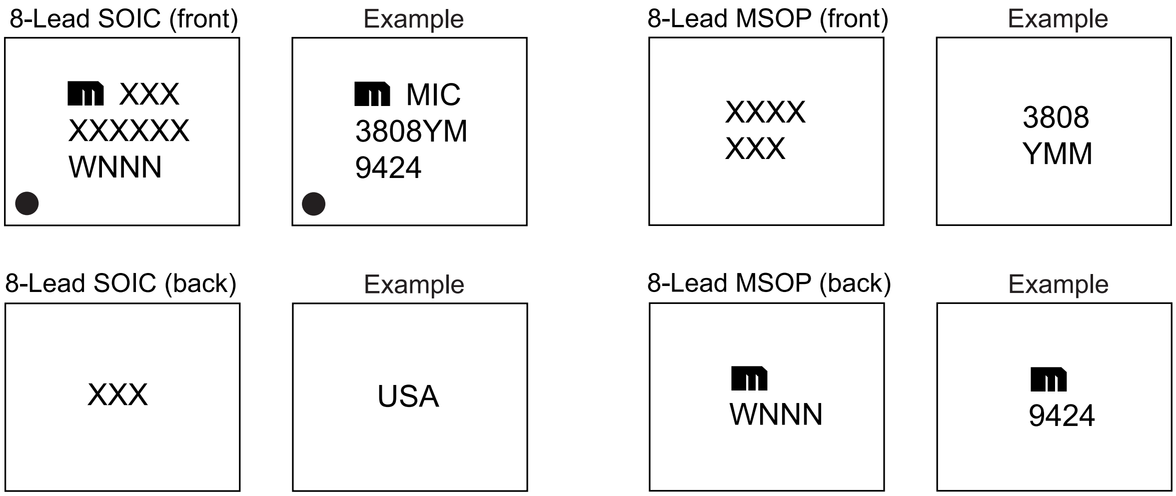
4.7 Decoupling and PCB Layout

PCB layout is critical to achieve reliable, stable and efficient operation. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to insure proper operation of the circuit:

- Low level signal and power grounds should be kept separate and connected at only one location, preferably the ground pin of the control IC. The ground signals for the current sense, voltage feedback and oscillator should be grouped together. The return signals for the gate drives should be grouped together and a common connection made at the ground pin of the controller. The low level signals and their returns must be kept separate from the high current and high voltage power section of the power supply.
- Avoid running sensitive traces, such as the current sense and voltage feedback signals next to or under power components, such as the switching FETs and transformer.
- If a current sense resistor is used, it’s ground end must be located very close to the ground pin of the MIC3808/9 controller. Careful PCB layout is necessary to keep the high current levels in the current sense resistor from running over the low level signals in the controller.
- A minimum 1 µf bypass capacitor must be connected directly between the VDD and GND pins of the MIC3808/9. An additional 0.1uf capacitor between the V_{DD} end oscillator frequency setting resistor and the ground end of the oscillator capacitor may be necessary if the resistor is a distance away from the main 1 µF bypass capacitor.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

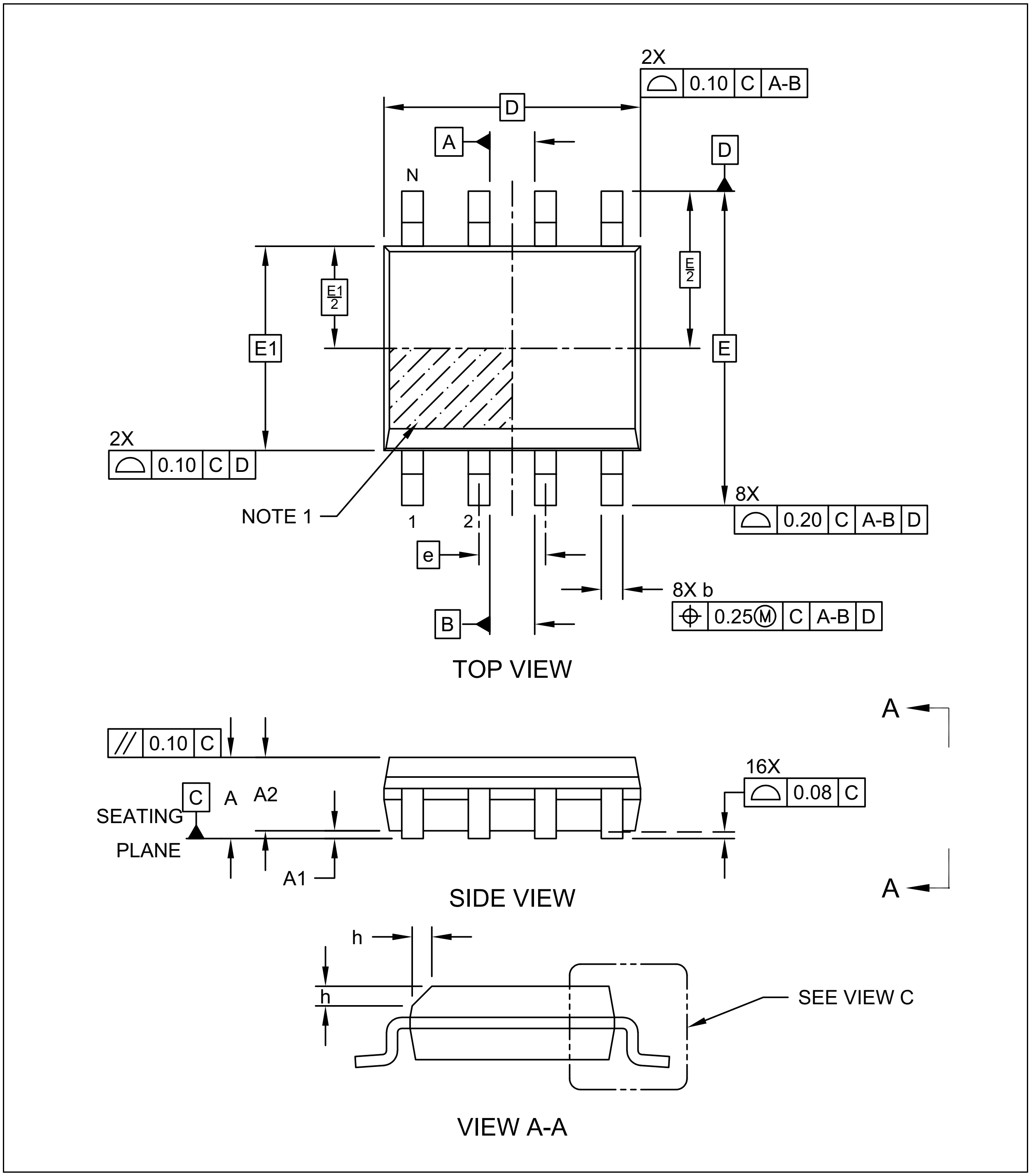
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N.

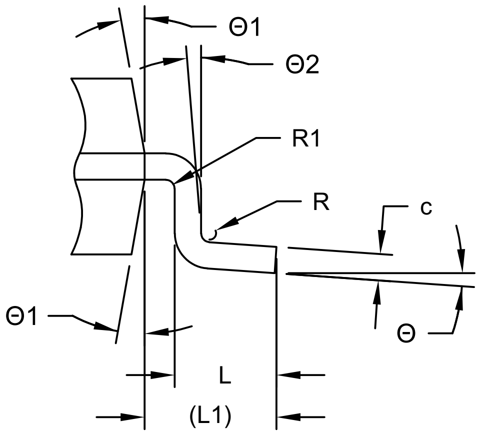
8-Lead 3.90 mm SOIC Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

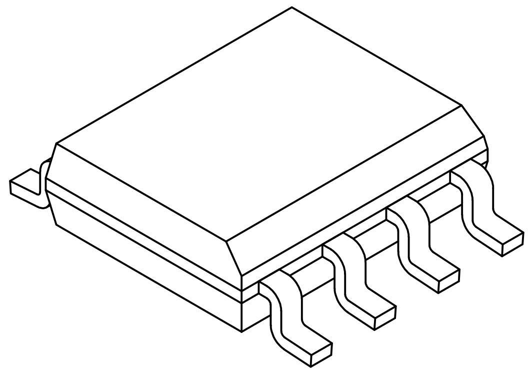


8-Lead 3.90 mm SOIC Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



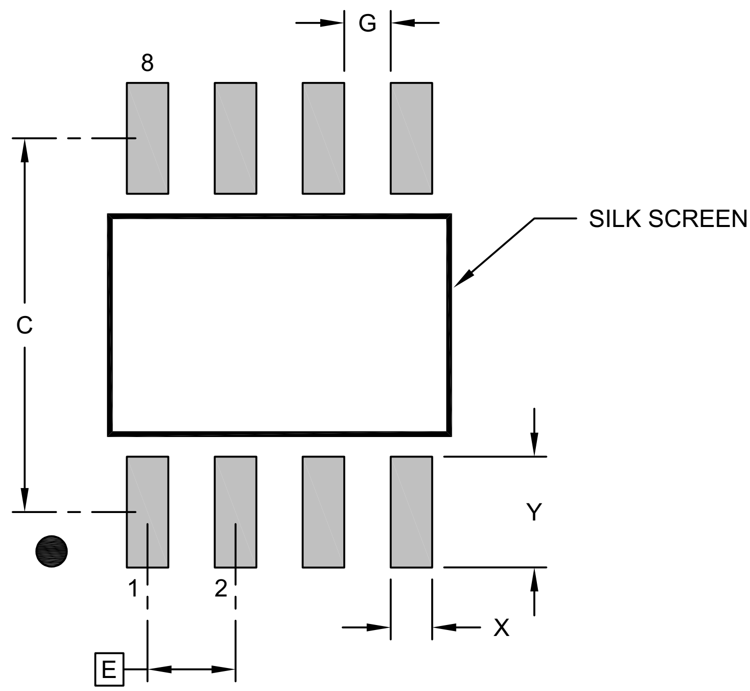
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.35	-	1.75
Standoff	A1	0.10	-	0.25
Molded Package Height	A2	1.25	-	1.65
Overall Length	D	4.90 BSC		
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Index Chamfer	h	0.25	-	0.50
Terminal Width	b	0.31	0.41	0.51
Terminal Thickness	c	0.17	-	0.25
Terminal Length	L	0.40	-	1.00
Footprint	L1	1.04 REF		
Terminal Bend Radius	R	0.07	-	-
Terminal Bend Radius	R1	0.07	-	-
Lead Angle	Θ	0°	-	8°
Mold Draft Angle	Θ1	5°	-	15°
Lead Angle	Θ2	0°	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

8-Lead 3.90 mm SOIC Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (Xnn)	X			0.60
Contact Pad Length (Xnn)	Y			1.60
Contact Pad to Contact Pad (Xnn)	G	0.67		

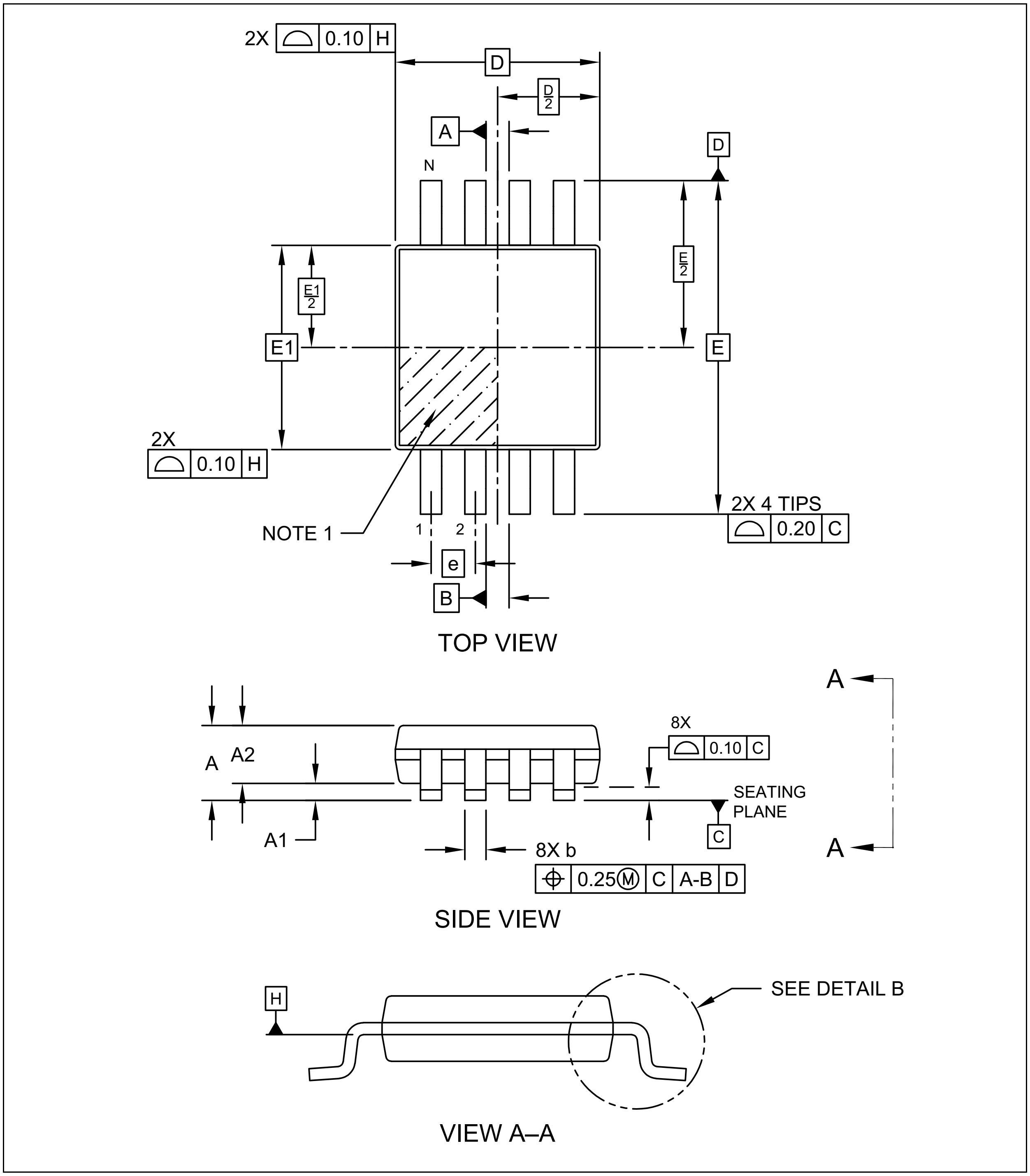
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

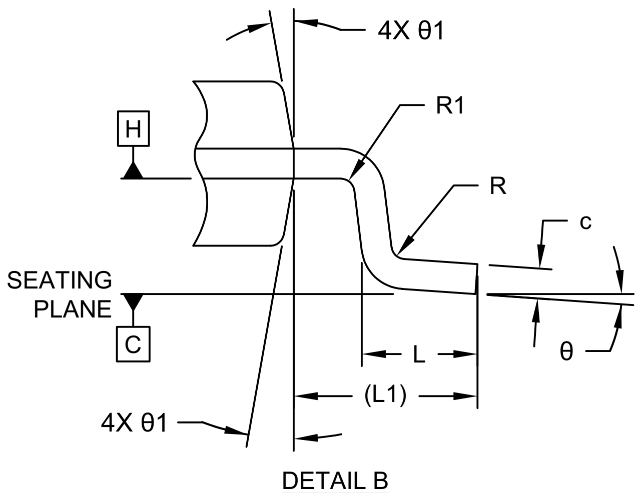
8-Lead 3 mm x 3 mm MSOP Package Outline and Recommended Land Pattern

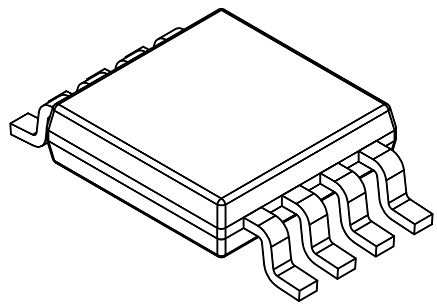
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



8-Lead 3 mm x 3 mm MSOP Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





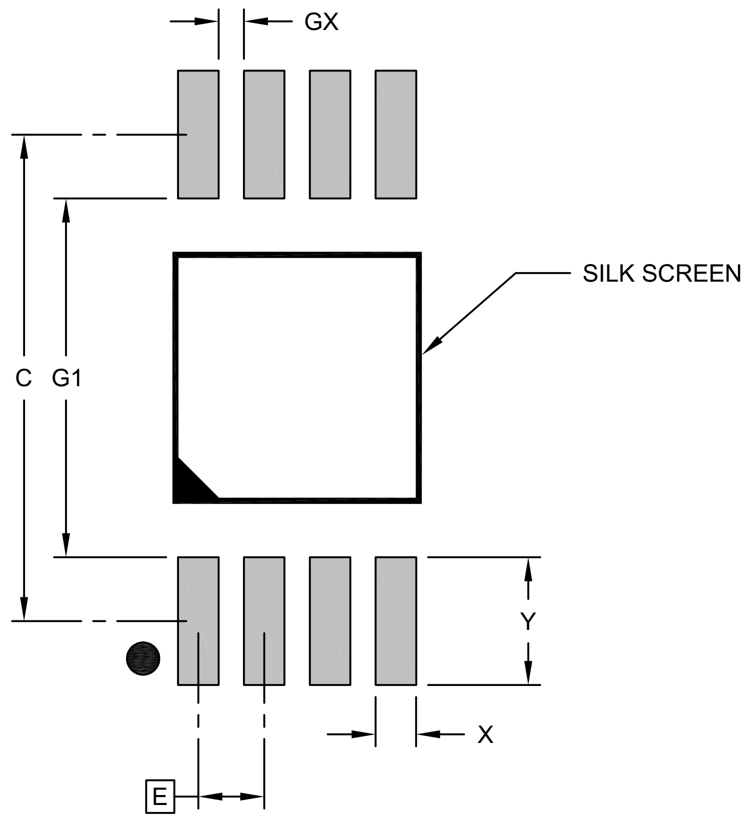
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.94	1.02	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.25	0.30	0.40
Terminal Thickness	c	0.13	0.15	0.23
Terminal Length	L	0.45	0.55	0.70
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

8-Lead 3 mm x 3 mm MSOP Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.80	
Contact Pad Width (X8)	X			0.40
Contact Pad Length (X8)	Y			1.26
Contact Pad to Contact Pad (X4)	G1	3.54		
Contact Pad to Contact Pad (X6)	GX	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Micrel document MIC3808/9 to Microchip data sheet DS20006724A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	XX	-XX
Device	Junction Temp. Range	Package	Media Type

Device:	MIC3808: MIC3809:	Push-Pull PWM Controller Push-Pull PWM Controller
Temperature Range:	Y =	–40°C to +85°C
Package:	M = MM =	8-Lead 3.90 mm SOIC 8-lead 3x3 mm MSOP
Media Type:	<blank> = -TR =	95/Tube 2500/Reel

Examples:

a) MIC3808YM: MIC3808, –55°C to +150°C Temp. Range, SOIC, 95/Tube

b) MIC3809YM-TR: MIC3809, –55°C to +150°C Temp. Range, SOIC, 2500/Reel

c) MIC3809YMM: MIC3809, –55°C to +150°C Temp. Range, MSOP, 95/Tube

d) MIC3808YMM-TR: MIC3808, –55°C to +150°C Temp. Range, MSOP, 2500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

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