5833

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

Designed to reduce logic supply current, chip size, and system cost, the UCN5833A/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits.

These 32-bit drivers have bipolar open-collector npn Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN5833A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. At an ambient temperature of +75°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. For high-density applications, the UCN5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050" (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FEATURES

■ To 3.3 MHz Data Input Rate

■ 30 V Minimum Output Breakdown

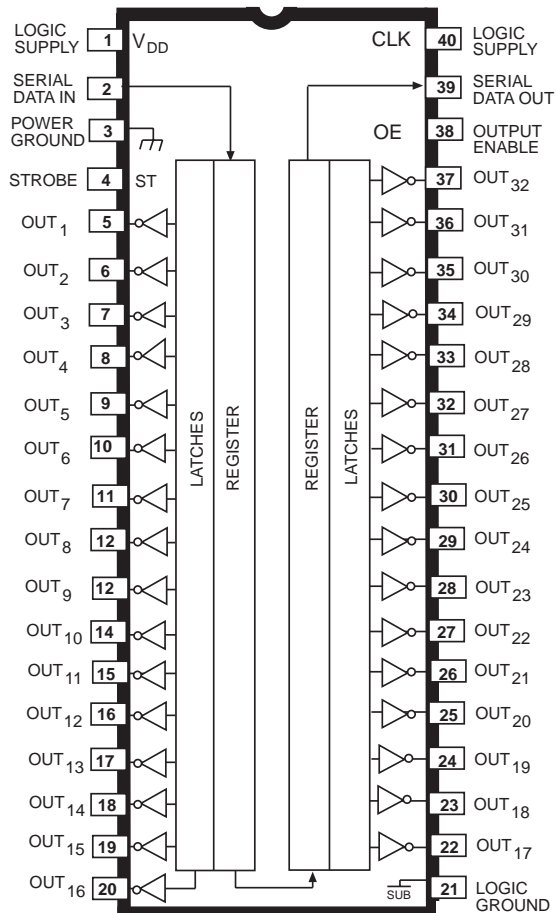■ Darlington Current-Sink Outputs

■ Low-Power CMOS Logic and Latches

UCN5833EP

Dwg. No. A-13,049

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . **30 V**

Logic Supply Voltage, V_{DD} . . . . **7.0 V**

Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
I_{OUT} (each output) . . . . **125 mA**

Package Power Dissipation, P_D
(UCN5833A) . . . . **3.5 W***
(UCN5833EP) . . . . **2.5 W***

Operating Temperature Range,
T_A . . . . **-20°C to +85°C**

Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number:

Part Number	Package
UCN5833A	40-Pin DIP
UCN5833EP	44-Lead PLCC

Allegro MicroSystems, Inc.

5833
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5833A

Pin	Signal
LOGIC SUPPLY	1 V_{DD}
SERIAL DATA IN	2
POWER GROUND	3
STROBE	4 ST
OUT$_1$	5
OUT$_2$	6
OUT$_3$	7
OUT$_4$	8
OUT$_5$	9
OUT$_6$	10
OUT$_7$	11
OUT$_8$	12
OUT$_9$	12
OUT$_{10}$	14
OUT$_{11}$	15
OUT$_{12}$	16
OUT$_{13}$	17
OUT$_{14}$	18
OUT$_{15}$	19
OUT$_{16}$	20

LATCHES REGISTER REGISTER LATCHES

Pin	Signal
CLK	40 LOGIC SUPPLY
OE	39 SERIAL DATA OUT
	38 OUTPUT ENABLE
37	OUT$_{32}$
36	OUT$_{31}$
35	OUT$_{30}$
34	OUT$_{29}$
33	OUT$_{28}$
32	OUT$_{27}$
31	OUT$_{26}$
30	OUT$_{25}$
29	OUT$_{24}$
28	OUT$_{23}$
27	OUT$_{22}$
26	OUT$_{21}$
25	OUT$_{20}$
24	OUT$_{19}$
23	OUT$_{18}$
22	OUT$_{17}$
21	LOGIC GROUND ($\overline{SUB}$)

Dwg. No. A-13,048

FUNCTIONAL BLOCK DIAGRAM

CLOCK
SERIAL DATA IN
STROBE
OUTPUT ENABLE

32-BIT SHIFT REGISTER

LATCHES

OUT$_1$ OUT$_2$ OUT$_3$ POWER GROUND OUT$_{30}$ OUT$_{31}$ OUT$_{32}$

V_{DD}

SERIAL DATA OUT

LOGIC GROUND
SUB

MOS
BIPOLAR
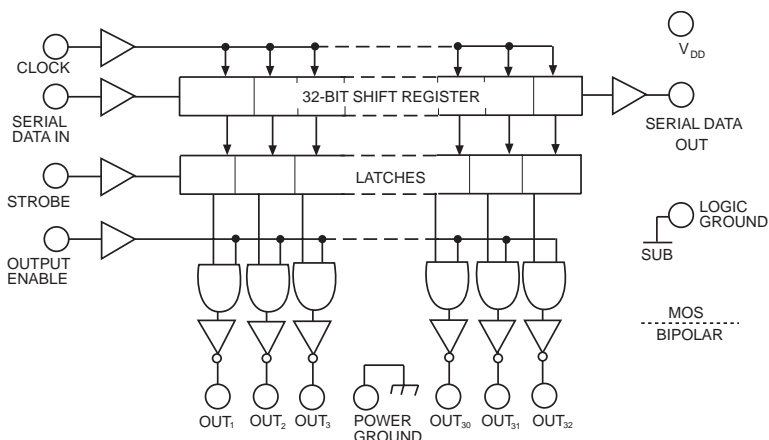
Dwg. No. A-13,057

TYPICAL INPUT CIRCUIT

V_{DD}
IN
SUB
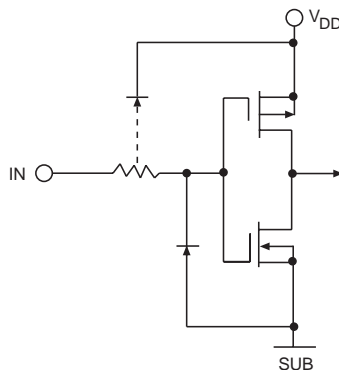
Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER
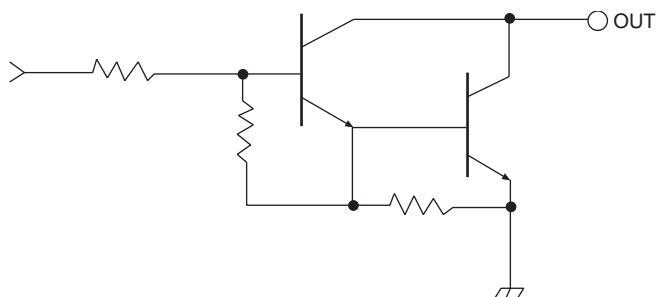
OUT

Dwg. No. A-13,051

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V, T_A = 70°C	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	1.2	V
		I_{OUT} = 100 mA	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0 V	—	-1.0	μA
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 μA	4.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 μA	—	0.3	V
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	1.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	500	ns
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	500	ns

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Output Enable Input	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	⌐	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⌐	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	⌐┐	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State
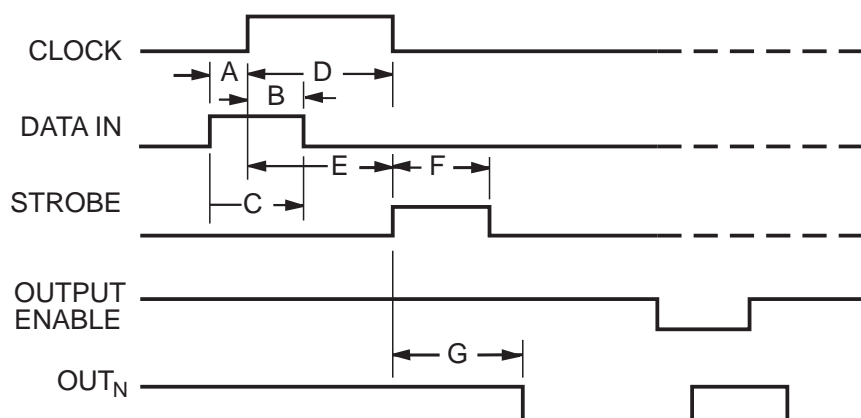
Dwg. No. A-12,276A

TIMING CONDITIONS
(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse
   (Data Set-Up Time) ....**75 ns**

B. Minimum Data Active Time After Clock Pulse
   (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and
   Output Transition .... **500 ns**

   Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.
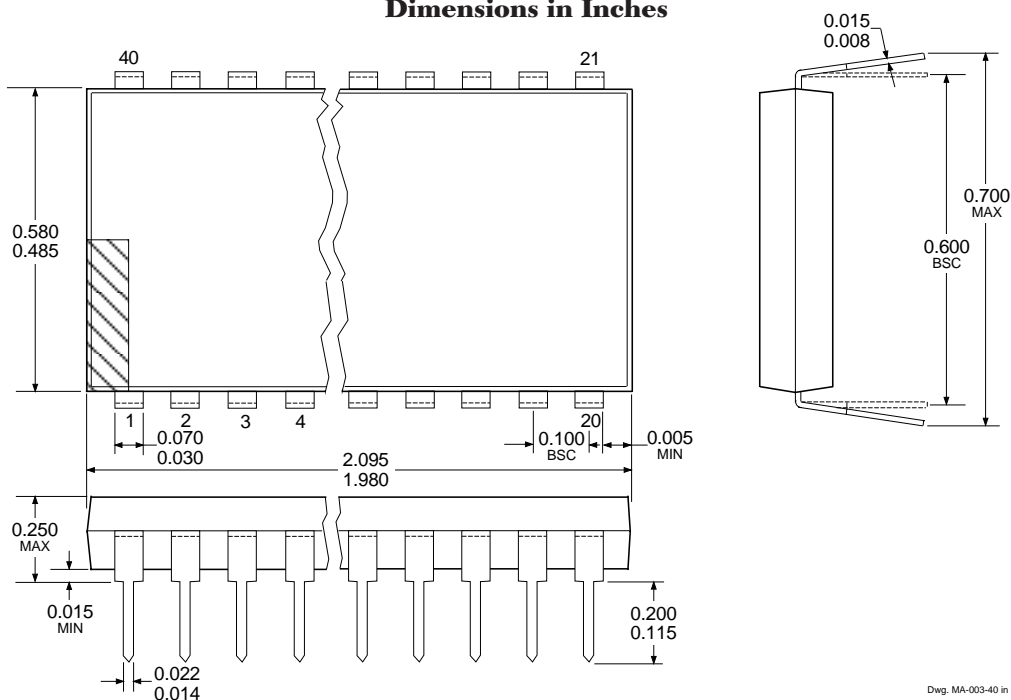
   Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

   When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

UCN5833A

Dimensions in Inches

40   21

0.015
0.008

0.700
MAX

0.600
BSC

0.580
0.485

1   2   3   4   20

0.070
0.030

2.095
1.980

0.100
BSC

0.005
MIN

0.250
MAX

0.015
MIN

0.200
0.115

0.022
0.014

Dwg. MA-003-40 in

Dimensions in Millimeters
(Based on 1" = 2.54 mm)

40   21

0.381
0.204

17.78
MAX

15.24
BSC

14.73
12.32

1   2   3   4   20

1.77
0.77

53.2
50.3

2.54
BSC

0.13
MIN

6.35
MAX

0.39
MIN

5.08
2.93

0.558
0.356
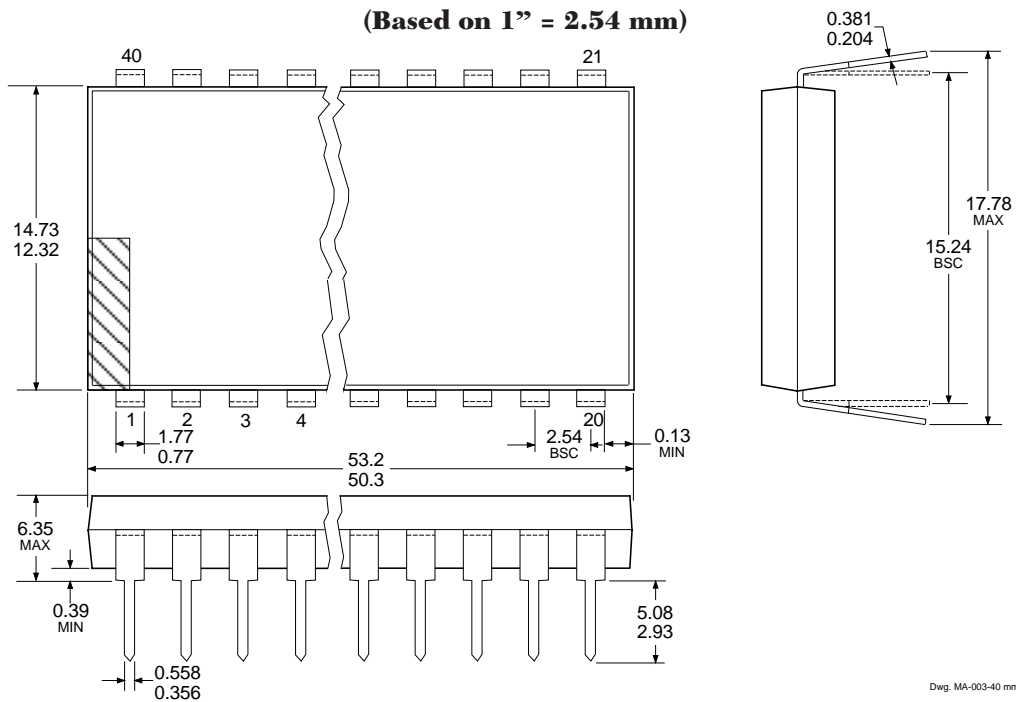
Dwg. MA-003-40 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
        2. Lead spacing tolerance is non-cumulative.
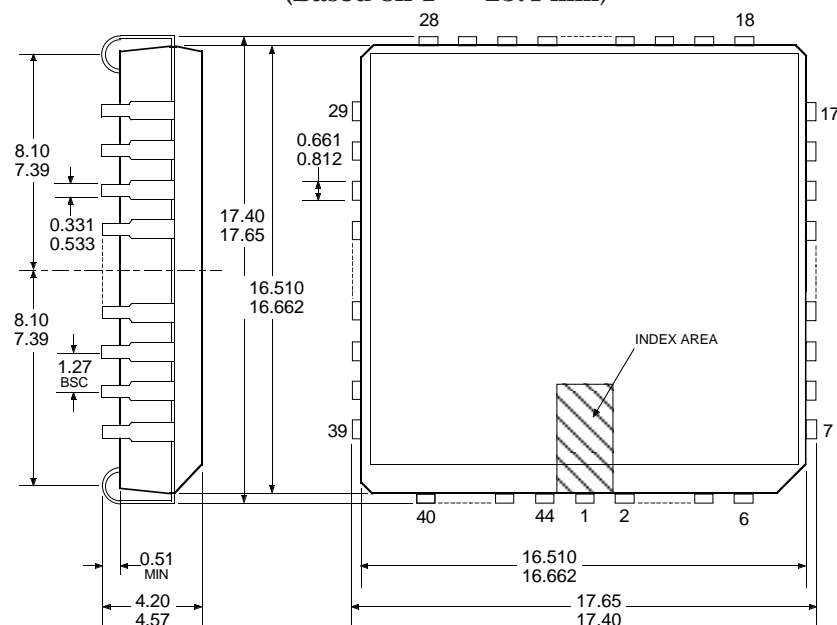   3. Lead thickness is measured at seating plane or below.

UCN5833EP
Dimensions in Inches
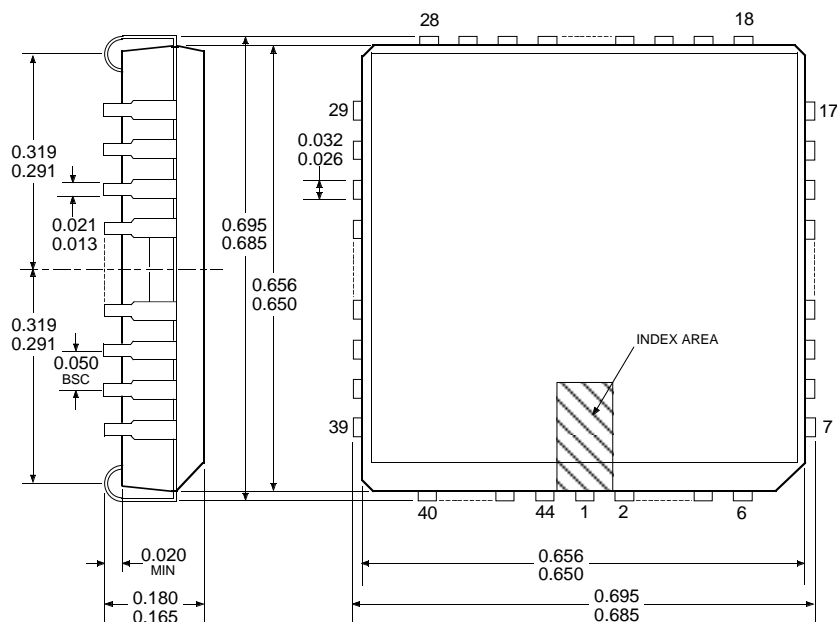
Dwg. MA-005-44A in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)

Dwg. MA-005-44A mm

NOTES: 1. Exact body and lead configuration at
           vendor's option within limits shown.
        2. Lead spacing tolerance is non-cumulative.

Allegro™
MicroSystems, Inc.

115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

BiMOS II (Series 5800) & DABiC IV (Series 6800)
INTELLIGENT POWER INTERFACE DRIVERS
SELECTION GUIDE

Function	Output Ratings *		Part Number †
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F
12-Bit (active pull-downs)	-25 mA	60 V	5811
20-Bit (active pull-downs)	-25 mA	60 V	5812-F
32-Bit (active pull-downs)	-25 mA	60 V	5818-F
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
SPECIAL-PURPOSE FUNCTIONS			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

*   Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits.
    Negative current is defined as coming out of (sourcing) the output.

†   Complete part number includes additional characters to indicate operating temperature range and package style.

‡   Internal transient-suppression diodes included for inductive-load protection.