

1.5A Dual High-Speed Power MOSFET Drivers

Features

- High-Speed Switching (C_L = 1000 pF): 30 nsec
- · High Peak Output Current: 1.5A
- · High Output Voltage Swing:
 - V_{DD} -25 mV
 - GND +25 mV
- Low Input Current (Logic '0' or '1'): 1 μA
- · TTL/CMOS Input Compatible
- Available in Inverting and Noninverting Configurations
- · Wide Operating Supply Voltage:
 - 4.5V to 18V
- · Current Consumption:
 - Inputs Low 0.4 mA
 - Inputs High 8 mA
- Single Supply Operation
- Low Output Impedance: 6Ω
- Latch-Up Resistant: Withstands > 500 mA Reverse Current
- ESD Protected: 2 kV

Applications

- · Switch Mode Power Supplies
- · Pulse Transformer Drive
- Clock Line Driver
- Coax Cable Driver

General Description

The TC426/TC427/TC428 are dual CMOS high-speed drivers. A TTL/CMOS input voltage level is translated into a rail-to-rail output voltage level swing. The CMOS output is within 25 mV of ground or positive supply.

The low-impedance, high-current driver outputs swing a 1000 pF load to 18V in 30 nsec. The unique current and voltage drive qualities make the TC426/TC427/TC428 ideal power MOSFET drivers, line drivers, and DC-to-DC converter building blocks.

Input logic signals may equal the power supply voltage. Input current is a low 1 μ A, making direct interface to CMOS/bipolar switch-mode power supply control ICs possible, as well as open-collector analog comparators.

Quiescent power supply current is 8 mA maximum, which is important in DC-to-DC converter applications with power efficiency constraints and high-frequency switch-mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pF load to 18V at 100 kHz.

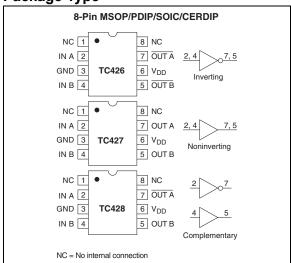
TC426 is inverting driver.

TC427 is noninverting driver.

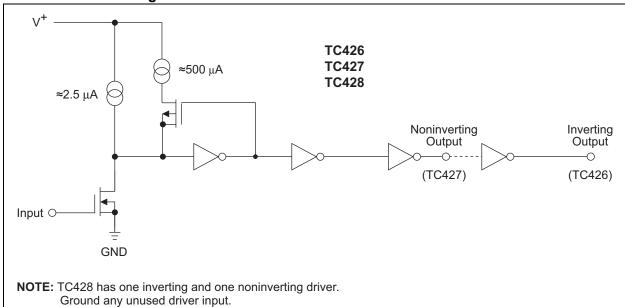
TC428 contains an inverting and noninverting driver.

Other pin-compatible driver families are the TC1426/TC1427/TC1428, TC4426/TC4427/TC4428 and TC4426A/TC4427A/TC4428A.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage	+20V
Input Voltage, Any Terminal	V _{DD} + 0.3V to GND – 0.3V
Power Dissipation (T _A ≤ 70°C)	
PDIP	730 mW
CERDIP	
SOIC	
MSOP	340 mW
Derating Factor	
PDIP	8 mW/°C
CERDIP	
SOIC	4 mW/°C
MSOP	4.8 mW/°C
Operating Temperature Range	
C Version	0°C to +70°C
I Version	25°C to +85°C
E Version	40°C to +85°C
M Version	55°C to +125°C
Storage Temperature Range	65°C to +150°C

[†] Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T _A = +25°C with 4.5V ≤ V _{DD} ≤ 18V, unless otherwise noted.									
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions			
Input									
V _{IH}	Logic 1, High Input Voltage	2.4	_	_	V				
V _{IL}	Logic 0, Low Input Voltage	_	_	0.8	V				
I _{IN}	Input Current	-1	_	1	μΑ	$0V \le V_{IN} \le V_{DD}$			
Output									
V _{OH}	High Output Voltage	V _{DD} – 0.025	_	_	V	I _{OUT} = 0 mA			
V _{OL}	Low Output Voltage	_	_	0.025	V	I _{OUT} = 0 mA			
R _{OH}	High Output Resistance	_	10	15	Ω	I _{OUT} = 10 mA, V _{DD} = 18V			
R _{OL}	Low Output Resistance	_	6	10	Ω	I _{OUT} = 10 mA, V _{DD} = 18V			
I _{PK}	Peak Output Current	_	1.5	_	Α	Note 1			
Switching	Time (Note 1)								
t _R	Rise Time	_	_	30	nsec	Figure 3-1, Figure 3-2			
t _F	Fall Time	_	_	30	nsec	Figure 3-1, Figure 3-2			
t _{D1}	Delay Time	_	_	50	nsec	Figure 3-1, Figure 3-2			
t _{D2}	Delay Time			75	nsec	Figure 3-1, Figure 3-2			
Power Sup	ply								
I _S	Power Supply Current	_	_	8	mA	V _{IN} = 3V (Both Inputs)			
		_	_	0.4		V _{IN} = 0V (Both Inputs)			

Note 1: Ensured by design. Not production tested.

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range (-55°C to +125°C) with 4.5V \leq V _{DD} \leq 18V, unless otherwise noted.									
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions			
Input									
V _{IH}	Logic 1, High Input Voltage	2.4	_	_	V				
V_{IL}	Logic 0, Low Input Voltage	_	_	0.8	V				
I _{IN}	Input Current	-10	_	10	μА	$0V \le V_{IN} \le V_{DD}$			
Output									
V _{OH}	High Output Voltage	V _{DD} – 0.025	_	_	V	I _{OUT} = 0 mA			
V _{OL}	Low Output Voltage	_	_	0.025	V	I _{OUT} = 0 mA			
R _{OH}	High Output Resistance	_	13	20	Ω	I _{OUT} = 10 mA, V _{DD} = 18V			
R _{OL}	Low Output Resistance	_	8	15	Ω	I _{OUT} = 10 mA, V _{DD} = 18V			
Switching	Time (Note 1)								
t _R	Rise Time	_	_	60	nsec	Figure 3-1, Figure 3-2			
t _F	Fall Time	_	_	60	nsec	Figure 3-1, Figure 3-2			
t _{D1}	Delay Time	_	_	75	nsec	Figure 3-1, Figure 3-2			
t _{D2}	Delay Time	_	_	120	nsec	Figure 3-1, Figure 3-2			
Power Sup	Power Supply								
I _S	Power Supply Current		_	12 0.6	mA	V _{IN} = 3V (Both Inputs) V _{IN} = 0V (Both Inputs)			

Note 1: Ensured by design. Not production tested.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin MSOP, PDIP, SOIC, CERDIP)	Symbol	Description
TC426/TC427/TC428	3	
1	NC	No internal connection.
2	IN A	Control input A, TTL/CMOS compatible logic input.
3	GND	Ground.
4	IN B	Control input B, TTL/CMOS compatible logic input.
5	OUT B/OUT B/OUT B	CMOS totem-pole output.
6	V_{DD}	Supply input, 4.5V to 18V.
7	OUT A/OUT A/OUT A	CMOS totem-pole output.
8	NC	No internal connection.

3.0 APPLICATIONS INFORMATION

3.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 1000 pF load to 18V in 25 nsec requires an 0.72A current from the device power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (< 0.5 in.) should be used. A 1 μF film capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

3.2 Grounding

The TC426 and TC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits, or a ground plane, should be used.

3.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. At T_A = +25°C with a logic '1' input, the maximum quiescent supply current is 8 mA. Logic '0' input level signals reduce quiescent current to 0.4 mA maximum. Minimum power dissipation occurs for logic '0' inputs for the TC426/TC427/TC428. **Unused driver inputs must be connected to VDD or GND**.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making the device TTL compatible over the 4.5V to 18V supply operating range. Input current is less than 1 μA over this range.

The TC426/TC427/TC428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560, and similar switch-mode power supply integrated circuits.

3.4 Power Dissipation

The supply current vs. frequency and supply current vs. capacitive load characteristic curves will aid in determining power dissipation calculations.

The TC426/TC427/TC428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- · Output stage AC and DC load power.
- · Transition state power.

Output stage power is:

Po =
$$P_{DC}$$
 + PAC
= $V_0 (I_{DC}) + f C_L V_S^2$

Where:

Vo = DC output voltage

I_{DC} = DC output load current
f = Switching frequency
Vs = Supply voltage

In power MOSFET drive applications, the P_{DC} term is negligible. MOSFET power transistors are high-impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

During output level state changes, a current surge will flow through the series-connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF". The current spike flows only during output transitions. The input levels should not be maintained between the logic '0' and logic '1' levels. Unused driver inputs must be tied to ground and not be allowed to float. Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

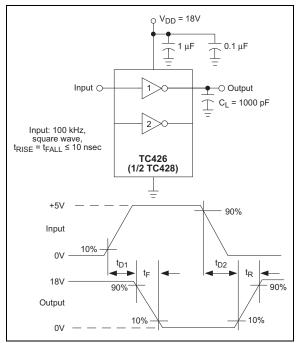


FIGURE 3-1: Inverting Driver Switching Time Test Circuit.

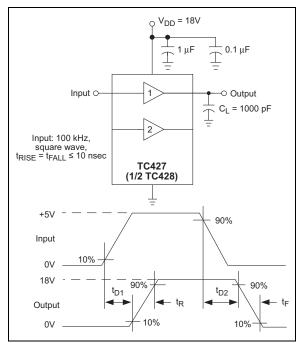


FIGURE 3-2: Noninverting Driver Switching Time Test Circuit.

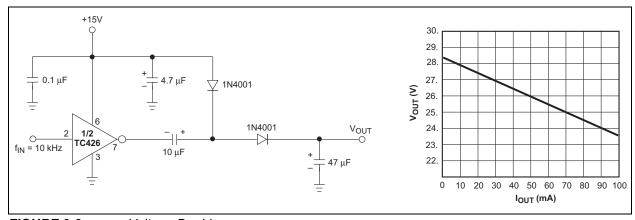


FIGURE 3-3: Voltage Doubler.

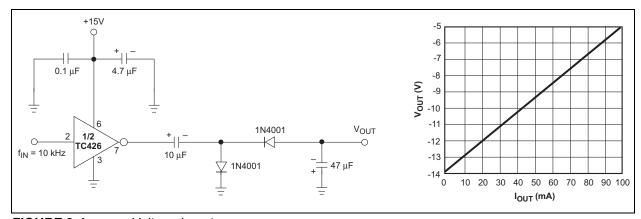
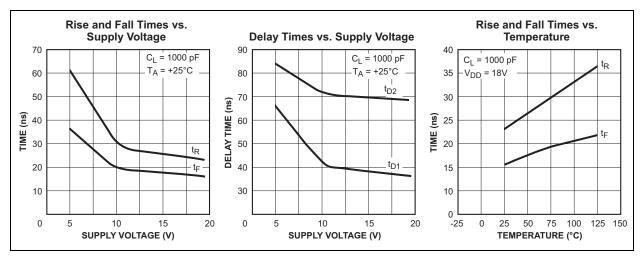
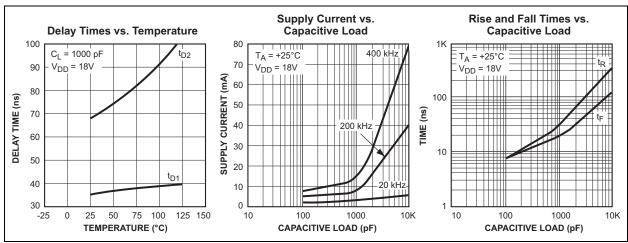


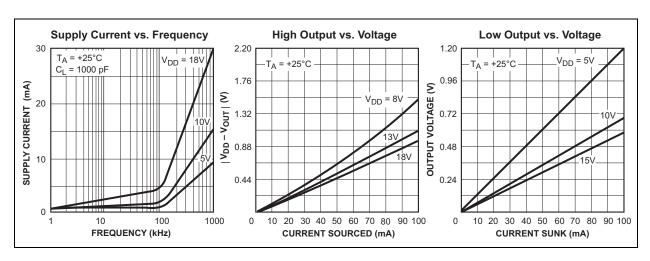
FIGURE 3-4: Voltage Inverter.

4.0 TYPICAL CHARACTERISTICS

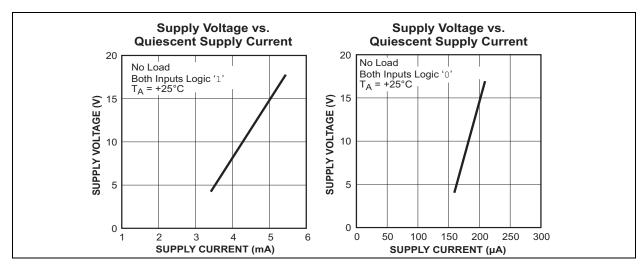
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

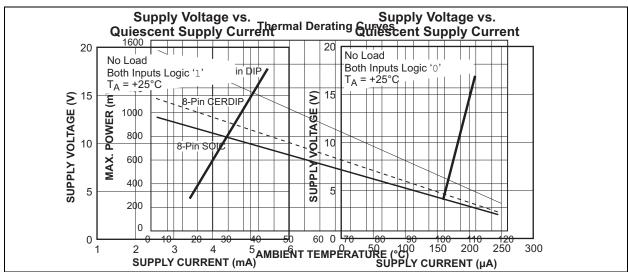






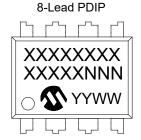
TYPICAL CHARACTERISTICS (CONTINUED)



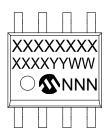


5.0 PACKAGING INFORMATION

5.1 Package Marking Information



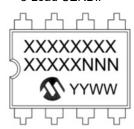
8-Lead SOIC



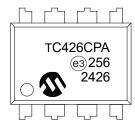
8-Lead MSOP



8-Lead CERDIP



Example



Example



Example



Example



Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

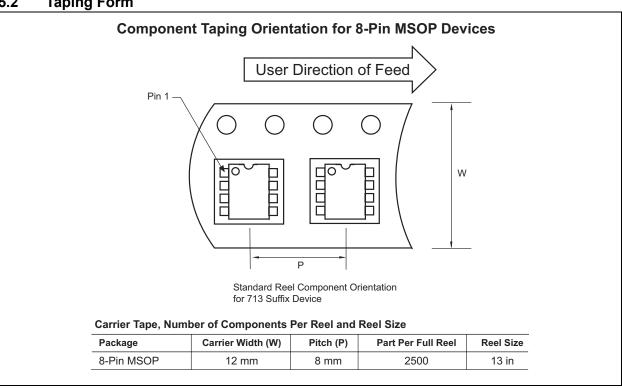
e3 Pb-free JEDEC® designator for Matte Tin (Sn)

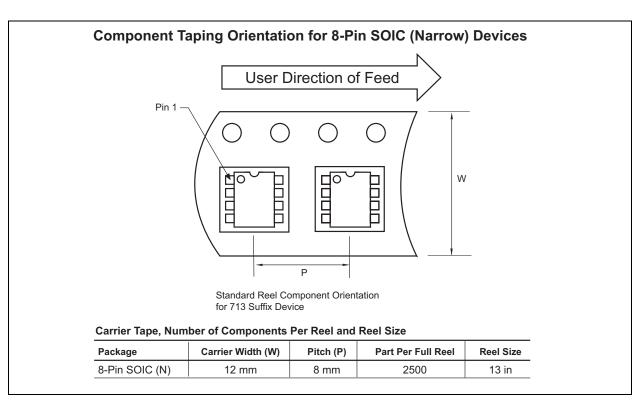
This package is Pb-free. The Pb-free JEDEC designator (@3)

can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5.2 **Taping Form**

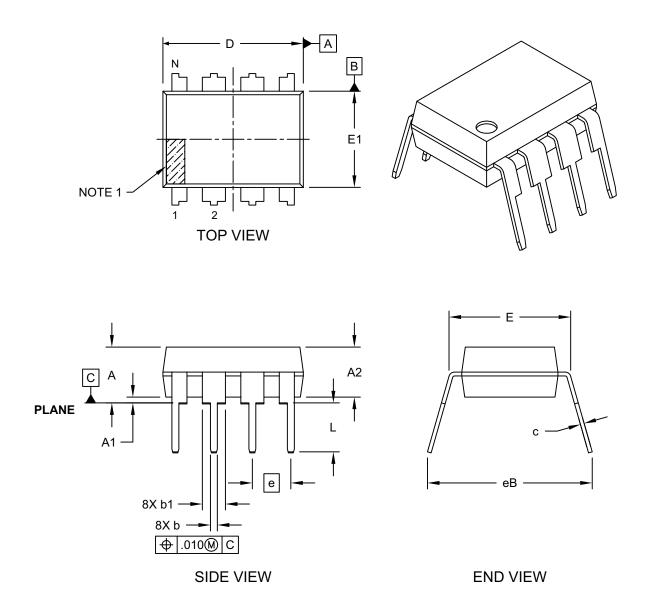




5.3 Package Dimensions

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP] Atmel Legacy Package

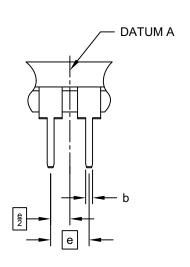
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



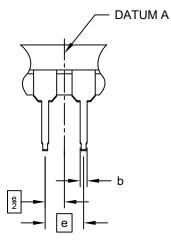
Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 1 of 2

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP] Atmel Legacy Package

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



ALTERNATE LEAD DESIGN (NOTE 5)



		INCHES		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		.100 BSC	
Top to Seating Plane	Α		-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	1	•
Shoulder to Shoulder Width	Е	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eВ	-	-	.430

Notes:

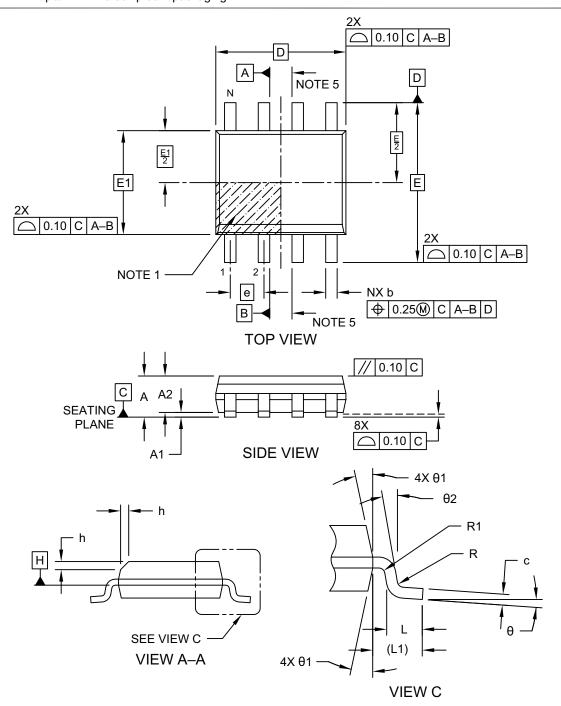
Note:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M $\,$
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 ln.) Body [SOIC] Atmel Legacy Global Package Code SWB

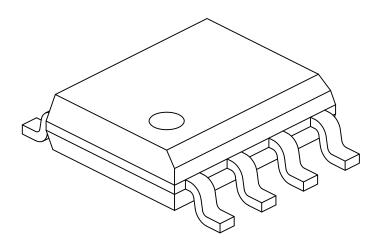
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 ln.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		1.27 BSC	
Overall Height	Α	-	ı	1.75
Molded Package Thickness	A2	1.25	1	-
Standoff §	A1	0.10	ı	0.25
Overall Width	Е		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	1	0.50
Foot Length	L	0.40	ı	1.27
Footprint	L1		1.04 REF	
Lead Thickness	С	0.17	-	0.25
Lead Width	b	0.31	1	0.51
Lead Bend Radius	R	0.07	1	_
Lead Bend Radius	R1	0.07	-	_
Foot Angle	θ	0°	_	8°
Mold Draft Angle	θ1	5°	-	15°
Lead Angle	θ2	0°	-	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

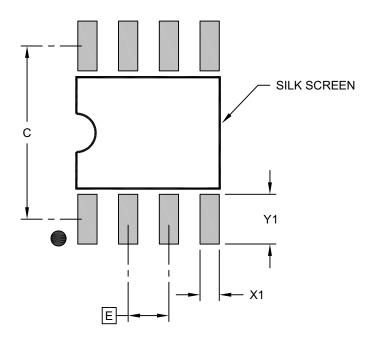
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 ln.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	IILLIMETER	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

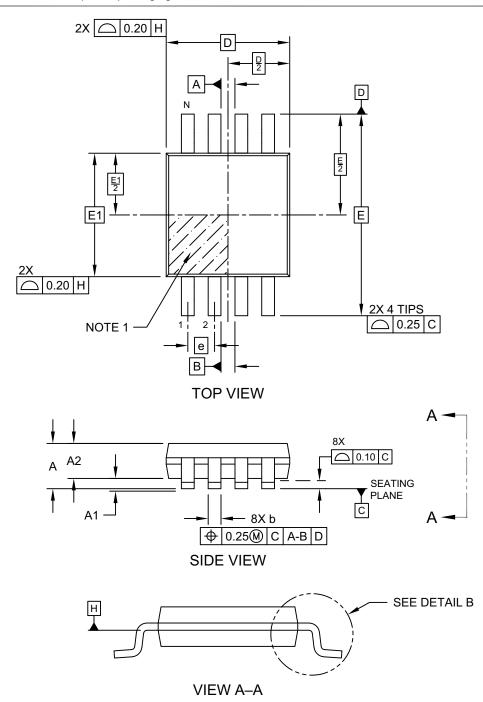
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

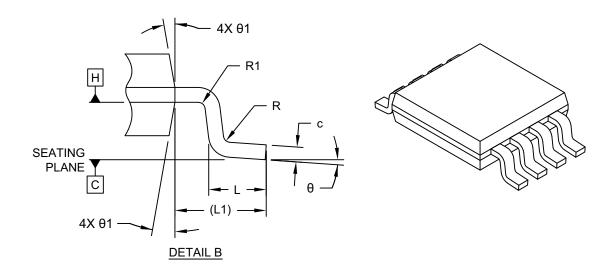
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111-A3X Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimensio	n Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	е		0.65 BSC	
Overall Height	Α	ı	_	1.10
Standoff	A1	0.00	_	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	Е		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	_	0.40
Terminal Thickness	С	0.08	_	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	_	-
Lead Bend Radius	R1	0.07	_	_
Foot Angle	θ	0°	_	8°
Mold Draft Angle	θ1	5°	_	15°

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M

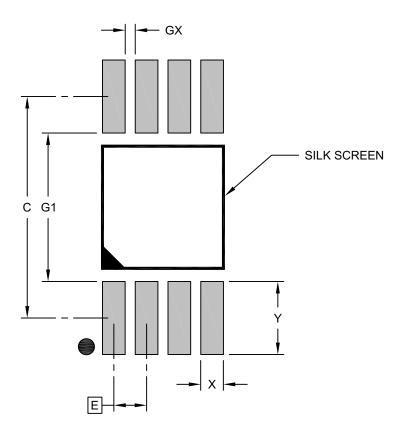
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-A3X Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	IILLIMETER	S	
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E 0.65 BSC			
Contact Pad Spacing	С		4.40	
Contact Pad Width (X8)	Х			0.45
Contact Pad Length (X8)	Υ			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

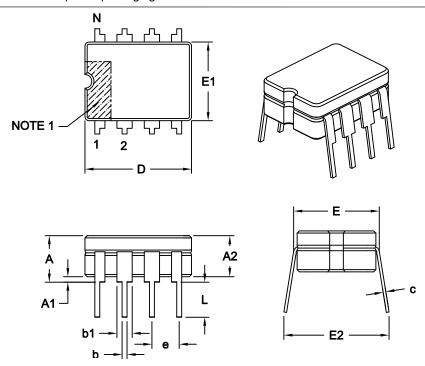
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-A3X Rev F

8-Lead Ceramic Dual In-Line (JA) ~ .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	ı	-	.200
Base to Seating Plane §	A1	.015	-	1
Ceramic Package Height	A2	.140	-	.175
Shoulder to Shoulder Width	Е	.290	-	.320
Ceramic Pkg. Width	E1	.230	.248	.300
Overall Length	D	.370	.380	.400
Tip to Seating Plane	L	.125	-	.200
Lead Thickness	С	.008	-	.015
Upper Lead Width	b1	.045	_	.065
Lower Lead Width	b	.015	-	.023
Overall Row Spacing	E2	.314	_	.410

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-001C

APPENDIX A: REVISION HISTORY

Revision E (June 2025)

- Update Features, General Description and Section 3.4, Power Dissipation.
- Added MSOP package information throughout the document.
- Updated measurement unit in Section 4.0
 "Typical Characteristics", graphic "Supply
 Voltage vs. Quiescent Supply Current", No load,
 Both Inputs Logic '0'.
- Updated Section 5.0 "Packaging Information" by adding Package Markings Information and Package Outline Drawings.
- Removed Device Selection Table and added Section "Product Identification System".
- Minor text and format changes throughout.

Revision D (December 2012)

· Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

D4 D7 110	y ng(1)	Examples:
Device	X /XX [X] ⁽¹⁾	a) TC426COA: 1.5A Dual High-Speed Power MOSFET Driver, Inverting, 0°C to +70°C Temp. Range, 8-Lead SOIC Package, 100/Tube
Device:	TC426: 1.5A Dual High-Speed Power MOSFET Driver, Invertour TC427: 1.5A Dual High-Speed Power MOSFET Driver, Not TC428: 1.5A Dual High-Speed Power MOSFET Driver, Cor	ninverting -40°C to +85°C Temp. Range,
Temperature Range:	C = 0°C to +70°C E = -40°C to +85°C I = -25°C to +85°C	c) TC427IJA: 1.5A Dual High-Speed Power MOSFET Driver, Noninverting, -25°C to +85°C Temp. Range, 8-Lead CERDIP Package, 56/Tube
Package:	M = -25 C to +85 C $M = -55 °C to +125 °C$ $PA = 8-Lead PDIP$	d) TC427MJA: 1.5A Dual High-Speed Power MOSFET Driver, Noninverting, -55°C to +125°C Temp. Range, 8-Lead CERDIP Package, 56/Tube
Tape and Reel:	OA = 8-Lead SOIC JA = 8-Lead CERDIP UA = 8-Lead MSOP Blank = Tube, 60/Tube (8-Lead PDIP option only) Blank = Tube, 100/Tube (8-Lead MSOP/SOIC option only)	e) TC427EOA713: 1.5A Dual High-Speed Power MOSFET Driver, Noninverting, -40°C to +85°C Temp. Range, 8-Lead SOIC Package, Tape and Reel, 3300/Reel
	Blank = Tube, 56/Tube (8-Lead CERDIP option only) 713 = Tape and Reel, 3300/Reel (8-Lead MSOP/SOIC	f) TC428CPA: 1.5A Dual High-Speed Power
		g) TC428COA713: 1.5A Dual High-Speed Power MOSFET Driver, Complementary, 0°C to +70°C Temp. Range, 8-Lead SOIC Package, Tape and Reel, 3300/Reel
		Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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