EVB-LAN9698-10port Hardware Manual

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9698-10port Hardware Manual. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

The manual layout is as follows:

- Chapter 1. "Overview" – This chapter lists additional documentation needed.
- Chapter 2. "EVB-LAN9698-10port Reference Board" – This chapter provides a brief overview of the reference board and its main features.
- Chapter 3. "Management Software" – This chapter provides information on the software management of the reference board.
- Chapter 4. "LED Indicators and Board Connectors" – This chapter is a short walk-through on identifying board connectors and LEDs.
- Chapter 5. "Detailed Hardware Description" – This chapter describes the hardware details of the reference board.
- Chapter 6. "Environmental Requirements" – This chapter describes the environmental requirements.
- Appendix A. "PCB Layout" – This chapter shows the different PCB layers, especially the routing to the DDR RAM.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003924A (08-04-25)	Initial release	

Chapter 1. Overview

1.1 INTRODUCTION

This hardware manual describes the design of the EVB-LAN9698-10port reference board, demonstrating the LAN9698RED Ethernet Switch device with Parallel Redundancy Protocol (PRP)/High-availability Seamless Redundancy (HSR). The LAN9698 has a total bridging bandwidth of 102 Gbit/s.

Regarding basic board design, the LAN9698 and other derivatives, such as the LAN9694 and LAN9696, are all very similar devices. They use the same Ball Grid Array (BGA) package, pin layout, number of Serializer/Deserializer (SerDes) macros and types. They also incorporate the VCore-IV Central Processing Unit (CPU) sub-system and associated interfaces. The main difference is the maximum bandwidth supported.

1.2 AUDIENCE

This document is developed primarily for hardware and software engineers who want to get an overview of designing products based on the LAN9698RED or its derivatives.

1.3 REFERENCES

1.3.1 Microchip Documents

Concepts and materials available in the following references may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN9698-10port Reference Schematic Design*
- *LAN9698 Data Sheet*
- *LAN8840 Tri-Speed Single PHY Data Sheet*
- *ENT-AN1187 Using the Serial GPIO/LED Controller*

1.3.2 IEEE Standards

- IEEE 802.1D™, Media Access Control (MAC) Bridges
- IEEE 802.1Q™, Bridges and Bridged Networks
- IEEE 802.3™, CSMA/CD Access Method and Physical Layer Specification
- IEEE 1588™-2019, Precision Clock Synchronization Protocol

1.3.3 (Optical) Module Standards

- SFP+ MSA, ftp://ftp.seagate.com/sff/SFF-8431.PDF

1.4 ACRONYMS AND DEFINITIONS

TABLE 1-1: ACRONYMS AND DEFINITIONS

Term	Definition
A/D	Analog/Digital
AC	Alternate Current
BGA	Ball Grid Array
CLI	Command Line Interface
CPU	Central Processing Unit
CuPHY	Copper PHY
DAC	Direct Attach Copper
DDR	Data Double Rate
DHCP	Dynamic Host Configuration Protocol
DIP	Dual In-line Package (switch)
EMI	Electromagnetic Interference (emissions)
eMMC	embedded Multi Media Card
FET	Field-Effect Transistor
GNSS	Global Navigation Satellite Systems
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HLL	Hyper Light Load
HSR	High-availability Seamless Redundancy
ICM	RJ45 connector with Integrated Magnetics
JTAG	Joint Test Access Group (IEEE1149)
LOS	Loss-of-Signal
MDIO	Management Data Input/Output
MII	Media Independent Interface
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NMEA	National Marine Electronics Association
NPI	Node Processor Interface
OCuLink	Optical Copper Link
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical layer device
PLD	Programmable Logic Device
PRP	Parallel Redundancy Protocol
PTP	Precision Time Protocol (IEEE1588)
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media-Independent Interface
RMC	Recommended Minimum Specific GNSS Data
RPM	Revolutions Per Minute
SDRAM	Synchronous Dynamic Random-Access Memory
SFP	Small Form-factor Pluggable transceiver
SFP+	Small Form-factor Pluggable transceiver for 10 Gbps
SGMII	Serial Gigabit Media-Independent Interface
SGPIO	Serial General Purpose Input/Output (GPIO)

TABLE 1-1: ACRONYMS AND DEFINITIONS

Term	Definition
SI	Serial Interface (SPI)
SyncE	Synchronous Ethernet (ITU-T G.8262/Y.1362)
TF-A	Trusted Firmware for Arm
TTL	Transistor-Transistor Logic
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus

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Chapter 2. EVB-LAN9698-10port Reference Board

2.1 INTRODUCTION

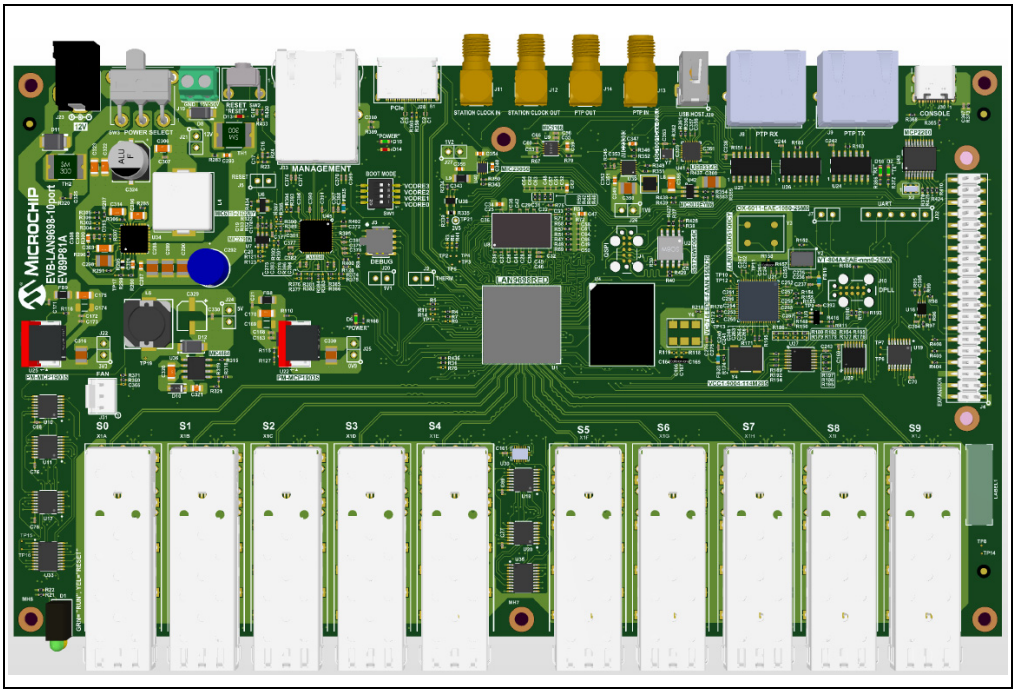
This chapter provides an overview of the reference board's features, software and hardware. See Figure 5-1 for details on the board's block diagram.

2.2 BOARD FEATURES

- One LAN9698RED Switch
- 10x SFP+ module slots (front), connected through SFI
- Network management port using LAN8840 single PHY
- USB-C port utilizing the MCP2200 for local management and software debugging
- USB-A host port utilizing the USB3343 to support memory key functionality
- Synchronous Ethernet (SyncE) DPLL ZL30732B to generate the board required clocks
- Two SMAs connectors for Precision Time Protocol (PTP) and two for Station Clock inputs and outputs
- Two ITU-T G.8275-compliant RS-422 interfaces for PTP applications
- Option for external CPU control via SPI and PCIe®
- Expansion header – Raspberry Pi® compatibility regarding power, UART and I^2C
- Barrel jack for 12V DC power and screw terminal for 48V/56V DC power

2.3 BOARD DESIGN

FIGURE 2-1: EVB-LAN9698-10PORT REFERENCE BOARD



2.4 CPU SUB-SYSTEM

2.4.1 Embedded Arm® Cortex®-A53 CPU System

By default, the LAN9698 is managed by its embedded CPU system with on-board SDRAM and Flash devices.

- Embedded Arm Cortex-A53 single core 64-bit processor operating at 1 GHz
- External memories include 1 GB DDR4 x 16 RAM (optional 2 GB can be mounted)
- 8 MB Quad Serial Peripheral Interface (QSPI) NOR and 8 GB embedded Multi Media Card (eMMC) NAND (50 MHz Data Double Rate (DDR) supported)
- Some GPIOs are implemented through the CPU sub-system Serial GPIO (SGPIO) engine (using inexpensive 74-series external shift registers) for connecting control signals to the10x SFP+ slots and for LED control

2.4.2 External CPU Connector

An external host CPU system can optionally control the LAN9698 through using either:

- PCIe 2.0 cable connector (OCuLink)
- SPI client located in the Expansion header (or in the QSPI Flash Program header)

The SPI client is set up through a specific Boot mode. The PCIe endpoint can either be set up through the SPI client or from a QSPI boot NOR Flash device.

2.5 MANAGEMENT

The embedded CPU system offers the Switch to be managed either through a Web Graphical User Interface (GUI) or through a Command Line Interface (CLI):

- Any Ethernet port connected to the Switch core can be used for local management through the Web GUI and/or Telnet/CLI session.
- A USB-C port is on-board converted to the Switch serial UART port (Flexcom0) to allow CLI access using a standard terminal application, like PuTTY or TeraTerm.

2.6 COPPER PHYS

The reference design features one Cu-port utilizing the LAN8840 single PHY, which supports pre-emption and PHY timestamping capabilities.

2.7 TIMING AND SYNCHRONIZATION

2.7.1 SyncE

The reference board supports SyncE through an on-board Microchip ZL30732B SyncE controller, which is managed as part of the general Switch management software. The on-board DPLL generates all the reference clocks used by the Switch and PHY. The clock source can be either a free-running oscillator or a clock, recovered from one of the 10G ports on the LAN9698.

The DPLL device prioritizes and selects the clock source under software control and attenuates jitter before presenting the resulting clocks for reference. A TCXO provides the base clock to the board DPLL, offering a Stratum-3 holdover. The TCXO can be removed for applications with less stringent requirements.

The board features an input and an output SMA for the DPLL device, supporting clock frequencies, such as 10 MHz, 2.048 MHz and 1.544 MHz.

2.7.2 PTP/IEEE 1588v2/802.1AS™-2020

PTP interfacing is available through all network ports with high accuracy timestamping in the LAN9698, through ITU-T G.8275-compliant RS-422 1 PPS + ToD I/O ports (ePPS header), and through two separate 1PPS input and output SMA connectors.

The Switch can be configured as boundary clock, transparent clock, PTP timeTransmitter or PTP timeReceiver. Likewise, it supports both one-step and two-step operations as well as multiple time domains.

2.8 POWER

The reference board is powered through either a standard 12V DC barrel jack or a two-pin screw terminal for 48V/56V DC power input.

The 48V/56V DC power (15V-75V input range) is locally converted to 12V DC using a Step-Down Buck-regulator, MIC28515.

A two-position switch is used to select between the external 12V or the locally generated 12V power. The 12V power sources a number of local DC/DC converters and the Fan connector.

Table 2-1 shows the power supplies generated and used on the board.

TABLE 2-1: DC/DC POWER SUPPLIES USAGE

Supply	DC/DC Converter	Used By
12V	0.9V up to 6.7A	LAN9698 Switch core and 10G SerDes I/O
	3.3V up to 5.7A	LAN8840, eMMC, ZL, USB and SFP+
	5.0V up to 1.7A	USB and DC/DC
5V	1.2V up to 480 mA	LAN9698 VDDIO_DDR and DDR4 VDD/VDDQ
	1.8V up to 1.7A	LAN9698: VDDIO, VDDH18, VDDPLLDDR LAN8840, ZL30732, eMMC, NOR
3.3V	2.5V up to 25 mA	DDR4
	1.1V up to 200 mA	LAN8840 PHY core and analog low. Locally PHY generated supply

The Expansion header can supply both 5V@0.5A and 3.3V@2A power.

NOTES:

Chapter 3. Management Software

3.1 INTRODUCTION

The reference board can be managed remotely using a browser-based Web GUI or locally through a USB serial port supporting a CLI.

3.2 CLI FOR MANAGEMENT AND DEBUGGING

The board can be connected directly to the USB port of a computer or laptop using a standard USB-to-USB Type-C® cable to access the text-based CLI.

The Windows driver and installer software file for the on-board UART converter is available at its homepage: (https://ww1.microchip.com/downloads/en/DeviceDoc/MCP2221_Windows_Driver_2021-02-22.zip).

When connected through the USB connector, the computer detects the on-board USB device, which includes giving the connection a COMx port number. From here, the port behaves like a standard serial port.

Once connected, point the Terminal program of choice to the new COM port, and set up the port to 115200 baud, 8 data bits, no parity, 1 stop bit and no flow control.

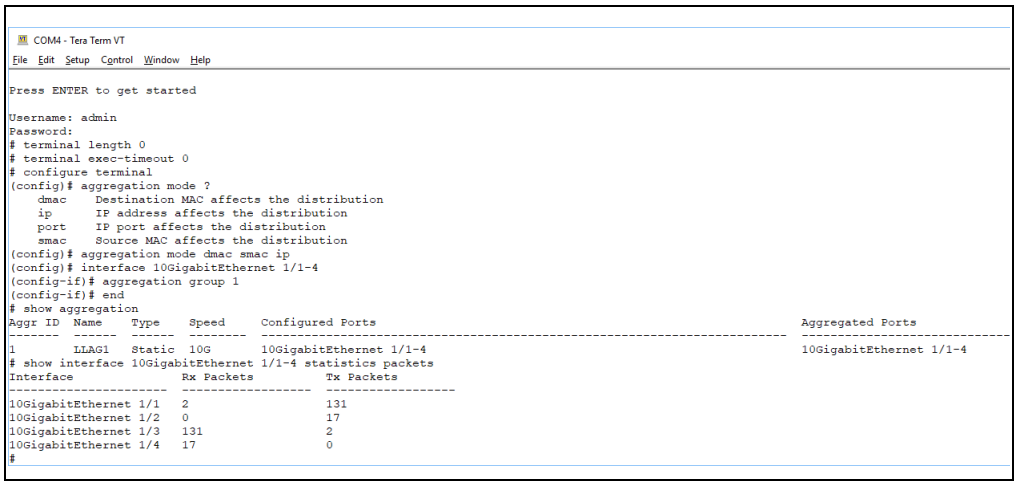
Log in to the Switch Application by using the default username, “admin” (without quotes), and leave the default password field blank. Help screens are available through the “?” or “help” command.

Note: To restore default settings and password, make a loop between ports 1 and 2 during power-on and allow the Switch Application to boot up completely.

One important use of the CLI is to determine the IP address of the Switch when Dynamic Host Configuration Protocol (DHCP) is enabled. This is done through the CLI command, “show interface vlan 1”. The command displays the IP address where the Web GUI is available.

An example of the CLI output when setting up a Static Aggregation on the 4x 10G ports is shown in Figure 3-1.

FIGURE 3-1: EXAMPLE CLI OUTPUT

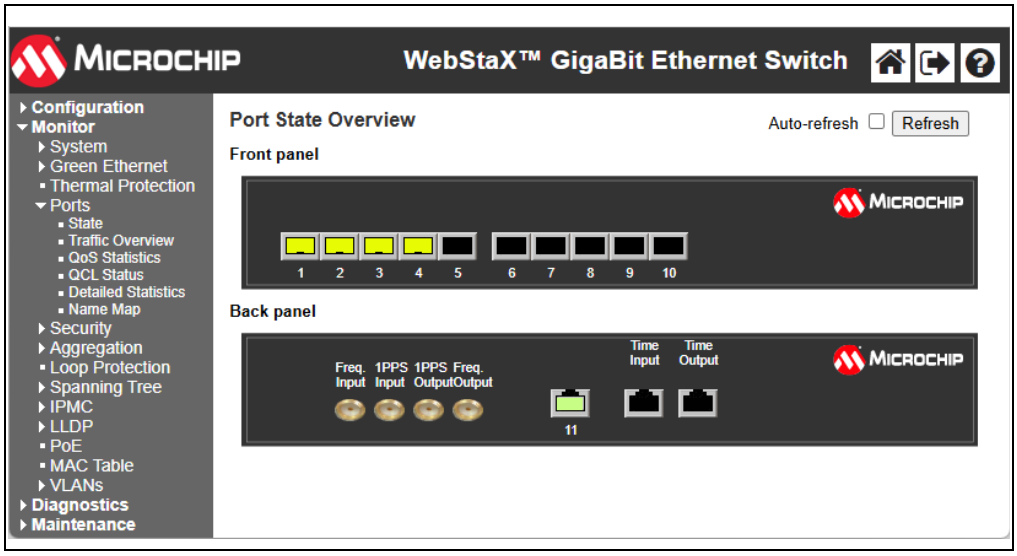


3.3 WEB GUI FOR MANAGEMENT

The Web GUI is available from a computer or laptop connected to a network port. Ensure that the computer and Switch are on the same IP subnet.

Launch a Web browser on the computer, enter the IP address of the Switch (by default, the static IP address is 192.0.2.1), and enter the login credentials when prompted. The default username is “admin” (without quotes) and the default password field should be left blank. A graphical representation of the Switch ports appears. See Figure 3-2 for the image of the Web GUI startup screen.

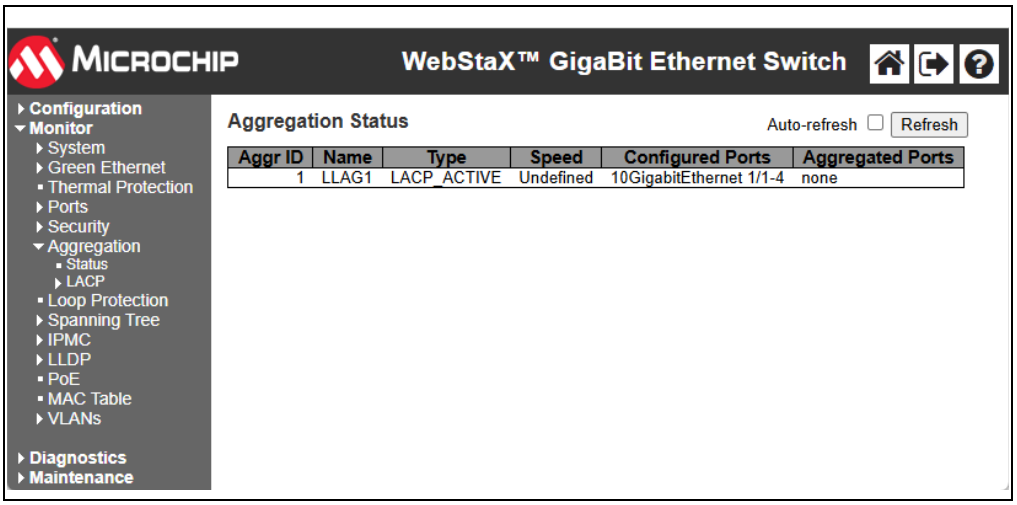
FIGURE 3-2: WEB GUI STARTUP SCREEN



Setup is done by selecting the **Configuration** menu at the top left and selecting an appropriate sub-menu item. Similarly, the status can be displayed through the **Monitor** menu. New versions of the Switch Application can be uploaded through the **Maintenance** menu. Help screens can be accessed by clicking the “?” icon located at the top right corner.

Figure 3-3 shows an example Web GUI screenshot of the status of the previous Aggregation setup.

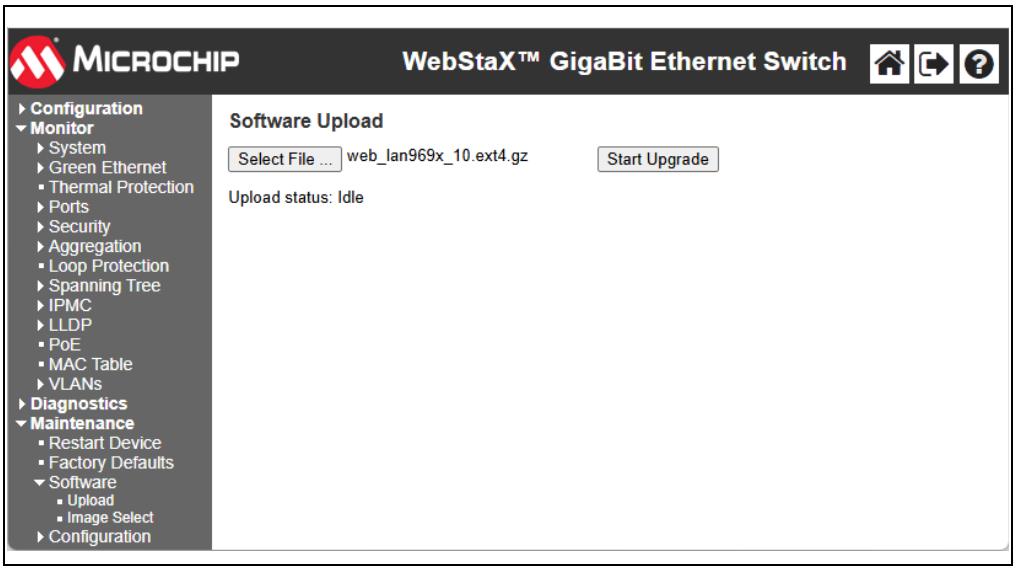
FIGURE 3-3: WEB GUI AGGREGATION STATUS



3.4 FIRMWARE UPGRADE USING WEB GUI

Figure 3-4 shows an example of doing a firmware upgrade into the on-board eMMC Flash device from the Web GUI, *Maintenance>Software>Upload* menu page.

FIGURE 3-4: WEB GUI FIRMWARE UPGRADE



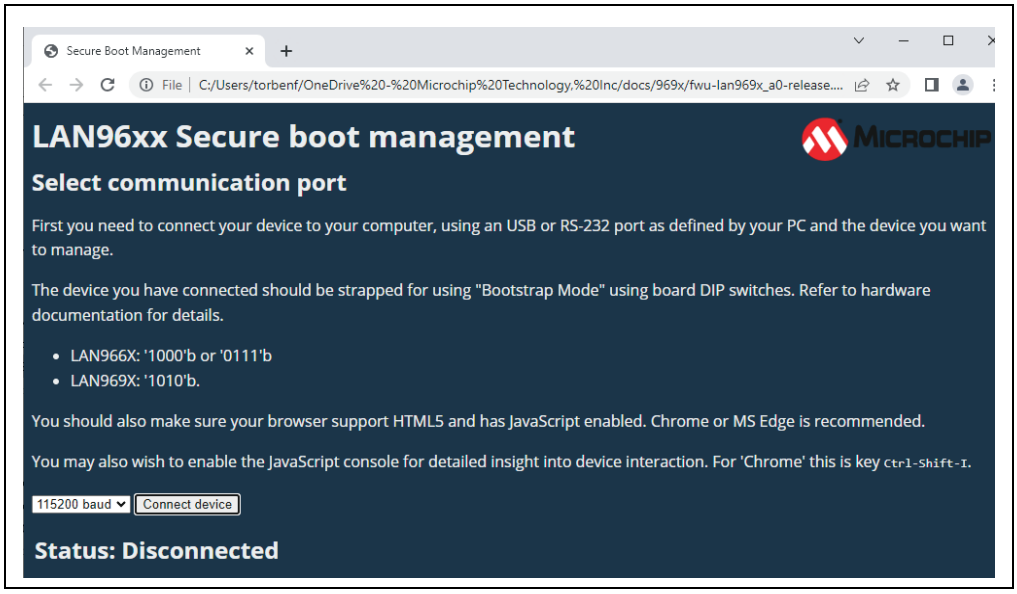
3.5 FIRMWARE UPDATE USING TRUSTED FIRMWARE FOR Arm (TF-A)

A browser-based update utility called `fwu.html` allows a simple approach for initial board bring-up or board recovering.

Complete the following steps for a firmware update:

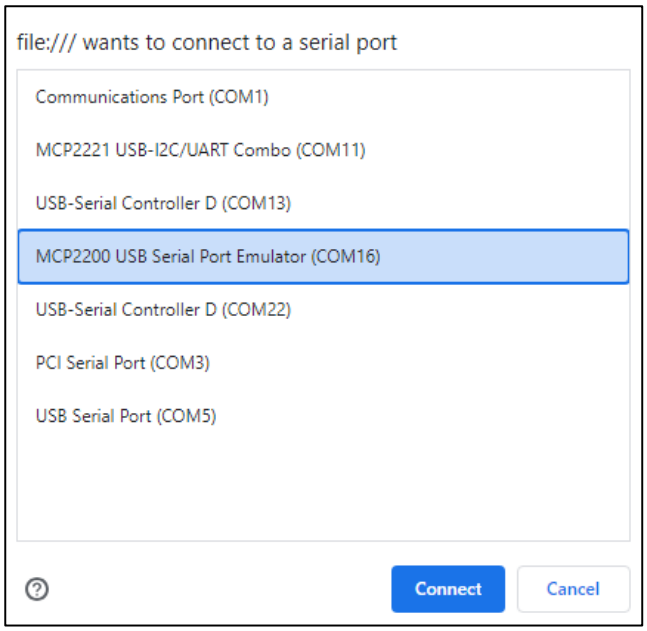
1. Connect the board directly to the USB port of a PC using a standard USB-A to USB-C cable to access the built-in Secure boot manager.
2. To have the `fwu.html` communicating with LAN9698, the board SW1 boot strapping must be set to '1010' for 115200 baud or '1011' for 921600 baud. (See Table 5-1.) The built-in bootstrap manager, BL1 will enable the FLEXCOM0 UART interface (connected to the USB port) on the next boot-up.
3. To get the latest `fwu.html` file, go to the following URL and click on the **Latest** button found on the right side of the screen, under "Releases".
   https://github.com/microchip-ung/arm-trusted-firmware.
   Download `fwu-lan969x_a0-release.html` and `lan969x_a0-release-mmc.gpt.gz`.
4. Make sure that the board's USB COM port is not assigned to a Terminal program running on the PC. If it is, then the HTML script will not work. A restart of the HTML script may be necessary after disabling the COM port from the Terminal program.
5. Use either Chrome or MS Edge browser and have the browser setting, Java-Script, enabled. Simply run the `fwu.html` file from the browser address field.
6. Click on the **Connect device** button. (See Figure 3-5.) The dialogue in Figure 3-6 appears.

FIGURE 3-5: CONNECTING TO LAN9698 FIRMWARE TOOL



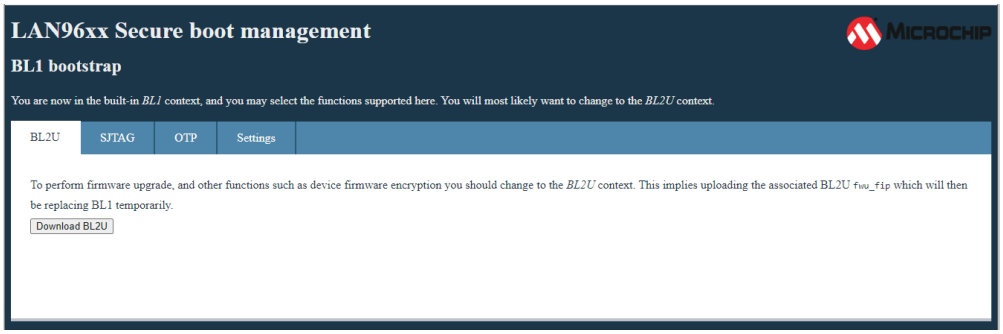
7. Select MCP2200 and click on **Connect**.

FIGURE 3-6: COM PORT SELECTION



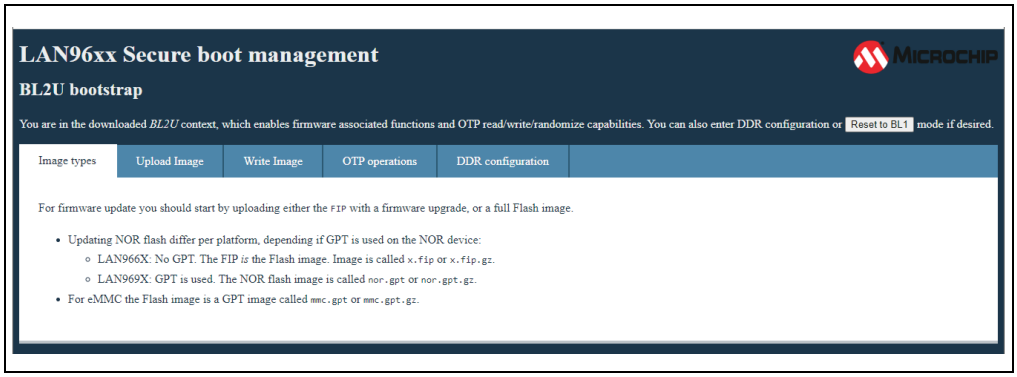
8. Once connected, Figure 3-7 appears. Click on **Download BL2U** to get the firmware update functions.

FIGURE 3-7: BL1 BOOTSTRAP PAGE



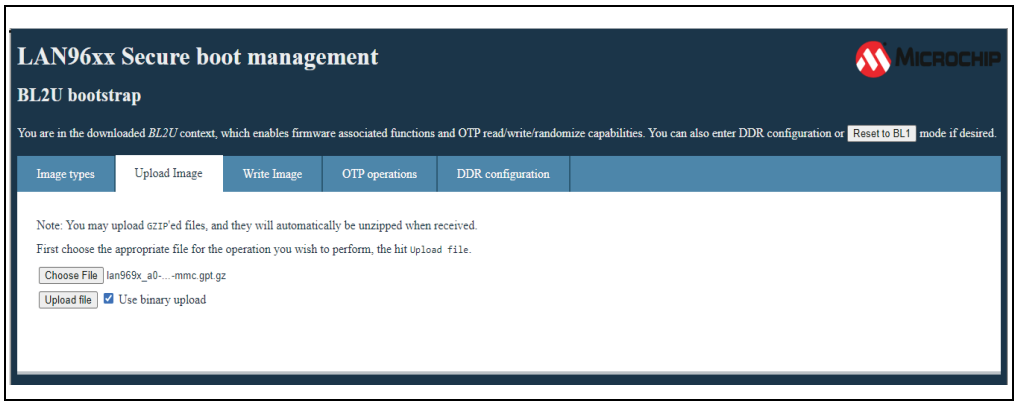
9. Within the BL2U monitor, select the **Upload Image** tab, see Figure 3-8.

FIGURE 3-8: BL2U FIRMWARE TOOLS



10. Click on **Choose File** and select the previously collected file `lan969x_a0-release-mmc.gpt.gz`, see Figure 3-9.

FIGURE 3-9: BL2U IMAGE UPLOAD

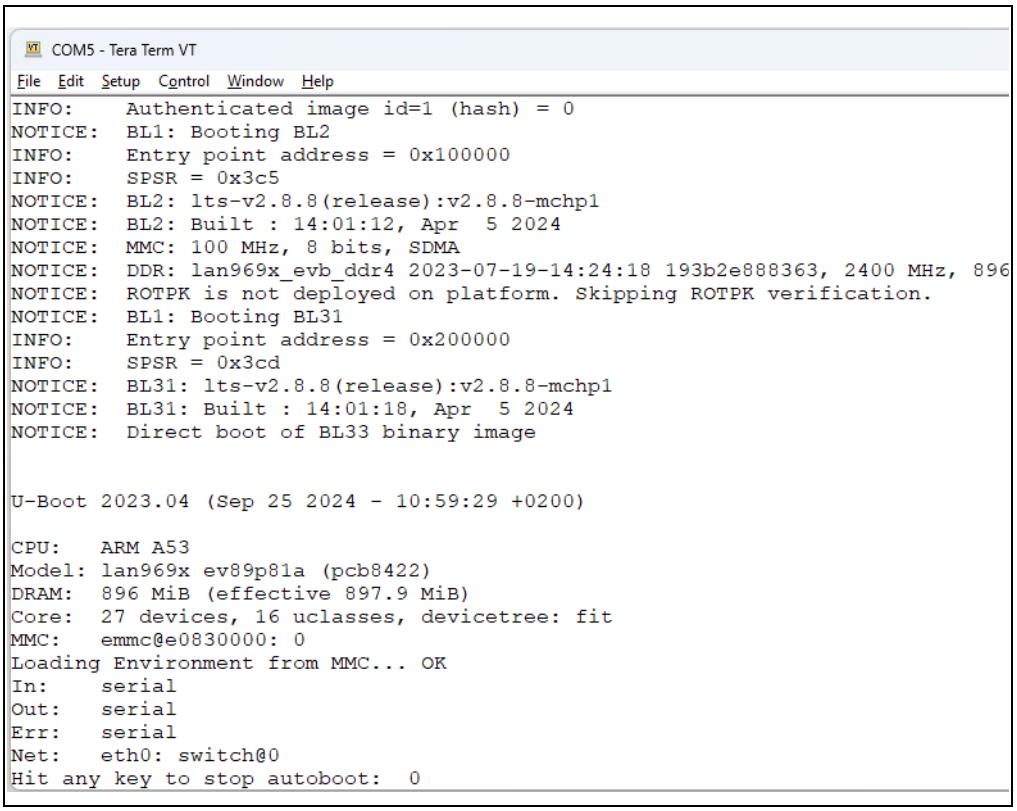


11. Click on **Upload file**. This will upload the file to the target RAM. This can take a while.
12. When done, select the next tab, **Write Image**, and choose eMMC as shown in Figure 3-10. Click on **Write Flash Image**. The Flash programming will take about 20 seconds.

FIGURE 3-10: BL2U FLASH PROGRAMMING

13. When the eMMC Flash programming is done, change SW1 DIP-switch back to '0000' and reset the board to boot up from the eMMC Flash.
14. Now, running a terminal program on your computer connected to the USB port, the U-Boot prompt in Figure 3-11 appears.

FIGURE 3-11: INITIAL BOOT LOG



15. Recommended step: Run the following commands to have the U-Boot environment match the current U-Boot version:

```
m => env default -a
m => saveenv
m => reset
```

16. Format and upload image to the on-board eMMC typed NAND Flash.
    To store the Switch Application in the eMMC, ensuring faster boot-up time, the eMMC must be formatted as indicated below. The board will automatically get an IP address from the attached network DHCP server. Once done, the download of the `ext4.gz` file from the TFTP server begins.

```
ver=U-Boot 2023.04 (Nov 07 2023 - 14:41:53 +0100)

Environment size: 4022/65531 bytes
m => setenv mmc_fw 10.205.27.2:kbp/smb_lan969x.ext4.gz
m => run mmc_boot01_dlup
switch@0 Waiting for PHY auto negotiation to complete....... done
Port  29: Up (internal)
BOOTP broadcast 1
BOOTP broadcast 2
BOOTP broadcast 3
BOOTP broadcast 4
DHCP client bound to address 10.205.28.25 (3659 ms)
Using switch@0 device
TFTP from server 10.205.27.2; our IP address is 10.205.28.25;
sending through gateway 10.205.28.1
Filename 'kbp/smb_lan969x.ext4.gz'.
Load address: 0x64000000
Loading:
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#################################################################
#########################
         4.4 MiB/s
done
Bytes transferred = 19477211 (12932db hex)
Uncompressed size: 134217728 = 0x8000000
success!

MMC write: dev # 0, block # 534528, count 262144 ... 262144 blocks
written: OK
success!

MMC write: dev # 0, block # 2631680, count 262144 ... 262144
blocks written: OK
m =>
```

17. When finished, the SW1 DIP-switch should remain at ‘0000’ for eMMC boot-up. Reset the board to reboot, and the Linux® image should start.

3.6 USING FIRMWARE UPDATE TO UPLOAD PCIE DRIVER

The LAN9698 can be controlled externally by using it as a PCIe endpoint. The SerDes macro and PCIe controller are, however, not per default setup.

The Firmware update utility can be used to upload a special `LAN969x_PCIe` image to the NOR Flash. The image configures and enables the PCIe endpoint interface. The bin file does not contain U-boot.

The `LAN969x_PCIe` image is released along with the TFA software. Go to https://github.com/microchip-ung/arm-trusted-firmware/releases/tag/v2.8.17-mchp1; under “Assets” locate and download: `lan969x_pcie-release.fip.gz`.

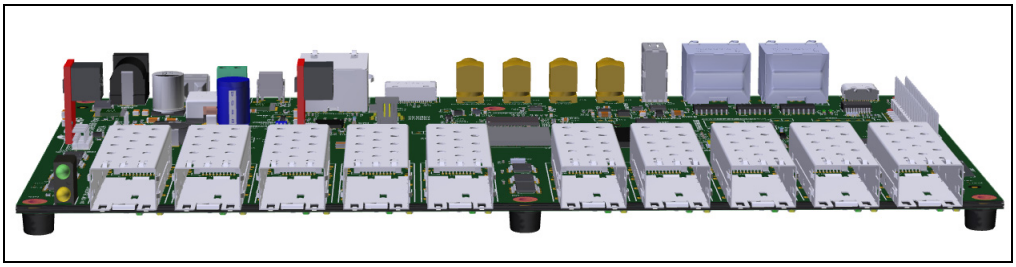
NOTES:

Chapter 4. LED Indicators and Board Connectors

4.1 FRONT BRACKET LAYOUT

Figure 4-1 shows the front bracket layout for the EVB-LAN9698-10port reference board.

FIGURE 4-1: FRONT BRACKET LAYOUT



4.1.1 Board Status and Reset LEDs

A double-LED (green/yellow, D1) is available to show the current board status. The green LED is controlled by the Switch Application, and the yellow LED is turned ON during board Reset.

4.1.2 SFP+ Slots

The reference board has 10x SFP+ slots for 10G transceivers. Each slot is organized as a single module and connects directly to the LAN9698 10G SerDes macro, S0-S9.

Each SerDes macro supports a variety of interface standards, such as SFI, 2500BASE-X, 1000Base-X and 100BASE-FX to optical Small Form-factor Pluggable (SFP) modules, as well as copper SFPs through XFI, Serial Gigabit Media-Independent Interface (SGMII) or 2.5G SGMII.

It can also support 10GBase-KR, 5GBASE-KR, 2500Base-KX, and 1000Base-KX by using Direct Attach Copper (DAC) cabling.

Under each SFP slot there are two LEDs available (green and yellow) to signal the current port status. The LED status indication is controlled through the Switch Serial GPIO engine.

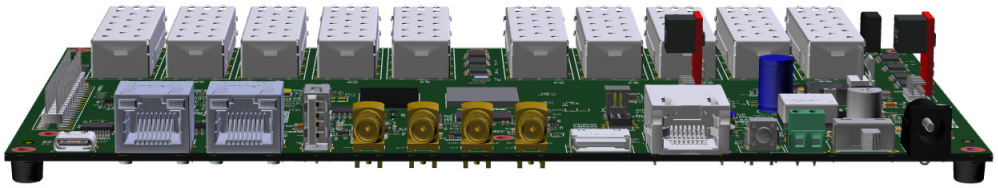
Likewise, the SFP MSA out-of-band control and monitoring of each SFP slot is made through the Switch Serial GPIO engine.

The SFP I^2C required clock muxing is made by using 2x (external) 8-channel analog multiplexers. Four select pins are controlled through the Switch Serial GPIO engine.

4.2 REAR-SIDE LAYOUT

Figure 4-2 shows the rear-side layout of the EVB-LAN9698-10port reference board.

FIGURE 4-2: REAR-SIDE LAYOUT



4.2.1 USB Type-C Serial Port

The USB 2.0 Type-C port, J30, uses an on-board serial-to-USB converter MCP2200 from Microchip. The USB driver software (Windows, Mac®, Linux) can be found at: https://www.microchip.com/wwwproducts/en/MCP2200.

The USB converter has eight GPIOs, which can control board Reset and VCORE Boot mode. Two GPIOs are controlling two data traffic LEDs: Tx (D2) and Rx (D16).

4.2.2 RS-422 Serial Time Synchronization Interface

An RS-422 serial port is available for synchronizing the PTP time of the system. It terminates into two RJ45 connectors: one PTP timeReceiver (input), J8, and one PTP timeTransmitter (output), J9.

In addition to the RS-422 serial port Rx/Tx signals for exchanging time information, the RJ45 connectors include signals for 1PPS input and output, and loopback within the PTP timeReceiver RJ45 connector.

The interface complies with the ITU-T G.8271/G.703 specification.

4.2.3 ULPI USB 2.0 Host

USB 2.0 Host mode is supported by using a USB 2.0 female type-A connector, J29, which exposes the local USB 2.0 ULPI port on LAN9698. The ULPI port is connected through a Hi-Speed USB 2.0 transceiver PHY. An on-board Power Distribution MOSFET switch provides the 5V_host sourcing, limited to 600 mA.

The actual host capabilities depend on the Linux OS system support—though a USB memory key has been tested for transferring files to the reference board. This may be used for firmware upgrading.

4.2.4 SMA Connectors

There are four SMA connectors. Two are used as inputs and two are used as outputs. The SMA inputs are LVTTL and 3V3 tolerant—they are not 5V tolerant. The SMA outputs are also providing LVTTL levels.

1. **Station Clock Input**, J11. Used for various input frequencies e.g., 1.544 MHz, 2.048 MHz and 10 MHz to the board DPLL. The clock input is AC coupled.
2. **Station Clock Output**, J12. Used to provide various frequencies e.g., 1.544 MHz, 2.048 MHz and 10 MHz from the board DPLL. The clock output is AC coupled.
3. **PTP IN**, J13. Used as 1PPS input into the board DPLL and the Switch PTP engine.
4. **PTP OUT**, J14. Used as 1PPS from either the board DPLL or the Switch PTP engine.

4.2.5 PCIe 2.0 – OCuLink Connector

The LAN9698 implements a single-lane PCIe Gen2 endpoint controller, that can be connected to any PCIe-capable system. The PCIe interface can be used by an external CPU to read and write the Switch registers.

The reference board offers PCIe connection over a standard OCuLink internal end-point, J28, when being set up as PCIe endpoint. See Table 5-12 for the OCuLink end-point connector pinout.

4.2.6 Management Port and Status LED

The Management port supports the normal tri-speed links (10/100/1000M). Despite its name, the port is treated as a normal Switch port within the Switch Application. The Management port can optionally be held in Reset until its DPPL provided clock is valid.

The associated RJ45 ICM connector has two LEDs (green and yellow). These port status LEDs are automatically controlled by the LAN8840 CuPHY. The left LED signals link (green solid) and the right LED signals traffic (yellow blinks).

4.2.7 Reset

A Reset button is available on the reference board. When pressed, it drives the input of a voltage supervisor low, thus creating a hard Reset to the board. A yellow LED (D1) and a red LED (D13) are used for indication.

If the Reset button is held, Reset is released on the voltage supervisor, but the state of the Reset button can be read by the software, once it is running again, to determine ‘long press’ and hereby setting the board back to the default setup. However, this is not currently supported by the Switch Application.

4.2.8 Power Select Switch

The slide switch, SW3, used for power selection between 12V DC (J23) or 48V/56V DC input (J19), has a 5A rating. When using the 12V DC input, the maximum current is less than 3A.

A green LED (D15) indicates Power-ON using the 5V supply. This LED is controlled by a 1.2V power good signal. Likewise, a red LED (D14) indicates 'Power failure' using the 3.3V supply.

4.3 ADDITIONAL ON-BOARD CONNECTORS

4.3.1 Expansion Header

The Expansion header can give an external CPU control over the SPI client register access interface, or it can be used for programming the on-board NOR Flash device, as the header implements a simple level conversion by using resistor dividing to support NOR Flash programming using a standard 3.3V Flash Programmer. Likewise, the on-board Boot mode strapping of VCORE_[3:0] can be overruled.

The Expansion header is partially compatible with Raspberry Pi. Global Navigation Satellite Systems (GNSS) modules (designed for RPI) can be mounted to provide GNSS time input to the system using UART (and National Marine Electronics Association (NMEA), ZDA or RMC message protocol) and 1PPS signals. (Waveshare GNSS TIMING HAT has been used, https://www.waveshare.com/neo-m8t-gnss-timing-hat.htm. Though this add-on Printed Circuit Board (PCB) requires a minor board change to route the 1PPS signal.)

Besides providing 3.3V and 5V power rails, the Expansion header exposes various Switch GPIO signals in Alternate mode as shown in Table 4-1.

TABLE 4-1: GPIO SIGNALS IN ALTERNATE MODE

Signal	Alternate Mode
I^2C	SCL, SDA (Host mode, FLEXCOM 3)
UART	RXD, TXD – RS-422 (Host mode, FLEXCOM 1)
PTP	1PPS_IN (PTP.SYNC5)
VCORE_[3:0]	Boot mode selection. SW1 must be set to '0000'.
SI	SPI.SCK, SPI.D1, SPI.D0, and SPI.nCS
Reset	Board Reset (Note that NOR Flash has no Reset)

4.3.2 Arm CPU JTAG Connector

The board has a standard JTAG/Debug 10-pin (0.05") header, J3, which can be used for boundary scan and ICE. System default is selecting ICE mode through resistor strapping.

4.3.3 QSPI Flash Program Header, 1.8V

In a production environment, the NOR boot Flash can be programmed on-board using an external 1.8V programmer connected to the QSPI Flash Program header, J1 (footprint only).

Note: Both Flash devices can also be programmed using the BL2U via the console port.

4.3.4 DPLL Programming Header, 3.3V

The board provides a DPLL programming header, J10 (footprint only), which is used with the Microchip Azurite GUI for the ZL30732B.

4.3.5 On-Die Temperature Sensor Header

Footprint for a two-pin header, J2, makes it possible to do measurements on the anode and cathode signals of the on-die thermal diode, if required. A temperature monitor like the EMC1812T-A can be used.

The Switch includes another internal thermal diode for measuring the junction temperature and an embedded Analog/Digital (A/D) converter for monitoring it through the register interface.

4.3.6 Fan Connector

A Fan connector, J31, is available next to the first SFP slot.

The Fan connector connects to a single Fan controller embedded in the Switch through a simple gating circuit. This allows for the Fan's health to be monitored at a given time through a Tacho input.

The Fan connector is powered from the 12V supply through a Pulse-Width Modulation (PWM)-controlled Field-Effect Transistor (FET) for adjustable Fan power by doing ground chopping.

4.4 BOOT MODE AND REFERENCE CLOCK

The Switch's Boot mode is strapped through its **VCORE[3:0]** pins using an on-board 4-pin DIP (Dual In-line Package) switch, SW3. System default is to boot from the on-board eMMC NAND Flash device.

These strapping input 'pins' can also be controlled from GPIO signals located on the UART-to-USB converter. This requires, however, that SW3 is set to '0000' (neutral).

Additionally, it is possible to strap the source to the core reference clock through **REFCLK_SEL**. REFCLK1 should be selected if PTP/1588 and SyncE are required to operate in separate time domains. As a default, the differential 156.25 MHz **REFCLK0** input is selected. Also this strapping pin can be controlled from the UART GPIO (**GP1**).

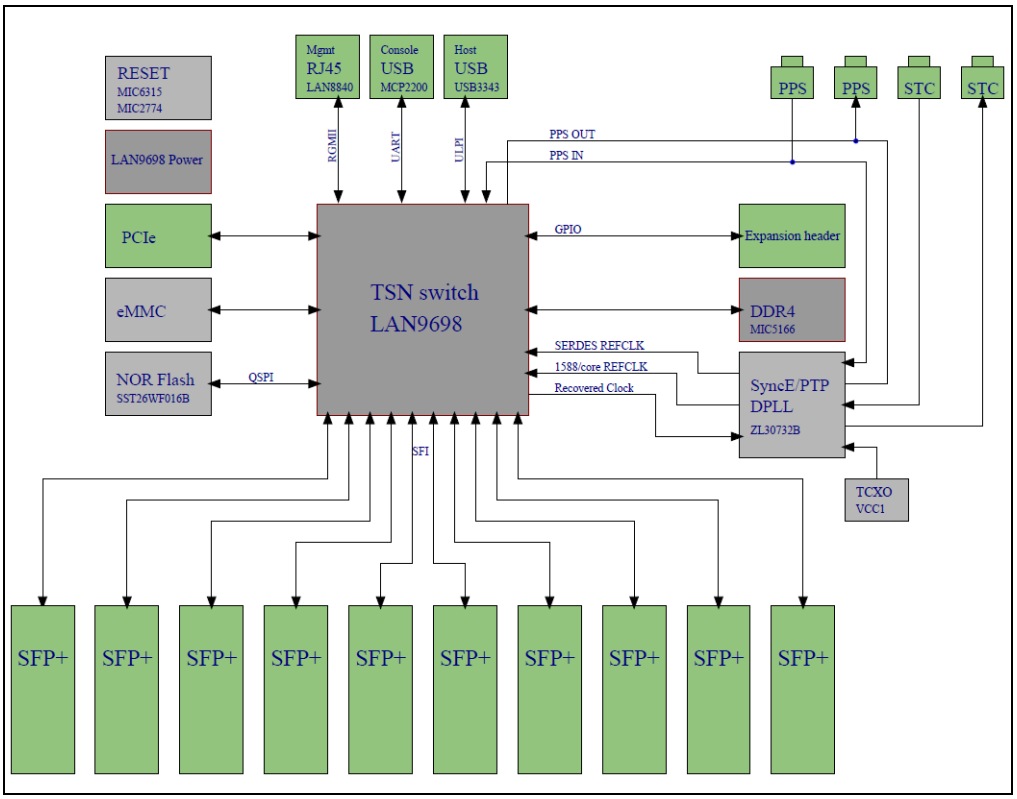
NOTES:

Chapter 5. Detailed Hardware Description

5.1 BLOCK DIAGRAM

Figure 5-1 depicts the block diagram of the EVB-LAN9698-10port reference board with its 10x SFP+ (10G) slots and one copper based tri-speed port intended for remote Management or as Node Processor Interface (NPI) for an external CPU. By default, this port functions as a standard port within the Switch.

FIGURE 5-1: EVB-LAN9698-10PORT BLOCK DIAGRAM



The design is based on the LAN9698RED Switch, which includes an Arm CPU that connects to external DDR4 SDRAM and bootable Flash devices: QSPI NOR and eMMC NAND.

Local management and software debugging are done through a dedicated UART port or any Ethernet port. The Switch's UART port is connected to a serial-to-USB converter, MCP2200. The same UART port is also be used for board bring-up, when using the `FWU.html` utility.

Optionally, the Switch can be controlled from an external CPU system connected through either a PCIe 2.0 OCuLink connector, J28, or through the SPI client found in the Expansion header, J4.

A SyncE capable DPLL ZL30732B/Azurite generates the required reference clocks to the Switch and PHY. The clock source can be either a free-running oscillator, TCXO type, or a clock recovered from one of the 10G SerDes ports.

The DPLL jitter attenuates the selected clock source and provides it back to the Switch and PHY, where it serves as reference clock. To prevent bit-wander, the generated clocks can be sourced independently, creating two separate clock domains: A SerDes clock for SyncE and a core clock for IEEE 1588.

There are four SMA connectors and two ITU-T G.8275-compliant RS-422 interfaces (1PPS + ToD input and output), which can be used for SyncE and IEEE 1588 applications.

5.2 VCORE-IV CPU SUB-SYSTEM

The LAN9698 includes an internal CPU sub-system, called VCore-IV. This sub-system has an embedded Arm Cortex-A53 single-core, 64-bit processor operating at 1 GHz and various peripheral host controllers for DDR, SD/eMMC, MIIM, USB and QSPI.

5.2.1 VCore Configuration Strapping

The Switch has four dedicated strapping pins for selection of the initial Boot mode. These are named **VCORE[3:0]**. On the reference board, Boot mode strapping is made through a dip-switch, SW1.

Table 5-1 shows the possible Boot modes that the reference board offers.

TABLE 5-1: BOOT MODE STRAPPING

VCORE[3:0]	Mode	Description
0000	eMMC FC0	Boot from eMMC Flash. Boot trace on Flexcom0 (115200/8/N).
0001	QSPI0 FC0	Boot from NOR Flash. Boot trace on Flexcom0 (115200/8/N).
0011	eMMC	Boot from eMMC Flash.
0100	QSPI0	Boot from NOR Flash.
1000	QSPI0 FC0 HS	Boot from NOR Flash. Boot trace on Flexcom0 (921600/8/N)
1010	TF-A FC0	TF-A monitor on Flexcom0 (115200/8/N)
1011	TF-A FC0 HS	TF-A monitor on Flexcom0 HS (921600/8/N)
1111	SPI client	QSPI0 is configured as SPI client. Internal CPU is disabled.

To let the Arm CPU boot from the eMMC interfaced NAND Flash device, the strapping must be set to ‘0000’ or ‘0011.’

The Flexcom0 UART interface is connected to the on-board serial-to-USB converter and is exposed on the USB Type-C connector, J30.

When the SPI client is selected, an external CPU can have access to the Switch register interface and from here setup and control the Switch device.

5.2.2 Clock Source Configuration Strapping

Through a resistor pin strap on REFCLK_SEL, the SerDes’ required 156.25 MHz differential clock is also used as base frequency for the LAN9698 Switch core. However, it is possible by changing the strapping or from the software to change configuration to use the 25 MHz reference clock input, **REFCLK1**, in IEEE 1588 applications to separate the SyncE and PTP timing domains.

5.2.3 DDR4 SDRAM

The Switch SDRAM interface is 16 bits wide and is targeted to operate at a clock rate of 1200 MHz, which therefore requires an SDRAM of speed grade 2400 Mtransfers/s or better.

The reference board is equipped with a single 1 GB DDR4 SDRAM (x16), AS4C512M16D4-75BCN. A larger SDRAM of 2 GB can optionally be mounted instead.

The DDR IO supply and the DDR_VTT termination regulator, MIC5166, are sourced by 1V2. DDR_VREF is generated by using a resistor divider on 1.2V, or it can optionally be sourced by the MIC5166.

5.2.4 eMMC NAND Flash

The VCore-IV CPU sub-system can boot directly from an eMMC interfaced NAND Flash. This is the intended and default Boot mode.

The reference board is equipped with an 8 GB eMMC NAND. Larger devices can be used, presently up to 64 GB. The eMMC can hold both the bootloader, U-boot and multiple copies of Linux and WebStaX Switch Application.

The NAND IO supply, VDDQ, is supplied with 1.8V to match the Switch IO level.

5.2.5 QSPI NOR Flash

The VCore-IV CPU sub-system can also boot from a NOR Flash device. The reference board is equipped with an 8 MB NOR QSPI boot Flash, SST26WF064C (SOIJ-8). This Flash can operate both as normal SPI and as QSPI IO mode. This NOR Flash can also hold the bootloader, U-boot (to separate bootloader and Switch Application from using the same Flash memory) or the machine protocol supporting VelocityDRIVE-SP.

Optionally, the board has footprint to instead mounting a 128MB NOR Flash, MX66U1G45G on the bottom of the PCB. This NOR Flash can like the eMMC Flash hold both bootloader and multiple copies of the OS and Switch Application.

The NOR IO supply, VDD, is supplied with 1.8V to match the dedicated QSPI on the Switch.

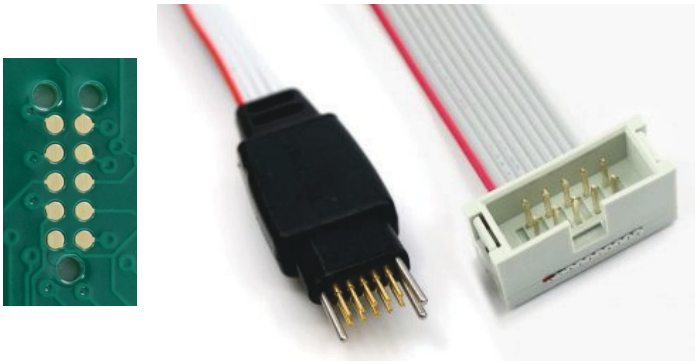
5.2.6 QSPI Flash Programming

During production, the NOR Flash can be programmed using an external Programmer either through a 2x5 pin footprint header, J1, or through the Expansion header, J4, described in Section 5.6 “Expansion Header”.

Both headers include a Reset signal, through which the Programmer can keep the Switch in Reset, and hereby releasing control of the Serial Interface (SI) Data output. This will allow the Programmer to drive the signals, while programming the QSPI NOR Flash device.

Figure 5-2 shows the footprint header and associated probe, which are intended to be used during production.

FIGURE 5-2: TC2050-NL-FP FOOTPRINT AND ASSOCIATED PROBE



The probe used is the TC2050-IDC-NL, which can be purchased from the Tag-Connect website:

https://www.tag-connect.com/product/tc2050-idc-nl-10-pin-no-legs-cable-with-rib-bon-connector

Table 5-2 describes the location of the different signals in the 2x5 pin header, J1.

TABLE 5-2: QSPI NOR FLASH PROGRAMMING FOOTPRINT HEADER, 1.8V

Pin	Direction	Signal
1	In	QSPI.CK – SPI clock to SPI Flash
2	—	GND
3	BiDir	QSPI.D1 – SPI data to/from SPI Flash
4	In	nReset – Reset signal to Switch. Can be strapped to pin 2
5	BiDir	QSPI.D2 – SPI data to/from SPI Flash
6	Out	1.8V supply – Supply and signal levels
7	In	QSPI.nCS – SPI chip select to SPI Flash
8	BiDir	QSPI.D3 – SPI data to/from SPI Flash
9	BiDir	QSPI.D0 – SPI data to/from SPI Flash
10	—	GND

5.2.7 Arm CPU JTAG Header

A standard Arm 10-pin header is used for boundary scan and ICE. Table 5-3 describes the 10-pin header.

TABLE 5-3: ARM JTAG HEADER (10 PIN, PITCH 0.05”), 1.8V

Pin	Direction	Signal	Description
1	Out	1V8 supply	Supply and signal levels
2	BiDir	TMS	JTAG Test Mode Select Input (See Note 1.)
3	—	GND	Ground
4	In	TCK	Test Clock Input
5	—	GND	Ground
6	Out	TDO	JTAG Test Data Output
7	—	KEY	—
8	In	TDI	JTAG Test Data Input
9	—	nDETECT	Not used. 10 kΩ pull-up
10	In	nRSTD	JTAG_CPU_nRST – can be modified to be general Switch Reset, nRESET.

Note 1: Bidir in SingleWire Debug mode.

The Switch provides a JTAG_SEL input signal used for selecting JTAG mode of operation. Table 5-4 shows which tap controller can be selected. Board strap default mode is CPU Tap controller.

TABLE 5-4: JTAG MODE OF OPERATION

JTAG_SEL	Mode
0	Test Tap controller
1	CPU Tap controller

5.2.8 FLEXCOM Usage

The VCore-IV CPU sub-system has four multi-purpose COM modules called FLEXCOM. The FLEXCOM[3:0] IOs are available as alternate functions on the GPIO pins.

5.2.8.1 UART FOR TF-A MONITOR AND CLI MANAGEMENT

The FLEXCOM0 UART is used as console port and is connected to a USB-to-UART serial converter, MCP2200.

The MCP2200 has 256-bytes user EEPROM and eight general purpose input/output pins. Four of the pins have alternate functions to indicate USB and communication status. The reference board uses the MCP2200 Tx/Rx functionality to indicate UART traffic through two green LEDs, D2 and D16.

The MCP2200 must initially be programmed to set the on-chip signals GP[5:0] mode as input. Otherwise, factory default settings will keep holding the reference board in Reset.

Table 5-5 describes the MCP2200 GPIO usage.

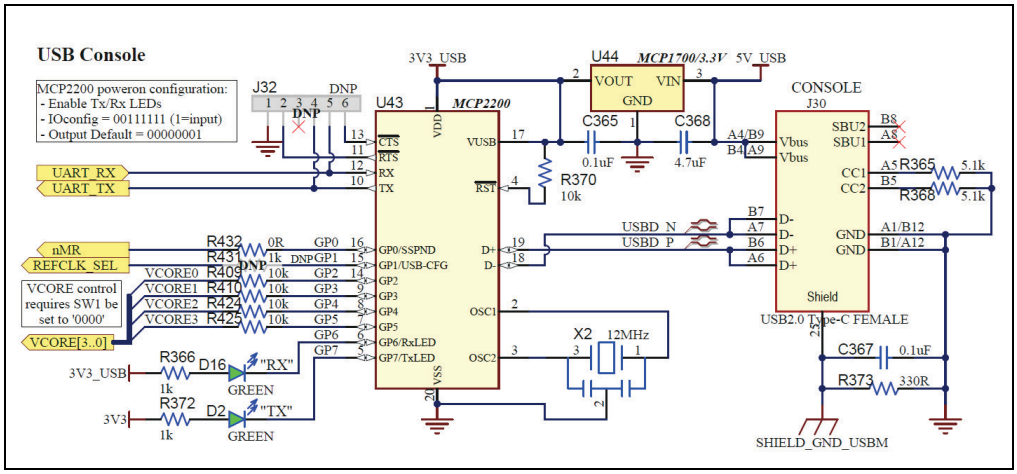
TABLE 5-5: MCP2200 GPIO USAGE

GP	Direction	Signal
0	Set as input	nMR. Board Reset. (Default set to high)
1	Set as input	REFCLK_SEL. Core clock select 0: 25 MHz 1: 156.25 MHz
2	Set as input	VCORE0 (See Note 1.)
3	Set as input	VCORE1
4	Set as input	VCORE2
5	Set as input	VCORE3
6	Out	RxLED functionality
7	Out	TxLED functionality

Note 1: SW1 must be set to '0000' when GP2-5 are in use. Table 5-1 for boot mode options.

Figure 5-3 shows the USB-to-UART Serial Conversion.

FIGURE 5-3: USB-TO-UART SERIAL CONVERSION



The USB converter is locally powered through its USB Type-C connector using a low dropout (LDO) voltage regulator, MCP1700. It awakes smoothly, when connected to a host USB.

5.2.8.2 UART FOR IEEE 1588 TIME INTERFACE – RJ45 G.703 PINOUT

FLEXCOM1 UART is connected to two RJ45-terminated RS422 connectors through the use of ISL3180E transceivers. Over temperature, ISL3180E has well-defined propagation delays in both Rx and Tx directions, and the signal levels on the RJ45 pins are standard RS422 levels.

These two RJ45 time connectors, J8 and J9, expose both the UART signals used for time information and 1PPS PTP signals. The latter includes a 1PPS output, which is located in the timeTransmitter connector, and a 1PPS load/save input, which is located in the timeReceiver connector. A feedback path can be set up (PPS_EN0) by which, the PTP timeReceiver can loopback the 1PPS signal within the same RJ45 connector, hence allowing determination of the transmission delay of the RS422 transceivers and the UTP cable between two 'time' connectors.

Table 5-6 and Table 5-7 describe the signals found in the two time connectors.

TABLE 5-6: TIMERECIEVER RJ45 CONNECTOR, J8

Pin	Direction	Signal
1	Out	1PPS FEEDBACK_TxN
2	Out	1PPS FEEDBACK_TxP
3	In	1PPS_RxN (load/save input). Local signal 1588 LD_SLV.
4	—	GND
5	Out	10 kΩ pull-down to ground
6	In	1PPS_RxP (load/save input)
7	In	UART_RxN
8	In	UART_RxP

TABLE 5-7: TIMETRANSMITTER RJ45 CONNECTOR, J9

Pin	Direction	Signal
1	In	FEEDBACK_RxN. Local signal 1588 LD_MST.
2	In	FEEDBACK_RxP
3	Out	1PPS_TxN. Local signal PTP_OUT.
4	—	GND
5	Out	10 kΩ pull-down to ground
6	Out	1PPS_TxP
7	Out	UART_TxN
8	Out	UART_TxP

Note: The FLEXCOM1 UART signals are locally converted to 3.3V and can also be found in the Expansion header, J4.

5.2.8.3 SERIAL INTERFACE FOR DPLL CONTROL

FLEXCOM2 SPI host interface is being used to control the on-board DPLL. This serial interface consists of the usual signals SPI clock DPLL.SCK (SCLK), data out DPLL.STX (MOSI), data in DPLL.SRX (MISO) and chipselect DPLL.nCS (nCS).

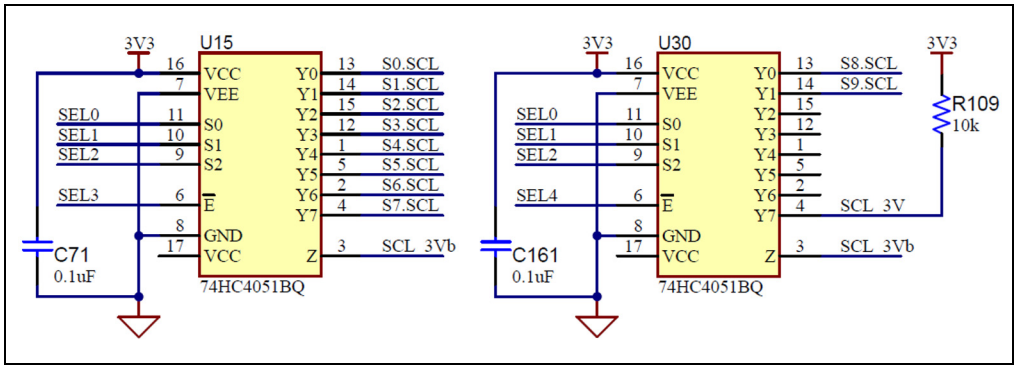
5.2.8.4 I^2C INTERFACE

FLEXCOM3 TWIHS is being used to offer a general I^2C interface for various usage: SFP and to support devices connected on the Expansion header, J4. Before use, the two I^2C signals, SCL and SDA, are voltage level converted to 3.3V by using a PCA9306.

SFP modules include an I^2C EEPROM used for identification. However, all SFPs reside on the same I^2C address, 1010_000, thus a multi-SFP system needs an I^2C segment per SFP in order to avoid I^2C address conflicts.

The Switch has a built-in I²C multiplexer targeting this issue by offering ten gated clock signals. These separate **TWI_GATE_SCL[9:0]** lines are available on the Switch GPIO pins in Alternate mode. However, the overall GPIO usage is constrained, and therefore the reference design implements the use of two external 8-channel analog multiplexer, 74HC4051BQ devices, see Figure 5-4.

FIGURE 5-4: I²C CLOCK MULTIPLEXING



The four select pins, **SEL[3:0]**, are controlled through the Switch Serial GPIO engine. The fifth signal, **SEL4** is a simple inversion of **SEL3**.

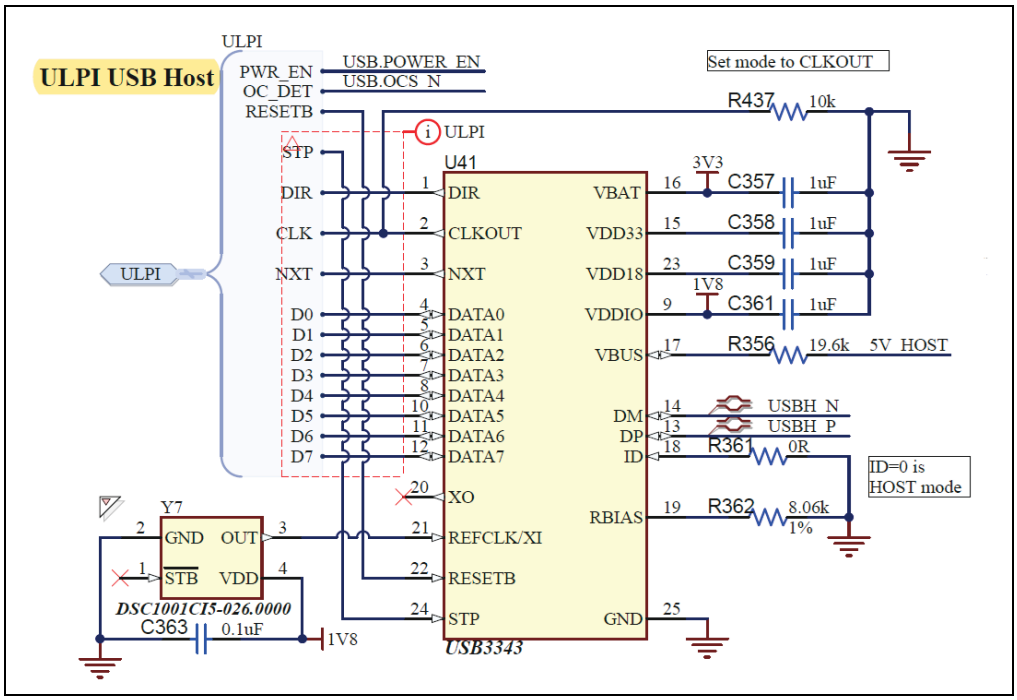
The ten **S[9:0].SCL** signals are routed to the SFP+ slots on the front. The remaining clock signal, **SCL_3V**, is routed to the Expansion header, J4.

5.2.9 ULPI USB 2.0 Host

The Switch built-in USB host controller is connected to a Hi-Speed USB 2.0 transceiver PHY, USB3343 through its ULPI port interface located on the Switch GPIO in Alternate mode.

Figure 5-5 shows how the external transceiver PHY has been implemented.

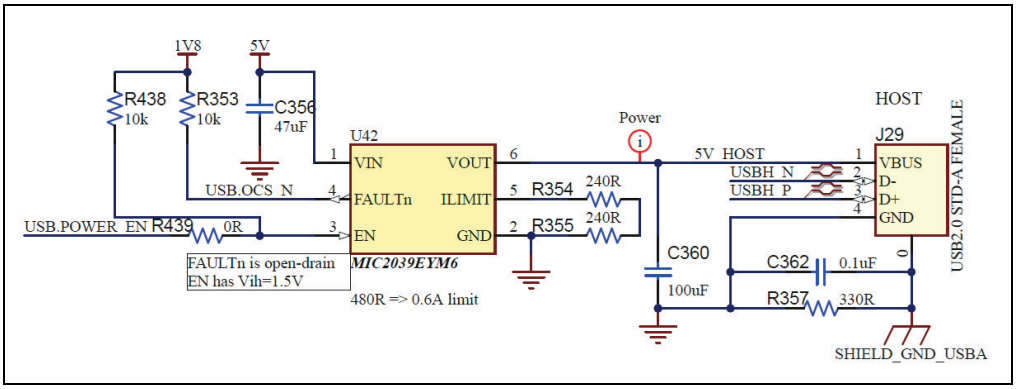
FIGURE 5-5: USB HOST PHY



USB 2.0 Host mode power sourcing is supported with a power distribution MOSFET, MIC2039. The external signals, POWER_EN (power enable) and OCS_N (overcurrent detection), are located on the Switch GPIO pins in Alternate mode.

Figure 5-6 shows how the 5V (600 mA) power sourcing is provided to the USB 2.0 type-A connector, J29.

FIGURE 5-6: USB HOST POWER SOURCING



5.2.10 Serial GPIO Controller

The Switch incorporates a Serial GPIO controller. It is documented in *ENT-AN1187 Using the Serial GPIO/LED Controller*.

Through four pins, the controller can interface to 74-series shift registers on the board to provide a flexible GPIO mechanism. The four Serial GPIO pins are located on the Switch GPIO in Alternate mode and named SG0_CLK, SG0_DO, SG0_DI and SG0_LD. These GPIO signals are locally converted between 1.8V and 3.3V.

Instead of using discrete shift registers, the external circuitry can be implemented in e.g., a central Programmable Logic Device (PLD). But the parallel inputs and outputs of this would then have to be routed across the board between the PLD and individual endpoints. By using shift registers, only the four Serial GPIO signals need to be routed “long distance” as each shift register can be distributed across the board as applicable.

In the reference design, the Serial GPIO controller is configured to use four bits per port and running 2.5 MHz. Its main task is to handle the out-of-band control signals towards the SFP slots and the RS-422 Time interface.

The design uses the following SGPIO logical ports: D0, D4, D8, D12, D16, D20, D24, D25, D26, D27 for control signals and LEDs for the 10x SFP slots. Logical ports D28 and D29 are used for control of the I^2C clock multiplexing and the RS-422 Time interface.

The SFP MSA defined signals, Tx Fault, Module Detect and Rx Loss-of-Signal (LOS), are inputs and read through 74HC165 shift registers. Each of these signals has a 10 kΩ pull-up as required per SFP MSA.

The SFP Rx LOS signals are each assigned to p[n]b[0] Serial GPIO input, which allows for a default connection within LAN9698 to the port Physical Coding Sublayer (PCS) as Signal Detect input.

Likewise, the output signals, Tx Disable, Rate Select, LED1 (green, indicating full speed) and LED2 (yellow, indicating low speed), are individually controlled through another set of shift registers using 74HC594.

As the shift register outputs are set low by the board Reset, additional inverters are required to set Tx Disable high (active) during Reset. This is done using inverting buffers, 74HC240. Likewise, the need for using pull-up resistors is also avoided.

Table 5-8 describes where the additional GPIO signals are located in the Serial GPIO engine.

TABLE 5-8: SERIAL GPIO CONTROLLER PIN DESCRIPTION

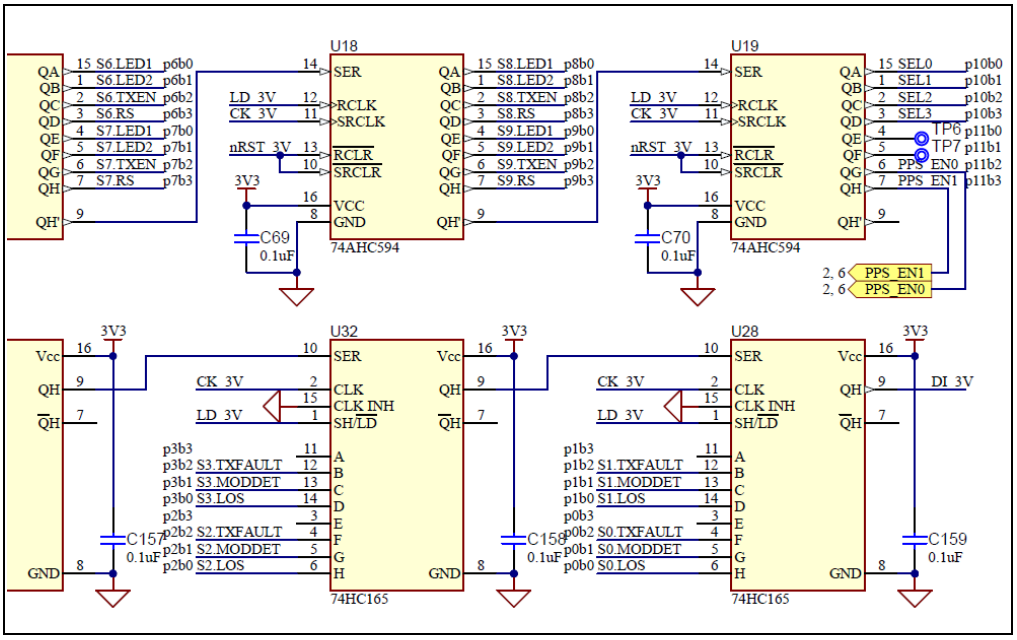
Port/Bit	Input	Output
p0b0	S0.LOS	S0.LED1
p0b1	S0.MODDET	S0.LED2
p0b2	S0.TXFAULT	S0.TXEN
p0b3	—	S0.RATESEL
p4b0	S1.LOS	S1.LED1
p4b1	S1.MODDET	S1.LED2
p4b2	S1.TXFAULT	S1.TXEN
p4b3	—	S1.RATESEL
p8b0	S2.LOS	S2.LED1
p8b1	S2.MODDET	S2.LED2
p8b2	S2.TXFAULT	S2.TXEN
p8b3	—	S2.RATESEL
p12b0	S3.LOS	S3.LED1
p12b1	S3.MODDET	S3.LED2
p12b2	S3.TXFAULT	S3.TXEN
p12b3	—	S3.RATESEL
p16b0	S4.LOS	S4.LED1
p16b1	S4.MODDET	S4.LED2
p16b2	S4.TXFAULT	S4.TXEN
p16b3	—	S4.RATESEL
p20b0	S5.LOS	S5.LED1
p20b1	S5.MODDET	S5.LED2
p20b2	S5.TXFAULT	S5.TXEN
p20b3	—	S5.RATESEL
p24b0	S6.LOS	S6.LED1
p24b1	S6.MODDET	S6.LED2
p24b2	S6.TXFAULT	S6.TXEN
p24b3	—	S6.RATESEL
p25b0	S7.LOS	S7.LED1
p25b1	S7.MODDET	S7.LED2
p25b2	S7.TXFAULT	S7.TXEN
p25b3	—	S7.RATESEL
p26b0	S8.LOS	S8.LED1
p26b1	S8.MODDET	S8.LED2
p26b2	S8.TXFAULT	S8.TXEN
p26b3	—	S8.RATESEL
p27b0	S9.LOS	S9.LED1
p27b1	S9.MODDET	S9.LED2

TABLE 5-8: SERIAL GPIO CONTROLLER PIN DESCRIPTION (CONTINUED)

Port/Bit	Input	Output
p27b2	S9.TXFAULT	S9.TXEN
p27b3	—	S9.RATESEL
p28b0	—	SEL0 (I2C_SCL slot select)
p28b1		SEL1
p28b2		SEL2
p28b3		SEL3 (Mux enable)
p29b0	—	—
p29b1		—
p29b2		PPS_EN0 (1PPS Rx enable)
p29b3		PPS_EN1 (1PPS Tx enable)

Figure 5-7 shows part of the reference board SGPIO implementation using shift registers.

FIGURE 5-7: PART OF THE SGPIO SHIFT REGISTER IMPLEMENTATION



5.2.11 Media Independent Interface (MII)-Management Bus Interface

The Switch has two MII-Management bus interfaces. Both are available on the Switch GPIO pins in Alternate mode. Only MIIM0 is used in this reference design.

MIIM0 is serving the back port LAN8840 PHY. The MII-Management address is 3.

Management Data Input/Output (MDIO) is terminated at the end using a pull-up. Drive strength for MDC is 1.

5.2.11.1 PHY INTERRUPTS

The Switch's Interrupt Controller has six dedicated Interrupt pins (operating as either input or output)—all located on the Switch GPIO pins in Alternate mode. Two pins are designated for MIIM use; however, they are not directly connected to the MDIO Controller.

In the reference design the single port CuPHY is using MIIM0_IRQ, which has a 10 kΩ pull-up.

5.2.12 Adjustable Fan Speed and Revolutions Per Minute (RPM) Monitoring

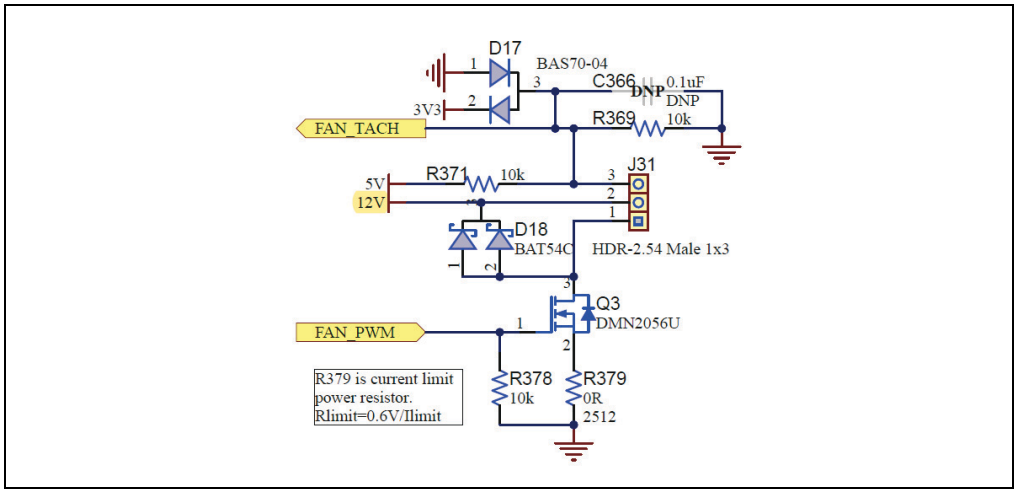
The reference board provides one Fan connector, which connects to the 12V power supply. By using the Switch built-in Fan controller, the Fan speed is adjustable through "ground chopping" with a PWM-controlled FET. Fan "health" is monitored through the Switch Tacho input. Table 5-9 describes the Fan pin header.

TABLE 5-9: FAN PIN HEADER DESCRIPTION

Pin	Description
1	Tacho input. Set point to 2.5V
2	12V output
3	Return path. Ground chopped and current limited

Both signals, PWM and TACHO, are located on the Switch GPIO pins in Alternate mode. Figure 5-8 shows the Fan control implementation.

FIGURE 5-8: FAN CONTROL



It is possible to limit the current drawn by the Fan by changing resistor R379. Changing it to 6Ω limits the current to 100 mA.

5.2.13 Switch GPIO Usage

The previous sections have described the reference board usage of the alternate GPIO features. Table 5-9 summarizes the usage of all 67 GPIO pins in the Switch. All GPIOs have an internal pull-up as their default setting.

TABLE 5-10: GPIO USAGE

GPIO	Mode	Signal	Description
0	ALT3	PCIe.PERST	PCIe Reset input
1	ALT3	USB.POW-ER_EN	USB Host Power enable output
2	GPIO	nBUTTON	Push button input. Long press detection
3	ALT1	FC0.RXD	FLEXCOM0 UART for TF-A and CLI.
4	ALT1	FC0.TXD	
5	ALT1	SGPIO.CK	Serial GPIO controller 0
6	ALT1	SGPIO.LD	
7	ALT1	SGPIO.DO	
8	ALT1	SGPIO.DI	
9	ALT1	MDC	MII-Management controller 0
10	ALT1	MDIO	
11	ALT1	MDINTn	
12	ALT3	USB.nRESET	USB Host PHY Reset output - RESETB
13	ALT3	USB.OC_DET	USB Host Over-Current Detect input
14	ALT1	eMMC.CMD	SD/eMMC host controller 0
15	ALT1	eMMC.CLK	
16	ALT1	eMMC.D0	
17	ALT1	eMMC.D1	
18	ALT1	eMMC.D2	
19	ALT1	eMMC.D3	
20	ALT1	eMMC.D4	
21	ALT1	eMMC.D5	
22	ALT1	eMMC.D6	
23	ALT1	eMMC.D7	
24	ALT1	eMMC.RSTn	
25	ALT1	PWM	PWM output
26	ALT1	TACH	Tacho input
27	ALT1	SE.RC0	SyncE Recovered Clock 0 output to DPLL
28	ALT1	FC1.RXD	FLEXCOM1 UART for RS-422
29	ALT1	FC1.TXD	

TABLE 5-10: GPIO USAGE (CONTINUED)

GPIO	Mode	Signal	Description
30	ALT2	ULPI.CLK	USB sub-system in Host mode
31	ALT2	ULPI.D0	
32	ALT2	ULPI.D1	
33	ALT2	ULPI.D2	
34	ALT2	ULPI.D3	
35	ALT2	ULPI.D4	
36	ALT2	ULPI.D5	
37	ALT2	ULPI.D6	
38	ALT2	ULPI.D7	
39	ALT2	ULPI.STP	
40	ALT2	ULPI.DIR	
41	ALT2	ULPI.NXT	
42	RGMII1	RX_D0	RGMII1 interface
43	RGMII1	RX_D1	
44	RGMII1	RX_D2	
45	RGMII1	RX_D3	
46	RGMII1	RX_CLK	
47	RGMII1	RX_CTL	
48	RGMII1	TX_D0	
49	RGMII1	TX_D1	
50	RGMII1	TX_D2	
51	RGMII1	TX_D3	
52	RGMII1	TX_CLK	
53	RGMII1	TX_CTL	
54	ALT1	SE.RC1	SyncE Recovered Clock 1 output to DPLL
55	ALT2	FC3.SCL	FLEXCOM3 TWIHS – I^2C for various use
56	ALT2	FC3.SDA	
57	ALT4	PTP.SYNC3	1PPS output to PHY’s
58	ALT4	PTP.SYNC4	1PPS output to SMA and RS-422
59	ALT4	PTP.SYNC5	1PPS input from SMA, RS-422, Expansion header
60	GPIO	nBRDRESET	Board Reset output
61	GPIO	STATUS	Status LED output – Green
62	GPIO	BoardDetect	10Ω pull-up: 1 GB DDR 10Ω pull-down: 2 GB DDR
63	ALT2	DPLL.nCS	FLEXCOM2 using Flexcom_shared_17
64	ALT1	DPLL.SCK	
65	ALT1	DPLL.SRX	
66	ALT1	DPLL.STX	

5.3 SWITCH CORE

5.3.1 Network Ports

The reference board exposes one Management Cu-port located at the back and 10x SFP+ ports at the front.

The Management port uses a single CuPHY, LAN8840, connected to the Switch's RGMII1 interface.

The configuration of the PHY is handled by the Switch Application. Details of the MII-management interface are described in Section 5.2.11 "Media Independent Interface (MII)-Management Bus Interface".

TABLE 5-11: REFERENCE BOARD PORT MAPPING

Board Port	Internal Port	Interface	Description
SFP0	D0	S0	SFI
SFP1	D4	S1	
SFP2	D8	S2	
SFP3	D12	S3	
SFP4	D16	S4	
SFP5	D20	S5	
SFP6	D24	S6	
SFP7	D25	S7	
SFP8	D26	S8	
SFP9	D27	S9	
—	D28	RGMII0	Unused
Management	D29	RGMII1	RGMII, MIIM0 address 3
PCIe	N/A	PCIE	PCIe endpoint controller

5.3.2 Copper PHY

5.3.2.1 MEDIA SIDE INTERFACE

The twisted pair interface on the copper PHY is fully compliant with the IEEE802.3-2005 specification for CAT-5 media.

The PHY integrates all passive components required to connect the PHYs' media interface to an external 1:1 transformer and common-mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The PHY supports auto-negotiation and downshift and can automatically detect the speed of a link, if auto-negotiation is disabled, providing the appropriate connection. For the current tri-speed PHY, this means 10M HDX/FDX, 100M HDX/FDX or 1000M FDX.

The PHY includes Automatic Crossover Detection functionality for all speeds (HP Auto MDI/MDI-X function) and the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled but can be disabled.

The PHY supports the IEEE standard range of 1m to 100m twisted pair cable. However:

- 1000Base-T mode requires a Category 5 enhanced cable in accordance with the cabling specifications defined by IEEE802.3-2005.
- 100BASE-TX mode requires a Category 5 cable, and 10BASE-T requires a Category 3 cable as specified in ISO/IEC 11801.

5.3.2.2 INTEGRATED MAGNETIC – ICM

Instead of separate magnetic modules and RJ45 connector, the reference board uses an RJ45 connector with integrated magnetic. This reduces the number of components on the board and the actual board area.

The Management port uses BEL L829-1J1T-43 ICM. Other pin-compatible parts may exist.

Generally, using good magnetics has a huge influence on Electromagnetic Interference (EMI) performance.

The Management port has two LEDs, located in the RJ45 connector. The green LED signals linkup and the yellow LED indicates traffic activity. The LEDs are driven from the CuPHY.

5.3.3 SFP+, SFI Interfaces

SFP signals are AC coupled in the SFP module and can therefore connect directly to the LAN9698 SFI high speed interfaces. The SFI interface can host a variety of optical modules by complying to different speeds: 10 Gbit/s, 2.5 Gbit/s, 1000BASE-X and 100Base-FX, as well as copper SFPs through XFI and SGMII. It is also possible to support 10GBase-KR, 5GBASE-KR, 2500Base-KR and 1000Base-KX by using DAC cabling.

The reference board serves 10x SFP+ slots using on-board I^2C clock multiplexing. The semi-static control signals RxLos, TxFault, TxDisable, ModuleDetect and RateSelect of the SFPs are connected to the Switch's Serial GPIO as detailed in Table 5-8. Likewise, the green and yellow LED signals to each SFP slot are also controlled by the Serial GPIO engine.

5.3.4 PCIe 2.0 Endpoint

Once enabled, the PCIe Gen2 endpoint controller gives access to the Switch registers. The PCIe endpoint does support frame injection and extraction. The maximum possible bandwidth depends on the 'horsepower' of the external CPU system. The PCIe endpoint is enabled during bootup from the bootloader, U-boot. There exists a special version of U-boot that stops further setup once the PCIe endpoint has been enabled and then stops further CPU execution—hereby allowing an external CPU getting register access to the Switch core.

Note:	The LAN9698 PCIe interface cannot operate as host/root-complex.

Table 5-12 describes the signals found in the on-board PCIe cable connector (OCu-Link). (BPTYPE = 0, no I^2C, PERST# (SB5) is open drain.)

TABLE 5-12: OCULINK PIN DESCRIPTION

Signal	Direction	Pin	Pin	Direction	Signal
3.3Vact Rx	NC	A1	B1	NC	5V
GND	—	A2	B2	—	GND
PERp0/PCIE_RX_P	In	A3	B3	Out	PETp0/PCIE_TX_P
PERn0/PCIE_RX_N	In	A4	B4	Out	PETn0/PCIE_TX_N
GND	—	A5	B5	—	GND
PERp1	NC	A6	B6	NC	PETp1
PERn1	NC	A7	B7	NC	PETn1
GND	—	A8	B8	—	GND
2W-CLK	NC	A9	B9	In	BPTYPE/VSP, 10 kΩ pull-down, no I^2C
2W-DATA	NC	A10	B10	In	CWAKEn, OBFF/VSP, 10 kΩ pull-up
GND	—	A11	B11	—	GND
PCIE_PERSTn (VSP), 10 kΩ pull-up	—	A12	B12	In	PCIE_CLK_P/VSP
CPRESNT (VSP), 1 kΩ pull-down	—	A13	B13	In	PCIE_CLK_N/VSP
GND	—	A14	B14	—	GND
PERp2	NC	A15	B15	NC	PETp2
PERn2	NC	A16	B16	NC	PETn2
GND	—	A17	B17	—	GND
PERp3	NC	A18	B18	NC	PETp3
PERn3	NC	A19	B19	NC	PETn3
GND	—	A20	B20	—	GND
5V	NC	A21	B21	NC	3.3Vact Tx
MNT. SHIELD	—	0	—	—	—

5.4 RESET CIRCUITRY

The Reset circuitry consists of two Reset signals: nCLKRESET and nRESET.

The nCLKRESET is used as master Reset to the on-board SyncE DPLL. The nCLKRESET is generated by a Microchip MIC6315-26D2UY (2.6V, 20 ms) voltage supervisor, when the 3.3V supply falls below the threshold, or the Reset button (SW2) is being pressed.

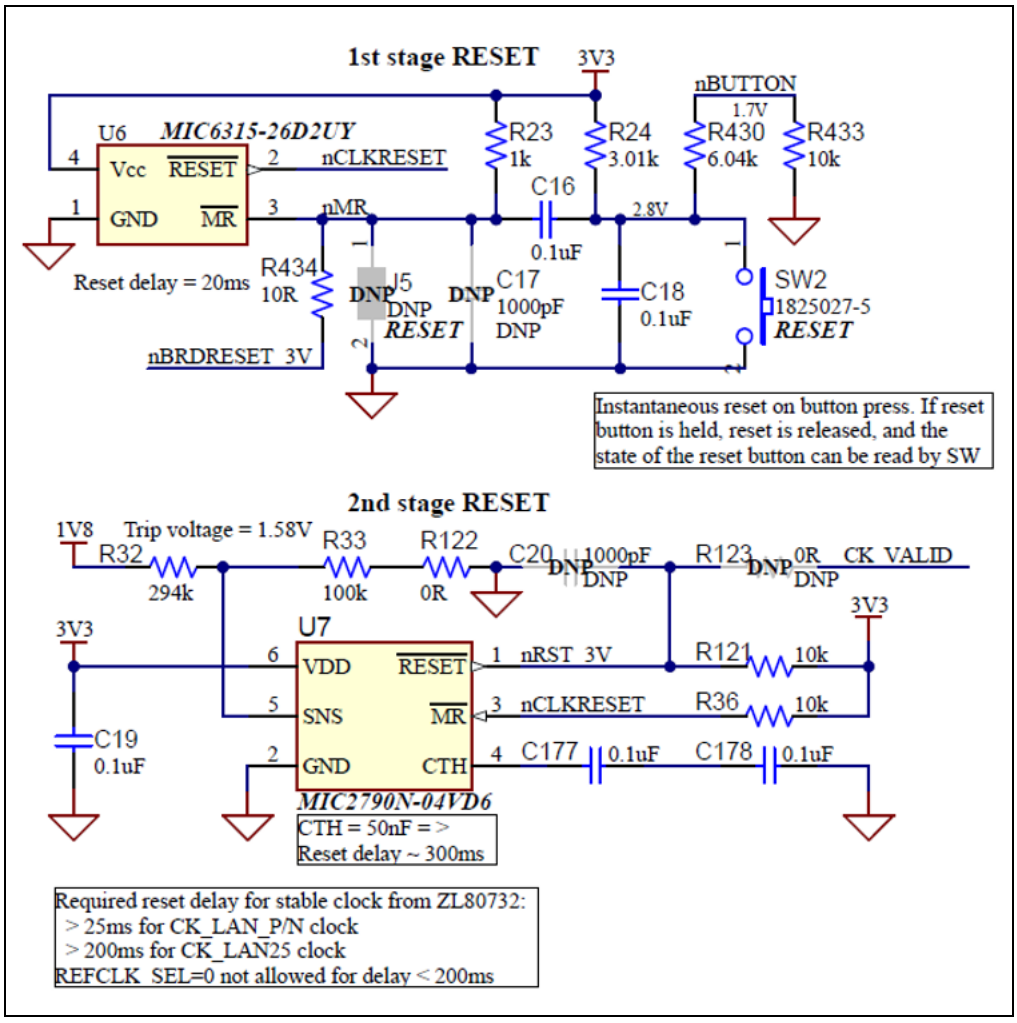
The Reset button (SW2) is available on the back of the reference board. When pressed, it drives the input of the voltage supervisor low, creating a hard board Reset. It functions as a one shot, so pressing it causes a Reset pulse, but it (nBUTTON) can afterwards be sampled by firmware to determine if it is still being pressed during boot-up, causing a “Reset to factory default”.

The nRESET is the overall board Reset and is generated by using Microchip MIC2790N-04VD6 (0.4V) voltage supervisor with programmable Reset delay. nRST_3V is asserted, when the sense voltage drops below the threshold, 0.4V, or when nCLKRESET is pulled low. The active-low Reset stays low for the duration of the Reset timeout delay once the sense voltage returns to normal and the manual Reset

transitions to a Logic High state. The Reset timeout delay period is set to 300 ms using an external 50 nF capacitor on the CTH input pin. The voltage supervisor is monitoring the 1.8V supply with threshold is set to 1.58V.

Finally, board Reset, nBRDRESET_3V can be generated from a Switch GPIO or prolonged through nRST_3V in the Expansion header, J4, see Section 5.6 “Expansion Header”.
The Reset circuitry is shown in Figure 5-9.

FIGURE 5-9: RESET CIRCUITRY



During board Reset, a yellow LED, D1 and a red LED, D13 are switched ON. The PHY Reset can optionally be controlled.

5.5 REFERENCE CLOCKS, SYNCHRONIZATION AND PTP

5.5.1 Switch and CuPHY Reference Clocks

The reference board uses differential clock distribution to the Switch and single-ended to the CuPHY used on the Management port. Differential distributed clocks offer the advantage of less jitter than single-ended clocks, which is required for complying with reference clock specifications. This is important for jitter performance reasons, when operating QSGMII and SFI interfaces. Differential clocks (buffers and PCB traces) typically emit less radiated noise than single-ended clocks.

The LAN9698 Switch core is configured for a 156.25 MHz reference clock input by pulling its **REFCLK_SEL** pin high. The CuPHY is configured for 25 MHz reference clock.

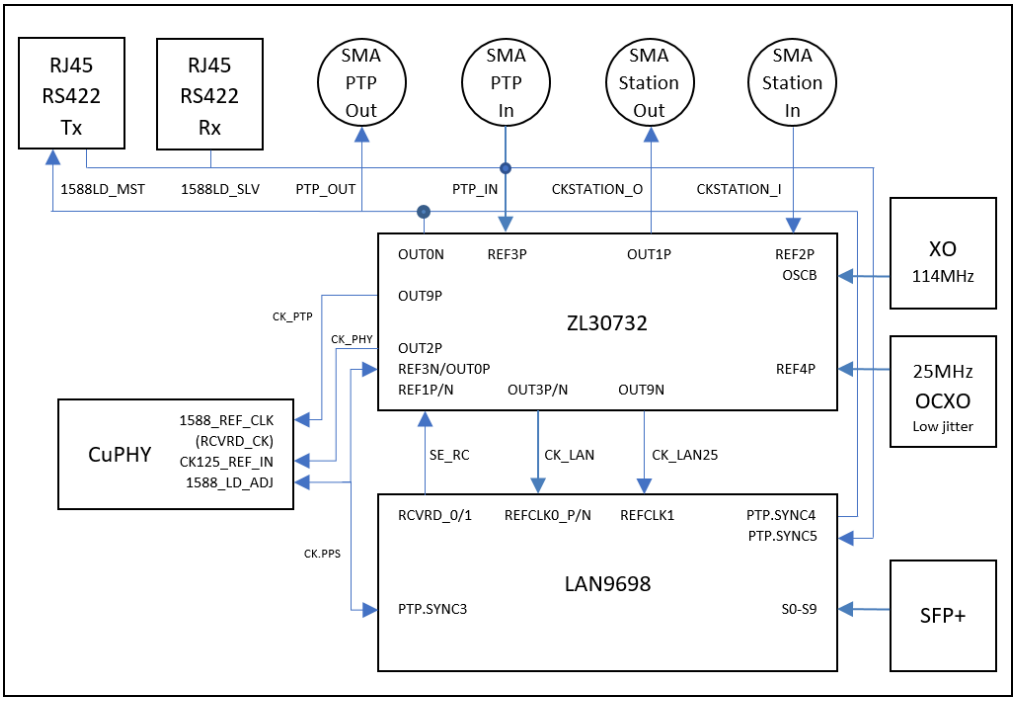
Recovered clocks, CuPHY 1588 and 1PPS clocks are distributed as single-ended clocks.

5.5.2 SyncE and PTP Generated Reference Clocks

For SyncE applications, all ports need to run from the same frequency source. Hence the reference board features central clocks that are distributed to the relevant recipients.

The reference board uses a factory pre-programmed ZL30732B as frequency multiplier and clock buffer. The ZL30732B is operating in split-XO mode using a 114.285 MHz oscillator together with a 25 MHz TCXO for increased frequency stability. Using a TCXO or an OCXO with its superior frequency stability is a requirement for some SyncE and IEEE 1588 applications, but it can be omitted in applications not requiring this. Figure 5-10 provides an overall view of the clock distribution on the reference board.

FIGURE 5-10: REFERENCE CLOCKS, RECOVERED CLOCKS, SYNCE AND PTP DIAGRAM



A design based on the EVB-LAN9698-10port reference board, which does not require SyncE and PTP capabilities, the ZL30732B can be replaced by the pin-compatible ZL30640, and the TCXO can be non-mounted.

The ZL30732B is programmed to generate the 156.25 MHz reference clock for the LAN9698 **REFCLK0** and a 25 MHz for LAN9698 **REFCLK1** (optional use), and to provide 25 MHz to the single PHY reference clock input and 125 MHz to its 1588 reference clock input for PHY timestamping.

Table 5-13 shows the ZL30732B frequency plan 00. The frequency plan is selected during Reset.

TABLE 5-13: ZL30732B FREQUENCY PLAN 'ZERO'

Signal	Description
OSCB	114.285 MHz clock input from XO
REF1	25 MHz recovered clocks from Switch (SE.RC)
REF2P	10 MHz Station Clock input from SMA (CKSTATION_I)/J11
REF2N	Optional IEEE 1588 feedback from OUT5P
REF3P	1PPS input from SMA (PTP_IN)/J13 or optionally from the Time interfaces
REF3N	1PPS feedback from Switch or DPLL 1PPS feedback
REF4P	25 MHz from TCXO (for split-XO operation)
REF4N	1PPS feedback from 1PPS clock buffer on PTP_OUT (delay compensation)
Frequency plan selection and GPIO functionality	
AC[4:0]	Pull-down. AC = '00000'. Use frequency plan zero
DPLL0 is used for SyncE. Drives Synth0 and Synth1.	
OUT1P	10 MHz Station Clock output to SMA (3.3V LVCMOS CKSTATION_O)/J12
OUT1N	TP9
OUT2P	25 MHz Management PHY reference clock (3.3V LVCMOS CK_RPHY25)
OUT2N	25 MHz SyncE feedback from DPLL (3.3V LVCMOS SE.RC0)
OUT3	156.25 MHz for Switch line reference clock (differential LVPECL CKL_P/N, 15 ms)
DPLL1 is used for PTP. Drives Synth2.	
OUT0P	1PPS to PHY's and optionally Switch (1.8V LVCMOS PTP.SYNC3)
OUT0N	1PPS to SMA, J14 and timeTransmitter, J9 (PTP_OUT converted to 3.3V)
OUT5P	Optional IEEE 1588 feedback to REF2N
OUT9P	125 MHz for single-PHY 1588 reference clock (1.8V LVCMOS CK_PTP6)
OUT9N	25 MHz for Switch 1588 reference clock (1.8V LVCMOS CK_LAN25)

5.5.3 SMA Connectors

The reference board has two input and two output SMA connectors as detailed in Table 5-14.

One input SMA connector, STATION CLOCK IN, is used for various input frequencies e.g., 1.544, 2.048 and 10 MHz into the board DPLL.

The other input SMA connector, PTP IN, is available for a 1PPS signal into the board DPLL and the Switch PTP Engine 5. Instead of coming from the SMA connector, the 1PPS input signal can also be sourced through a gated selection of the 1588 load/save signals from either the timeReceiver or timeTransmitter feedback in the two RS422 "Time" connectors. Their output enable is controlled by PPS_EN0 and PPS_EN1, respectively provided through the Serial GPIO engine.

One output SMA connector, PTP OUT, can be controlled by either the board DPLL or the Switch PTP engine 4. The other output SMA connector, STATION CLK OUT, is solely controlled by the board DPLL. This clock is generated in the SyncE clock domain. By default, the output frequency is 10 MHz. If other frequencies are wanted e.g., 1.544 or 2.048 MHz, this can be controlled by the running Switch Application.

TABLE 5-14: SMA CONNECTORS

SMA Name	Connector	Description
STATION CLOCK IN	J11	SyncE clock to board DPLL/REF2P. AC coupled
STATION CLOCK OUT	J12	SyncE clock from board DPLL/OUT1P. AC coupled
PTP IN	J13	1PPS to board DPLL/REF3P and Switch PTP.SYNC5/GPIO59 Optional 1588LD_SLV or 1588LD_MST (feedback) signal
PTP OUT	J14	1PPS from board DPLL/OUT0N or Switch PTP.SYNC4/GPIO 58

The SMA inputs are LVTTL and 3.3V tolerant - *they are not 5V tolerant*. The SMA outputs also provide 3.3V levels.

5.6 EXPANSION HEADER

The Expansion header, J4, is a 2 x 20, 0.1” pin connector and is partially Raspberry Pi compatible. It can be used for programming the NOR Flash or give an external CPU control over the SPI client register interface. It is also exposing various LAN9698 GPIO signals in Alternate mode.

The GPIO mapping towards the Expansion header can be seen in Table 5-15. All signals are 3.3V levels.

TABLE 5-15: 2X20-PIN EXPANSION HEADER, J4

Signal	Direction	Pin	Pin	Direction	Signal
3.3V	Out	1	2	Out	5V
I2C SDA (FLEXCOM3)	BiDir	3	4	Out	5V
I2C SCL (gated SEL=7)	Out	5	6	—	GND
Spare	NC	7	8	Out	UART_TxD (FLEXCOM1)
GND	—	9	10	In	UART_RxD (FLEXCOM1)
Spare	NC	11	12	In	PTP_IN (SYNCE5) (1PPS)
Spare	NC	13	14	—	GND
Spare	NC	15	16	NC	Spare
3.3V	Out	17	18	In	VCORE2
Spare	NC	19	20	—	GND
Spare	NC	21	22	In	nRST
Spare	NC	23	24	In	VCORE0
GND	—	25	26	In	VCORE1
Spare	NC	27	28	NC	Spare
Spare	NC	29	30	—	GND
Spare	NC	31	32	NC	Spare
VCORE3	In	33	34	—	GND
SPI.DI	In	35	36	In	SPI.nCS
Spare	NC	37	38	Out	SPI.D0
GND	—	39	40	In	SPI.SCK

Note: An add-on board using the Expansion header MUST have its own Power-On-Reset (POR), and the overall power consumption should be considered. Likewise, ensure that the VCORE[3:0] strapping settings are not overridden unintentionally. If the add-on board is intended to overwrite the board strapping, SW1 must be set to '0000'.

5.7 POWER DISTRIBUTION

The reference board is powered through either a standard 12V DC barrel jack, J23, or a two-pin screw terminal for 48V/56V DC power input, J19.

5.7.1 48/56V Input

The 48V/56V DC power (15V-75V input range) is locally converted to 12V DC using a step-down buck regulator, MIC28515. It can deliver a maximum of 5A and is set up to operate in HLL (Hyper Light Load) mode.

The MIC28515 offers a full suite of protection features to ensure safe operation of the device during Fault conditions. These include UVLO, external soft start to reduce current inrush, hiccup current limit short circuit protection and thermal shutdown.

5.7.2 DC/DC Converters

A slide switch, SW3, is used for power selection between 12V DC from jack or from the buck regulator. The 12V power supply sources a number of different 12V DC/DC converters:

- 0.9V for LAN9698 core supply (**VDD**) and SerDes10G IO (**VDDHS** and **VDDHV**). The DC/DC converter carries a calculated total load of 6.7A. Maximum current is 8A.
- 3.3V for SFP and CuPHY IO and analog high. The calculated load is 5.2A. Maximum current is 8A.
- 5V for USB host and additional DC/DC converters. The calculated load is 1.3A. Maximum current is 2A.

The 12V power supply also feeds direct power to the Fan connector and Expansion header. Table 5-16 summarizes the 12V power usage.

TABLE 5-16: 12V DC POWER USAGE

12V DC/DC Converters	Supply (V)	Maximum Current (A)	Power (W)
PM-MCP19035, LAN9698 Core and 10G SerDes	0.9	6.7	6.0
PM-MCP19035, LAN8840 PHY IO and SFP+	3.3	5.7	18.8
MIC4684, USB and Additional DC/DC Conversion	5.0	1.3	6.5
Power Dissipation in Supply (@80% efficiency)	—	—	7.4
Direct Use: Fan and Expansion Header	12.0	0.33	4.0
Total 12V	**12.0**	**3.56**	**42.7**

The PM-MCP19035 DC/DC Converters are located on DC/DC modules. The generated 5V DC power supply sources local DC/DC converters:

- 1.2V for LAN9698 DDR4 (**VDDIODDR**) and DDR4L RAM (**VDDQ**). The calculated load is 480 mA. Maximum current is 600 mA.
- 1.8V for LAN9698 CMOS IO (**VDDIO18**), SerDes (**VDDH**) and DDR-PLL (**VDDPLLDDR**). The calculated load is 1.7A. Maximum current is 3A.

The 5V power supply also feeds direct power to Fan control, USB host interface and the Expansion header. Table 5-17 summarizes the 5V power usage.

TABLE 5-17: 5V DC POWER USAGE

5V DC/DC Converters	Supply (V)	Maximum Current (A)	Power (W)
MIC23050, LAN9698 VDDIO DDR, and DDR4 VDDQ	1.2	0.5	0.6
MIC23303, LAN9698: VDDIO, VDDH, VDDPLLDDR ZL30732B: Core.	1.8	1.7	3.0
Power dissipation in supply (@80% efficiency)	—	—	0
Fan, Expansion header, and USB host interface	5.0	0.5	2.5
Total 5V	**5.0**	**1.3**	**6.1**

A single green LED (D15), which indicates Power-ON, is using the 5V supply.

The generated 3.3V DC power supply sources most of the board components, like eMMC NAND Flash, OC/XO's, ZL devices, SFP slots, shift registers and Expansion Header.

DDR4 VTT sink and source DDR termination regulator is sourced by 3V3. Table 5-18 summarizes the 3.3V power usage.

TABLE 5-18: 3.3V DC POWER USAGE

3.3V Devices	Supply (V)	Maximum Current (A)	Power (W)
MIC5377, 2.5V for DDR4	3.3	—	—
LAN8840 VDDIO and Analog High	3.3	0.2	0.7
ZL30732B VDD. OCXO	3.3	0.3	1.0
USB Host PHY, eMMC and Shift Registers	3.3	0.2	0.6
SFP+ Slot	3.3	5.0	16.5
Expansion Header	3.3	—	—
Total 3.3V	**3.3**	**5.7**	**18.8**

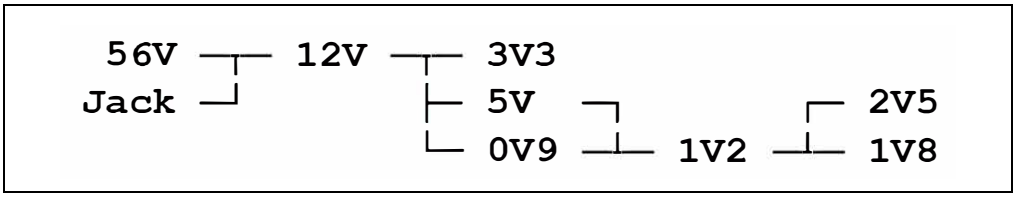
5.7.2.1 POWER SUPPLY SEQUENCING

The strategy for the power supply sequencing is not to let a higher-powered supply feeding lower-level powered grids through the device internal protection diode network. The general power supply sequence is therefore:

- LAN9698: 0V9 -> 1V2 -> 1V8
- DDR: 1V2 -> 2V5
  Note: Removing resistor R342 (PEN_2V5) will have both supplies to startup at the same time.

The overall power sequencing is illustrated in Figure 5-11.

FIGURE 5-11: POWER SEQUENCING



5.7.2.2 POWER SUPPLY, TEST POINTS

A two-pin footprint can be found on each power supply output.

- 56V: J19
- 12V: J21
- 5V: J24
- 3V3: J22
- 2V5: TP21
- 1V8: J26
- 1V2: J27
- 0V9: J25

Chapter 6. Environmental Requirements

6.1 STORAGE AND OPERATING CONDITIONS

The reference board is designed to operate within the following temperatures (case and airflow dependent):

- Operating temperature: -40° to +70°C
- Storage temperature: -10° to +70°C
- Operating humidity: 10% to 95% relative humidity, non-condensing

The reference board is provided without a case, so sufficient airflow might be needed if the air temperature is above 30°C.

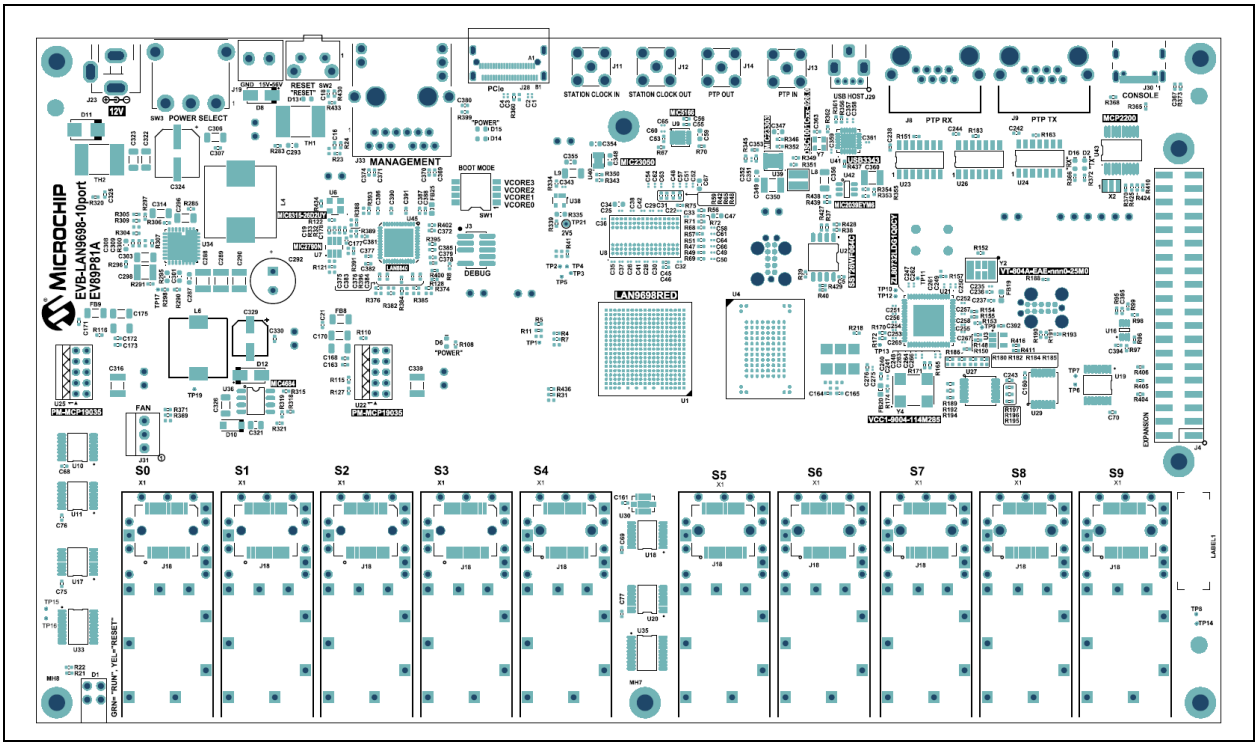
NOTES:

Appendix A. PCB Layout

A.1 DIMENSION

Figure A-1 shows the board outline. The board dimensions are 220 x 127 mm.

FIGURE A-1: EVB-LAN9698-10PORT REFERENCE BOARD OUTLINE



A.2 PCB LAYERS

The EVB-LAN9698-10port reference board uses six PCB layers, refer to Table A-1.

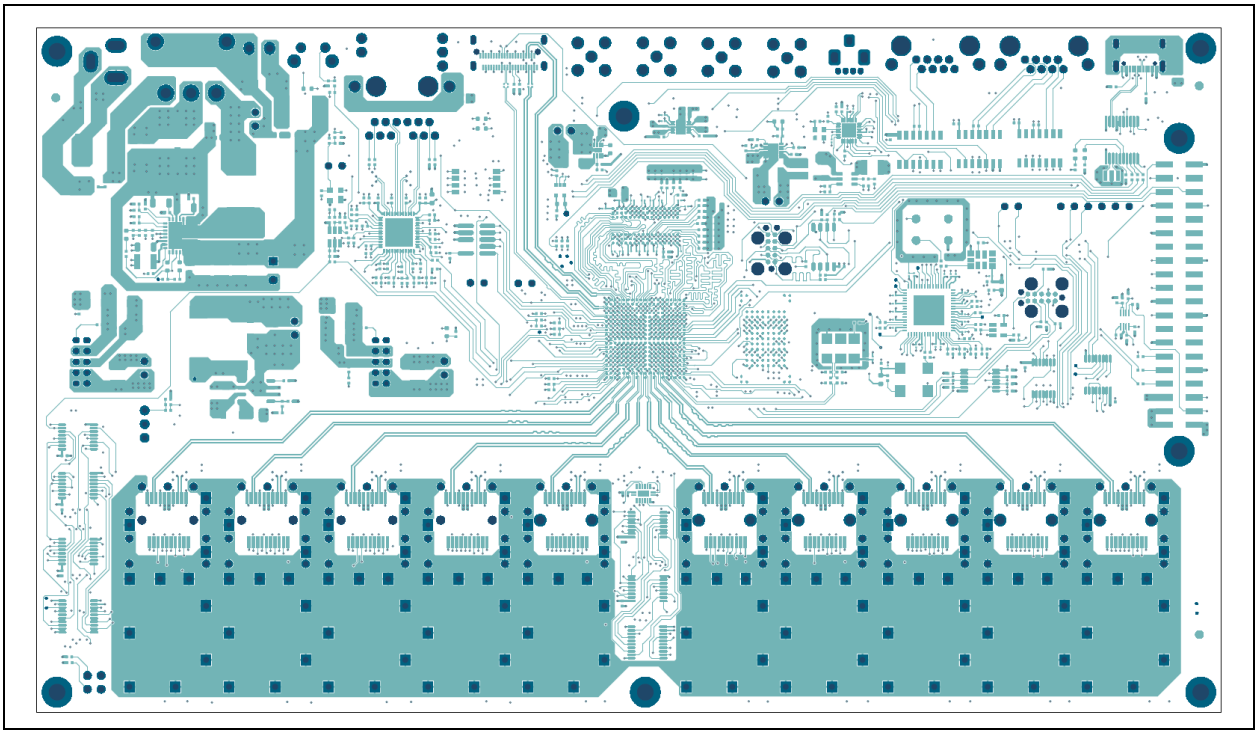
Solid ground planes on layers 2 and 5 ensure that all signals on layers 1 (top) and 6 (bottom) have a good reference plane. The two ground planes are also used to remove heat from components, and it must (also for this reason) be ensured that good connections between outer layer ground fills and the ground planes are established. (The outer layers do not have ground fill areas for copper balancing purposes.)

TABLE A-1: PCB LAYER OVERVIEW

Layer	Description
1	Top Layer. Signal traces for DDR4L. SerDes Tx paths to PHY and SFP
2	Ground Plane 1. Solid ground plane
3	Power Plane 1
4	Signal and Power Plane 2. Signal traces for DDR4L, RGMII to Single PHY
5	Ground Plane 2
6	Bottom Layer. Signal traces for DDR4L. SerDes Rx paths to PHY and SFPs

A.2.1 Layer 1 – Top Layer

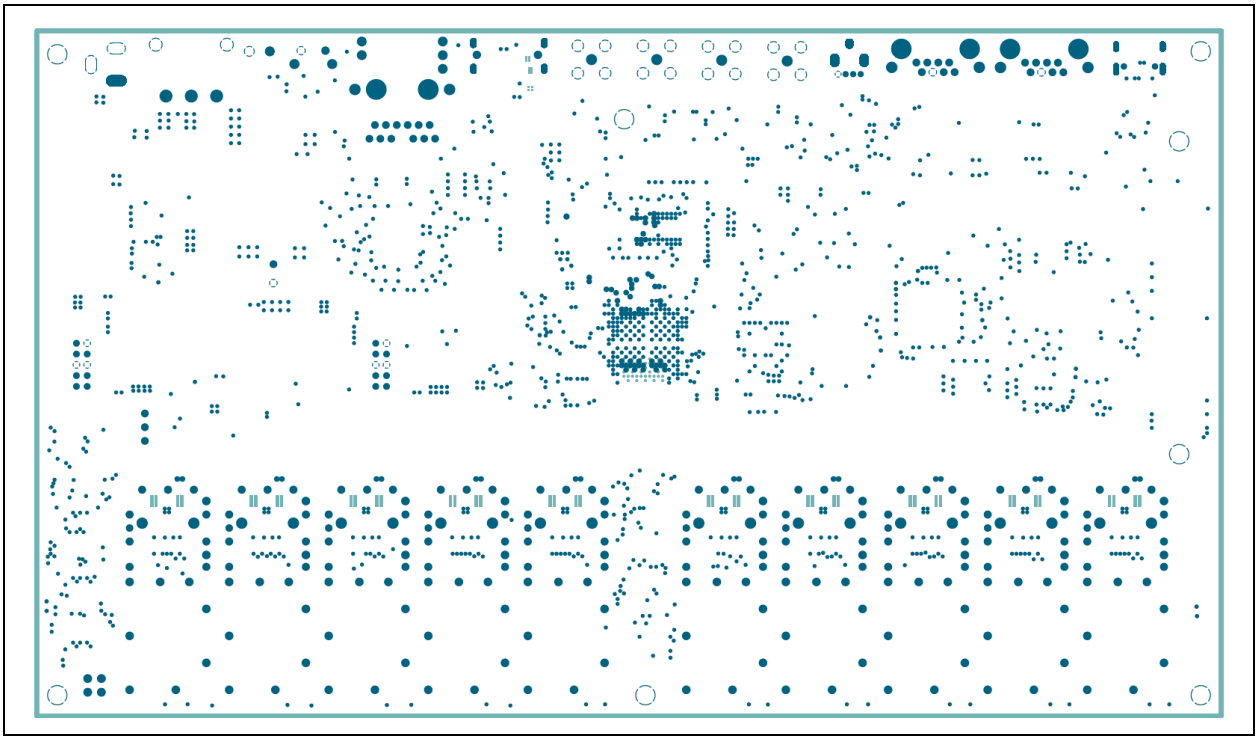
FIGURE A-2: LAYER 1 – TOP LAYER



The ground shield serves as a “quiet” ground for PHY copper media signals and SFP cages. It couples capacitively to the ground plane, providing a low-impedance return path for high-frequency noise.

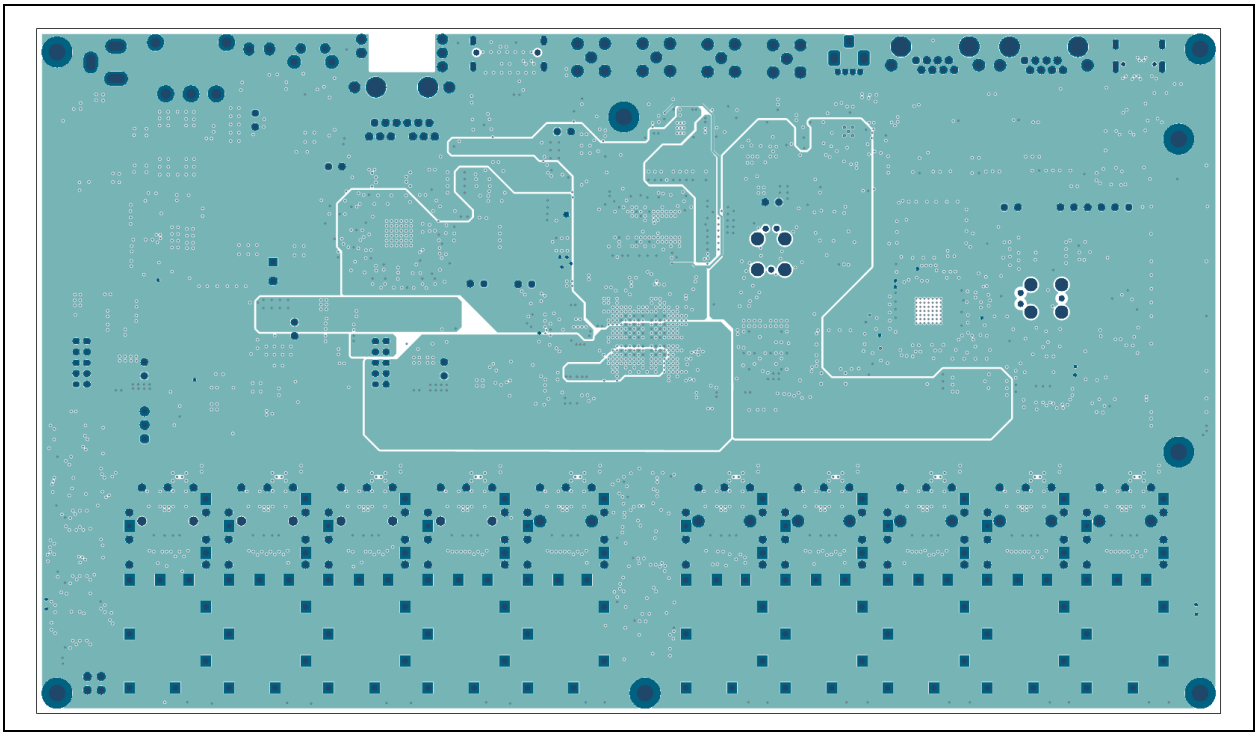
A.2.2 Layer 2 – Ground Plane 1

FIGURE A-3: INNER LAYER 2 – GROUND PLANE 1



A.2.3 Layer 3 – Power Plane 1

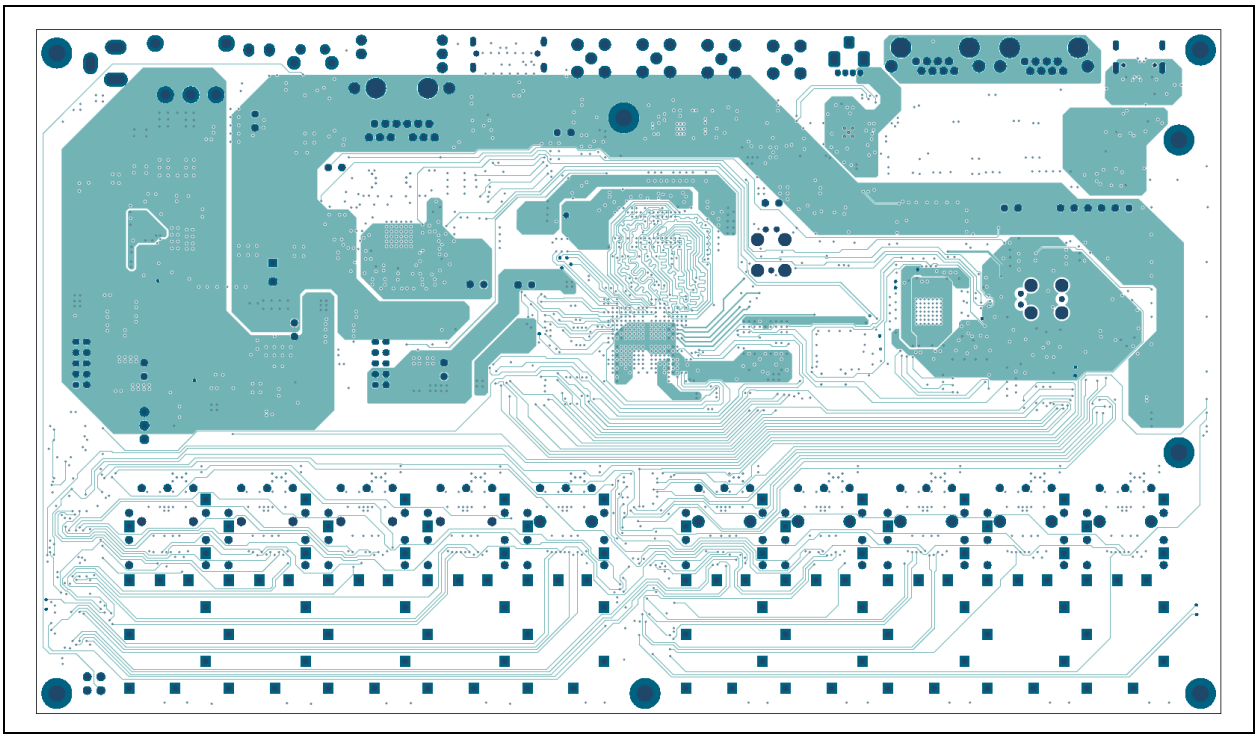
FIGURE A-4: INNER LAYER 3 – POWER PLANE 1



A.2.4 Layer 4 – Signal and Power Plane 2

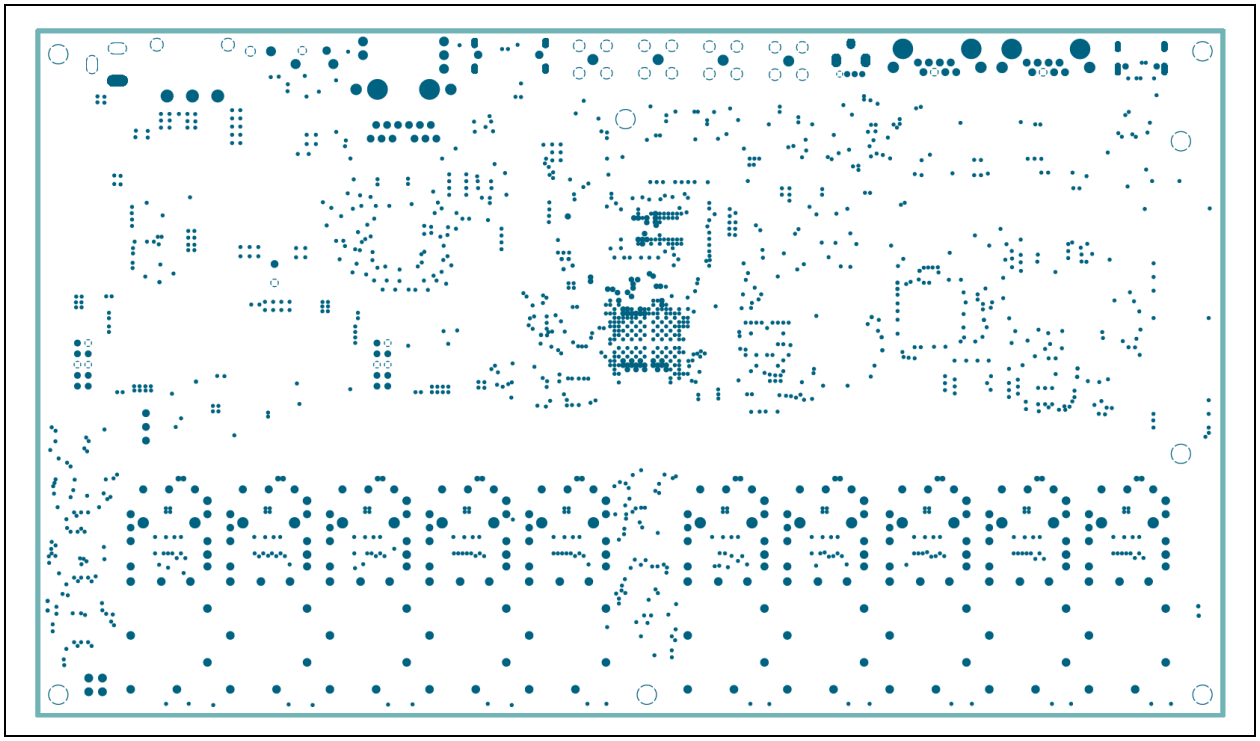
Various signal and power planes. See Figure A-5.

FIGURE A-5: INNER LAYER 4 – SIGNAL AND POWER PLANE 2



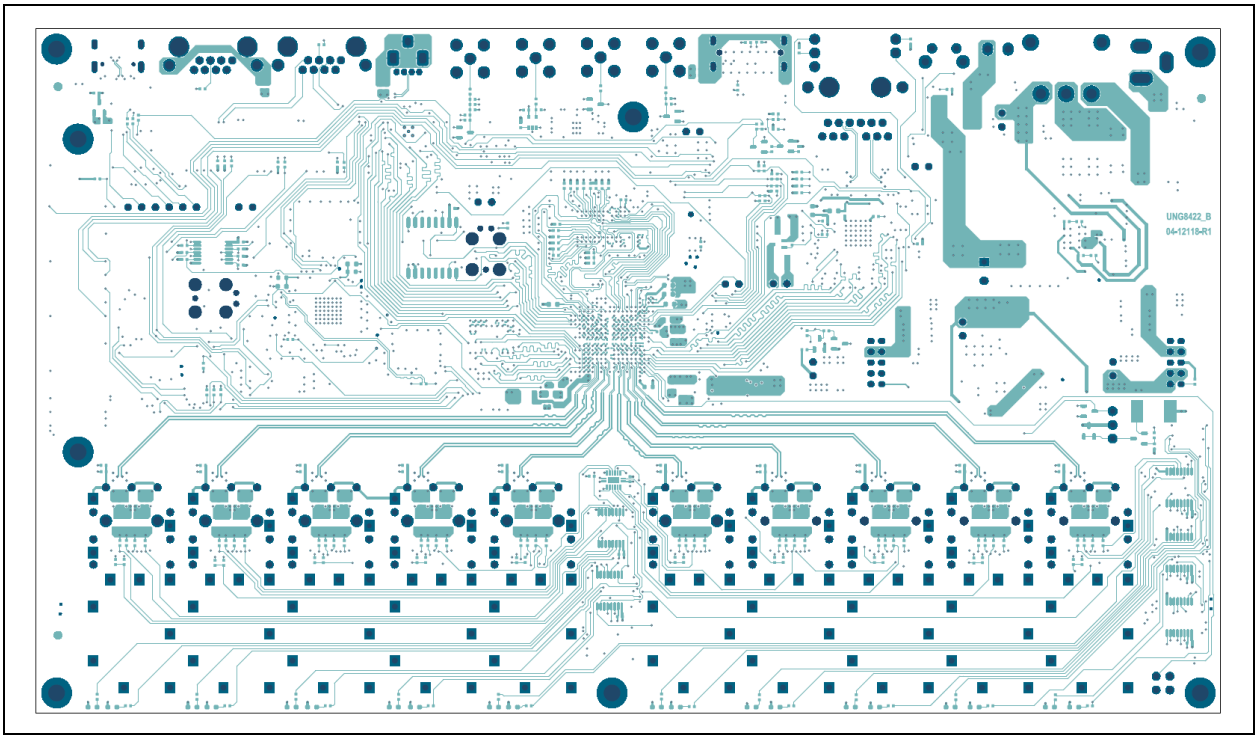
A.2.5 Layer 5 – Ground Plane 2

FIGURE A-6: INNER LAYER 5 – GROUND PLANE 2



A.2.6 Layer 6 – Bottom Layer

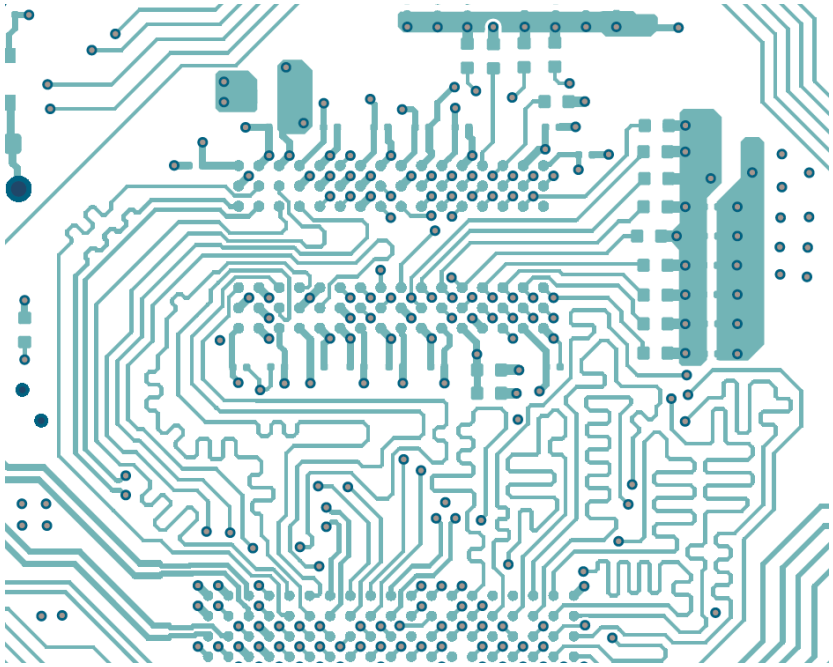
FIGURE A-7: LAYER 6 – BOTTOM LAYER



A.2.7 DDR4 Close-up on Top Layer

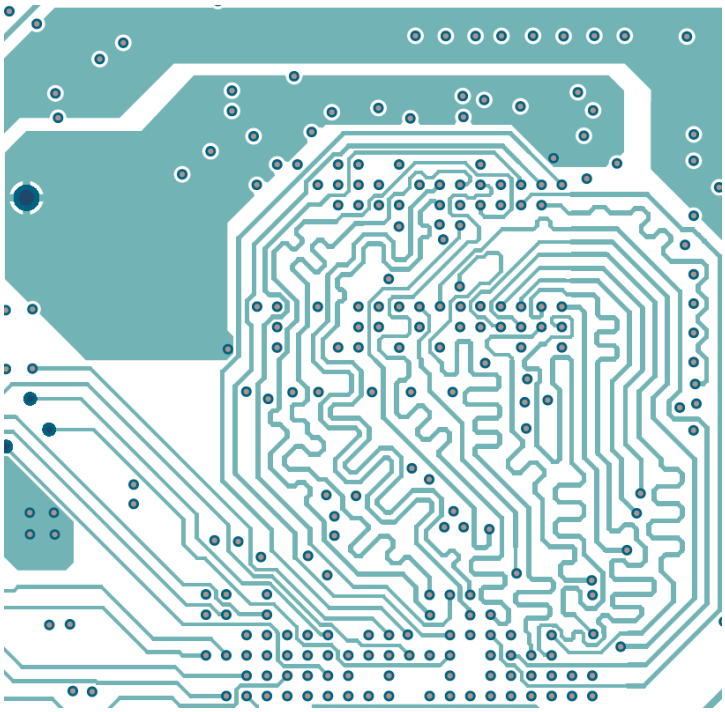
DDR4 in close-up to illustrate how the DDR length matching is acquired.

FIGURE A-8: DDR CLOSE-UP ON TOP LAYER



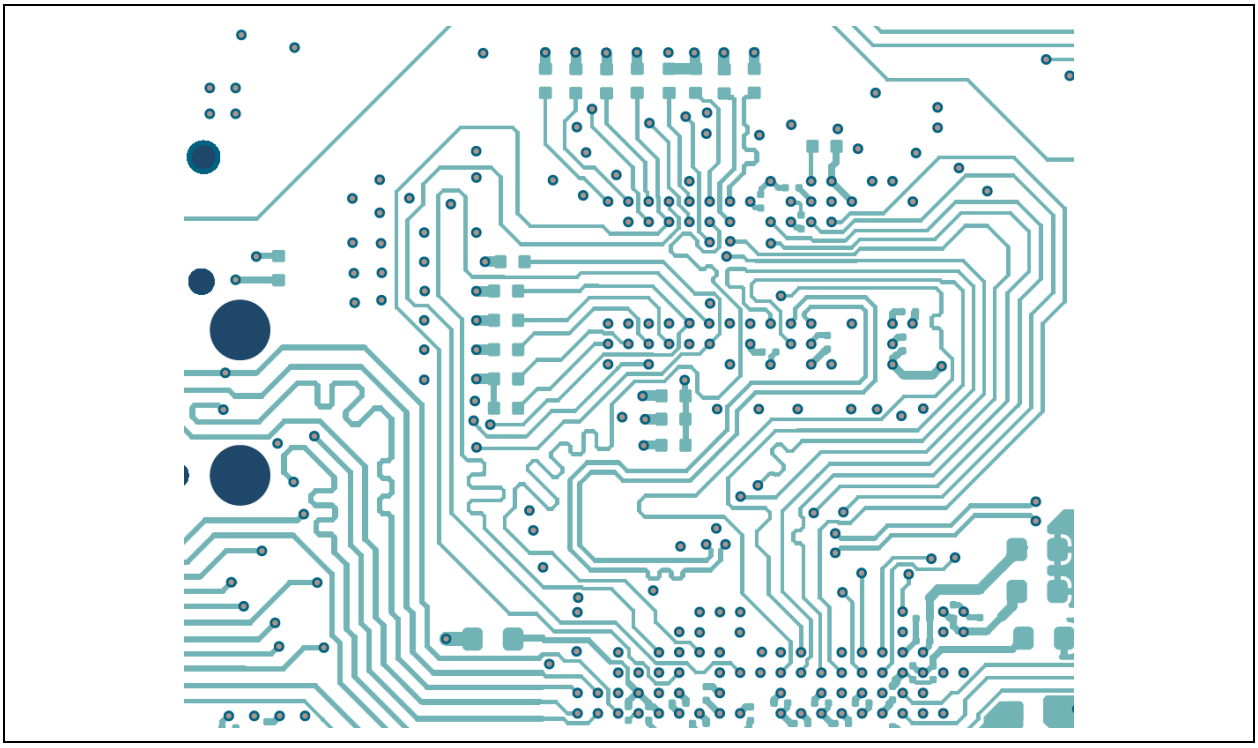
A.2.8 DDR4 Close-up on Signal and Power Plane 2

FIGURE A-9: DDR CLOSE-UP ON SIGNAL AND POWER PLANE 2



A.2.9 DDR4 Close-up on Bottom Layer

FIGURE A-10: DDR CLOSE-UP ON BOTTOM LAYER

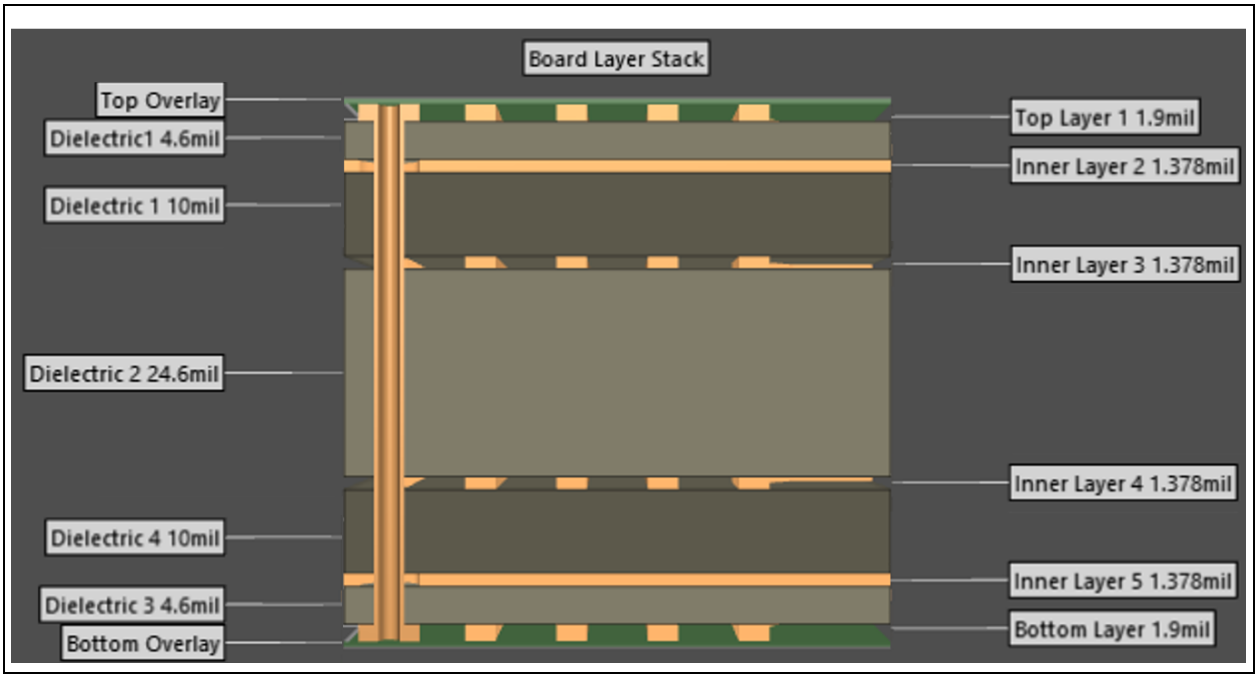


LAN969x package skew report is available upon request. Contact your Microchip representative.

A.3 PCB LAYER STACK-UP

The reference board is a six-layer impedance-controlled PCB. The stack-up is shown in Figure A-11.

FIGURE A-11: LAYER STACKED VISUALIZED



A.3.1 PCB Trace Widths, Clearance and Impedance

TABLE A-2: PCB TRACE WIDTHS, CLEARANCE AND IMPEDANCE

Layer	Name	Material	Thickness	Constant Dk/Df	Impedance Width/Spacing
—	Top Overlay	—	—	—	—
—	Top Solder	LPI Green	0.500 mil	3.5, 0.025	—
—	Top Finish	ENIG_3-6um Ni, 0.05-0.1um Au.	0.160 mil	—	—
1	Top Layer	CF-002	1.900 mil	—	50Ω SE: 7.5 mil 60Ω SE: 5.0 mil 85Ω Diff: 7/5 mil, 9/10 mil 100Ω Diff: 5/5.5, 6/9 mil
—	Dielectric1	PP-IT180A-2116_53	4.6 mil	4.08/0.01586	—
2	Ground Plane 1	CF-004	1.378 mil	—	—
—	Dielectric 1	CR-IT180A-2x2116	10.00 mil	4.38/0.0145	—
3	Power Plane 1	CF-004	1.378 mil	—	50Ω S: 10.5 mil 60Ω SE: 6.5 mil 100Ω Diff: 6.0/9.0 mil
—	Dielectric 2	PP-IT180A-3x7627	24.60 mil	4.75/0.01415	—
4	Signal and Power Plane 2	CF-004	1.378 mil	—	50Ω S: 10.5 mil 60Ω SE: 6.5 mil 100Ω Diff: 6.0/9.0 mil
—	Dielectric 4	CR-IT180A-2x2116	10.00 mil	4.38/0.0145	—
5	Ground Plane 2	CF-004	1.378mil	—	—
—	Dielectric 3	PP-IT180A-2116_53	4.60 mil	4.08/0.01586	—

TABLE A-2: PCB TRACE WIDTHS, CLEARANCE AND IMPEDANCE (CONTINUED)

Layer	Name	Material	Thickness	Constant Dk/Df	Impedance Width/Spacing
6	Bottom Layer	CF-002	1.90 mil	—	50Ω SE: 7.5 mil 60Ω SE: 5.0 mil 85Ω Diff: 7/5 mil, 9/10 mil 100Ω Diff: 5/5.5, 6/9 mil
—	Bottom Finish	ENIG_3-6um Ni, 0.05-0.1um Au.	0.160 mil	—	—
—	Bottom Solder	LPI Green	0.500 mil	3.5, 0.025	—
—	Bottom Overlay	—	—	—	—
—	Board Thickness	(1.64 mm)	64.43 mil	—	—

TABLE A-3: NET IMPEDANCE AND LENGTH MATCHING

Net Group	Type	Impedance	Length Matching	Tolerance (mm)	Max. Vias	Via Type	Layer	Note
Clock	SE	50Ω	None	—	4	All	All	—
SI	SE	50Ω	None	—	4	All	All	Daisy-chain
DDR_CMD_LANE	SE/DIFF	60Ω	Within lane	1	2	All	All	Note 2
DDR_DQ_LANE0	SE/DIFF	60Ω	Within lane	1	2	All	All	Note 2
DDR_DQ_LANE1	SE/DIFF	60Ω	Within lane	1	2	All	All	Note 2
USB	DIFF	85Ω	P/N only	1	2	All	All	—
DiffClock	DIFF	100Ω	P/N only	1	4	All	All	—
DiffClockCrit	DIFF	100Ω	P/N only	1	2	All	All	Note 5
SerDes10G	DIFF	100Ω	P/N only	0	2	—	Outer	Note 1
Sense	Analog	—	—	—	—	All	All	—
Power	Power	—	—	—	—	—	—	—
Static	SE	—	—	—	—	—	—	Note 3
Unspecified	SE	60Ω	—	—	—	—	All	Note 4

Note 1: Differential signal on outer layers

2: DDR SE impedance 60Ω between devices

3: No impedance => 4 mil trace on any layer

4: Any unspecified nets should be routed as 60Ω.

5: Critical clock nets: CLK156 - route with extra clearance.

NOTES: