

FCD620N60ZF

N-Channel SuperFET® II FRFET® MOSFET 600 V, 7.3 A, 620 mΩ

Features

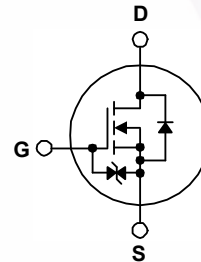
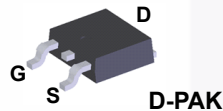
- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 528\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 20\text{ nC}$)
- Low Effective output Capacitance (Typ. $C_{oss(eff.)} = 71\text{ pF}$)
- 100% Avalanche Tested
- ESD Improved Capacity
- RoHS Compliant

Applications

- LCD / LED / PDP TV and Monitor Lighting
- Solar Invertor / AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD620N60ZF	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	7.3
		- Continuous ($T_C = 100^\circ\text{C}$)	4.6
I_{DM}	Drain Current	- Pulsed (Note 1)	21.9
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	135
I_{AR}	Avalanche Current	(Note 1)	1.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	0.89
dv/dt	MOSFET dv/dt		100
	Peak Diode Recovery dv/dt	(Note 3)	20
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	89
		- Derate Above 25°C	0.71
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCD620N60ZF	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD620N60ZF	FCD620N60ZF	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.6	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 7.3\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	5	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	20	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.6\text{ A}$	-	0.528	0.62	Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	855	1135	pF
C_{oss}	Output Capacitance		-	625	830	pF
C_{rss}	Reverse Transfer Capacitance		-	30	45	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	16	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	71	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 3.6\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	20	36	nC
Q_{gs}	Gate to Source Gate Charge		-	4.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7.7	-	nC
ESR	Equivalent Series Resistance		$f = 1\text{ MHz}$	-	2.7	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 3.6\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$ (Note 4)	-	15	40	ns
t_r	Turn-On Rise Time		-	7	24	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	80	ns
t_f	Turn-Off Fall Time		-	10	30	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	7.3	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	21.9	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 3.6\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 3.6\text{ A}$	-	84	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	0.325	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 1.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 3.6\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

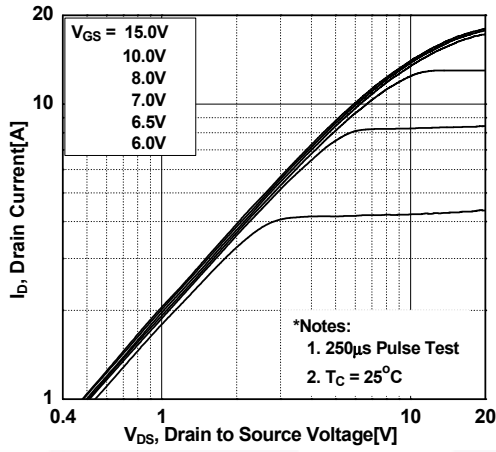


Figure 2. Transfer Characteristics

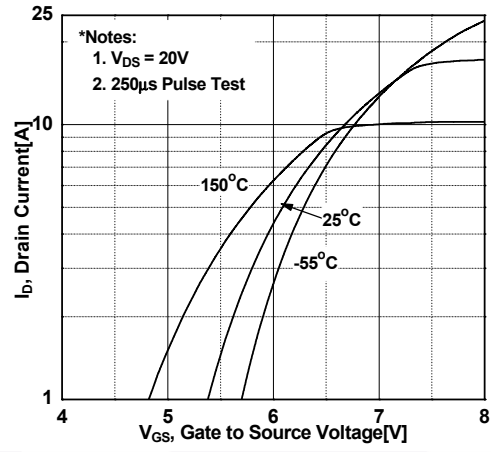


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

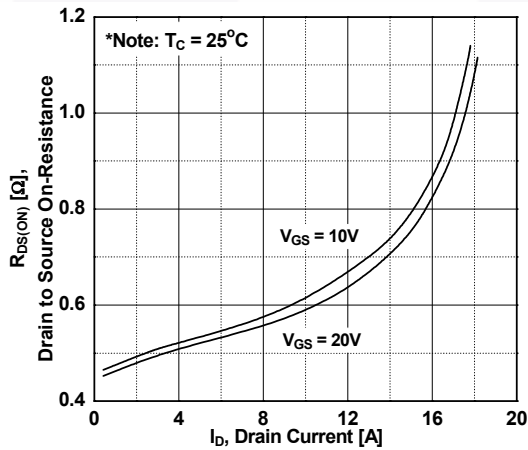


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

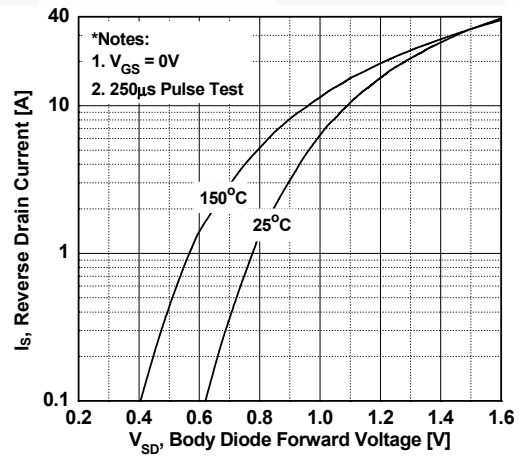


Figure 5. Capacitance Characteristics

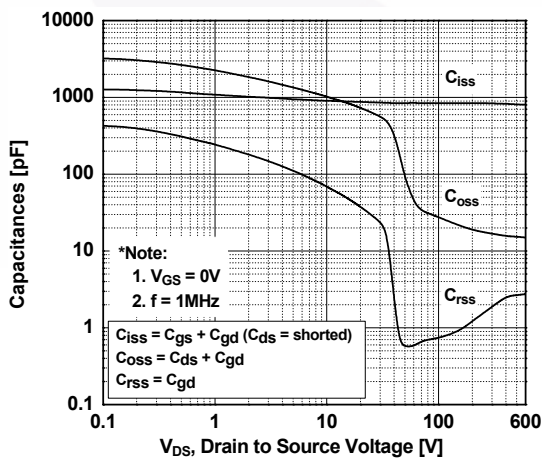
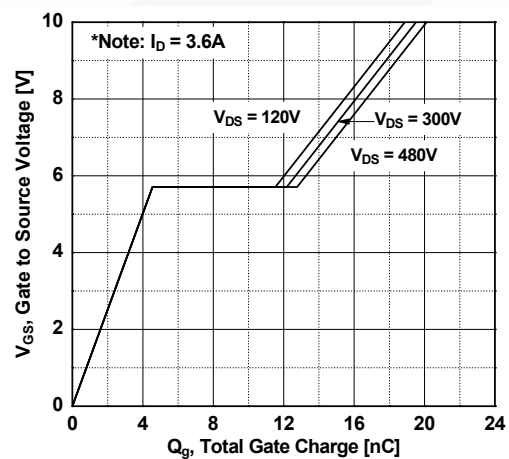


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

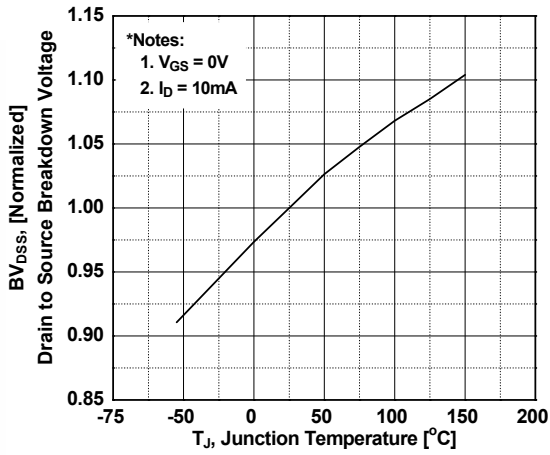


Figure 8. On-Resistance Variation vs. Temperature

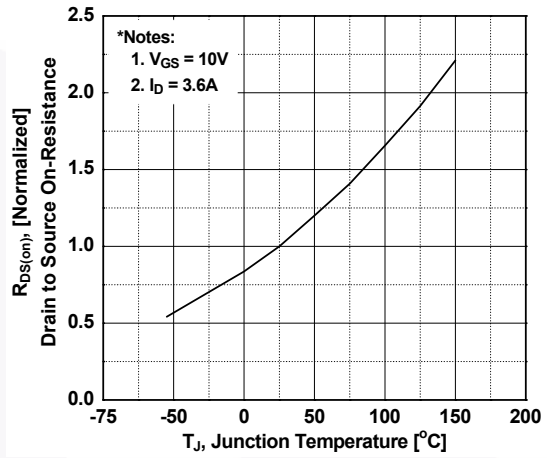


Figure 9. Maximum Safe Operating Area

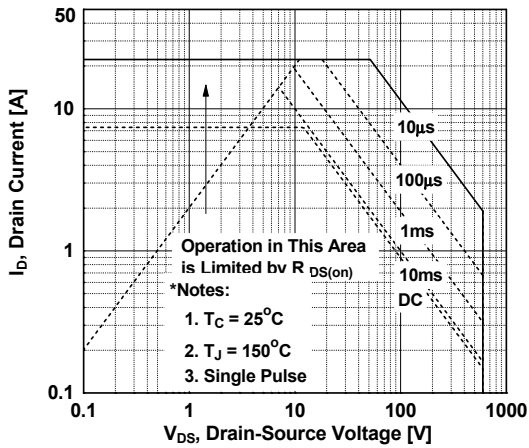


Figure 10. Maximum Drain Current vs. Case Temperature

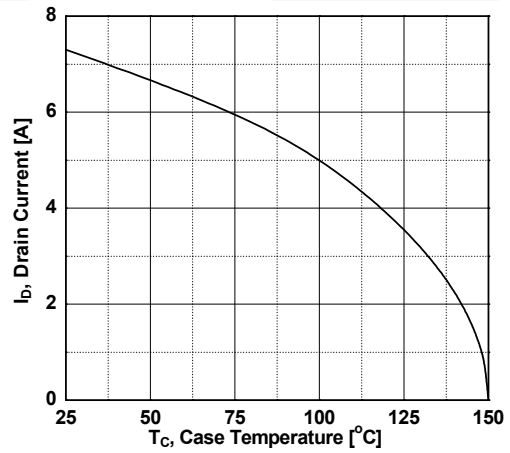
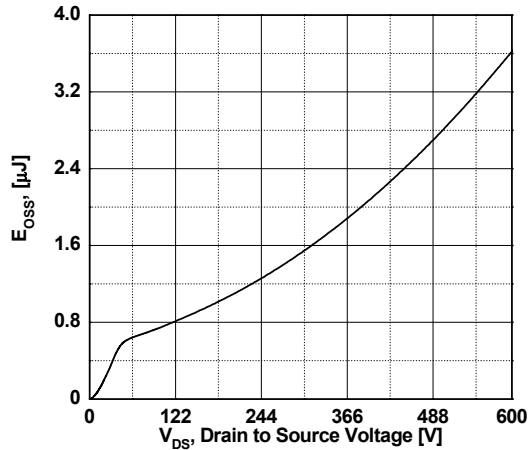
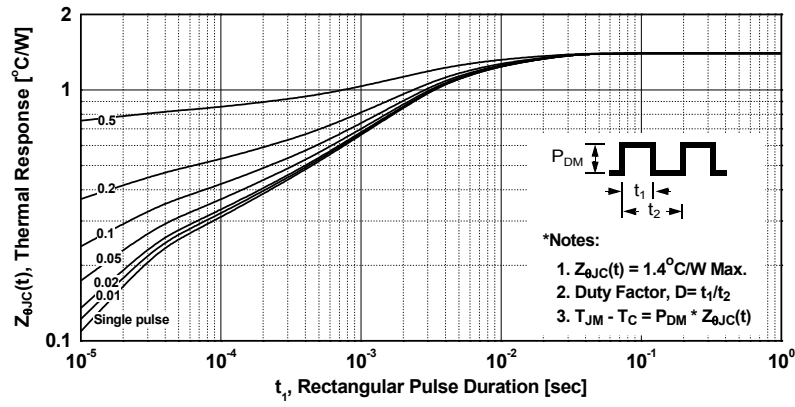


Figure 11. E_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



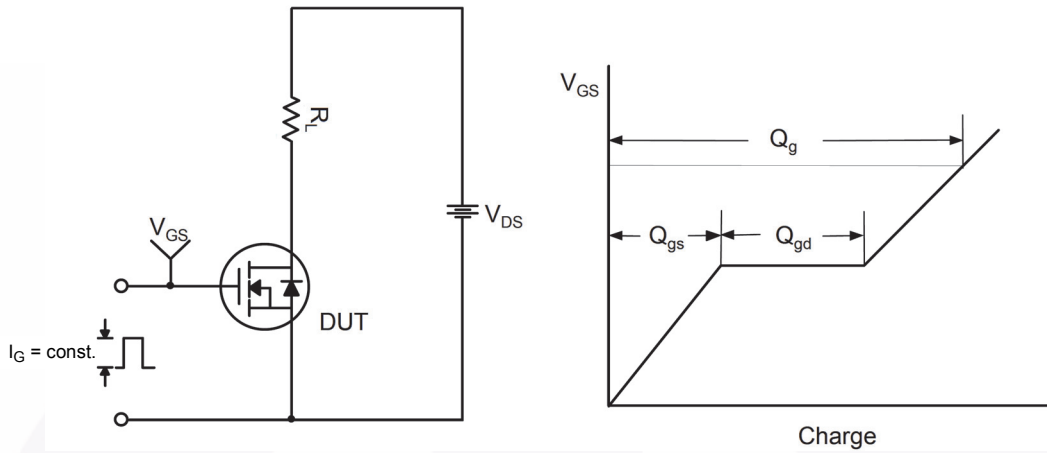


Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms

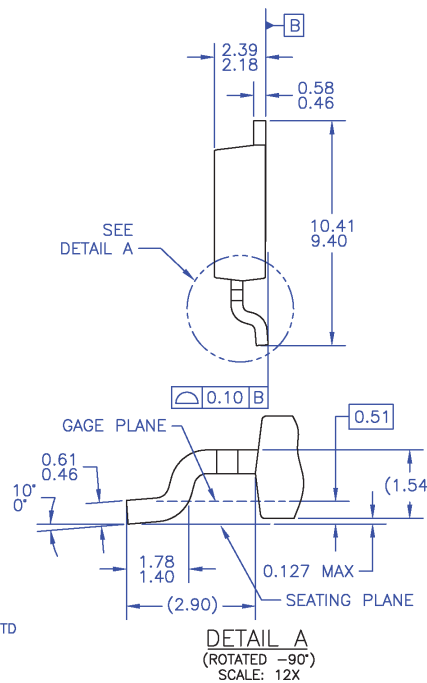
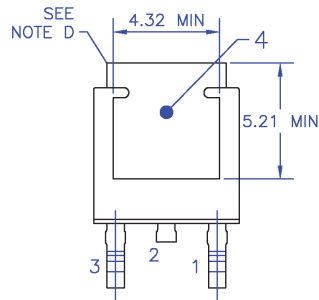
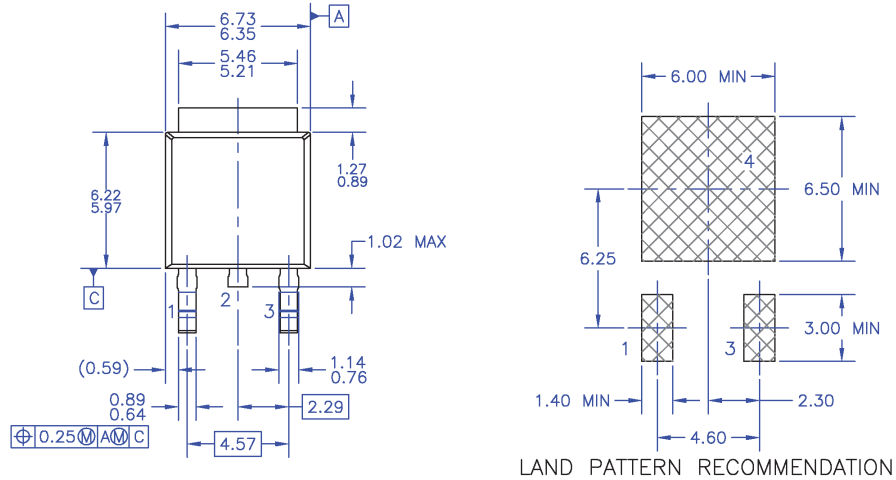


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Figure 17. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT252-003

