Datasheet

DS000496

AS7225

Calibrated XYZ Chromatic Smart Lighting Director

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Content Guide

1 General Description

The AS7225 Smart Lighting Director incorporates an embedded digital tri-stimulus chromatic calibrated for life nano-optic sensor providing direct CIE1931 XYZ and CIE 1976 u'v' coordinate mapping. Adaptive algorithmic support enables a companion microprocessor to implement closed-loop, autonomous adjustment of variable CCT and daylight responsive LED lamps and luminaires. The AS7225 arrives pre-calibrated, and is designed for rapid integration into white-tunable and daylight responsive luminaire designs, delivering directives to the local microprocessor via an industry-standard I²C bus or UART interface.

An additional on-chip I²C master provides native support for select **ams** sensors, such as the TSL2572 for combining in-looking CCT tunable director functions with outward-looking ambient light sensing and daylighting control. The AS7225's silicon via nano-optic deposited interference filters deliver high-stability over both time and temperature. The Director's integrated intelligence enables ams factory CCT calibration, which mitigates chip to chip variation. By combining this factory calibration with a supported luminaire design-level "application matrix", an end luminaire design can often eliminate the need for light-by-light calibration while delivering lifetime color control. With such a system calibration, accuracies within 2-4 Macadam steps are possible. The LGA package includes a built in aperture to control light entering the sensor array. No additional optics are required.

1.1 Key Benefits & Features

The benefits and features of AS7225, Calibrated XYZ Chromatic Smart Lighting Director, are listed below:

Figure 1:
Added Value of Using AS7225

Benefits	Features
Provides accurate external host MCU supervision of variable CCT and spectrally tunable lighting	Integrated intelligence with XYZ tri-stimulus color sensing for direct translation to CIE 1931 standard observer color map
Uses accurate XYZ sensed data to provide a host MCU, with its own PWMs, simple to use directives for closed loop tuned LED lighting	Automatically directs external warm and cool white PWM controlled LED strings for chromatic LED luminaire tuning. Also directs dimming (combined with PWM color tuning)
Automatic spectral and lumen maintenance over temperature and time	Supports autonomous color point and lumen output adjustment resulting in automatic spectral and lumen maintenance
Provides direct register or AT command based access to closed loop tuning directives	I²C slave digital or UART Interface

Benefits	Features
Used to interface other **ams** sensors with native support by the AS7225 (e.g. TSL2572 for adding Daylighting operation)	I²C master digital or UART interface
Rapid luminaire integration	Simple register-based or AT commands to control and configure key light-tuning supervisory and IoT sensor expansion functions
Complete data on lighting environment	Readable registers or AT commands for CIE 1931 and 1975 color-point coordinates, CCT, duv and lux
Calibrated sensing with minimal drift over time and temperature	Chromatic white color realized by silicon interference filters
Small package, with build in aperture	20-pin LGA package 4.5mm x 4.7mm x 2.5mm, with integrated aperture, -40°C to 85°C

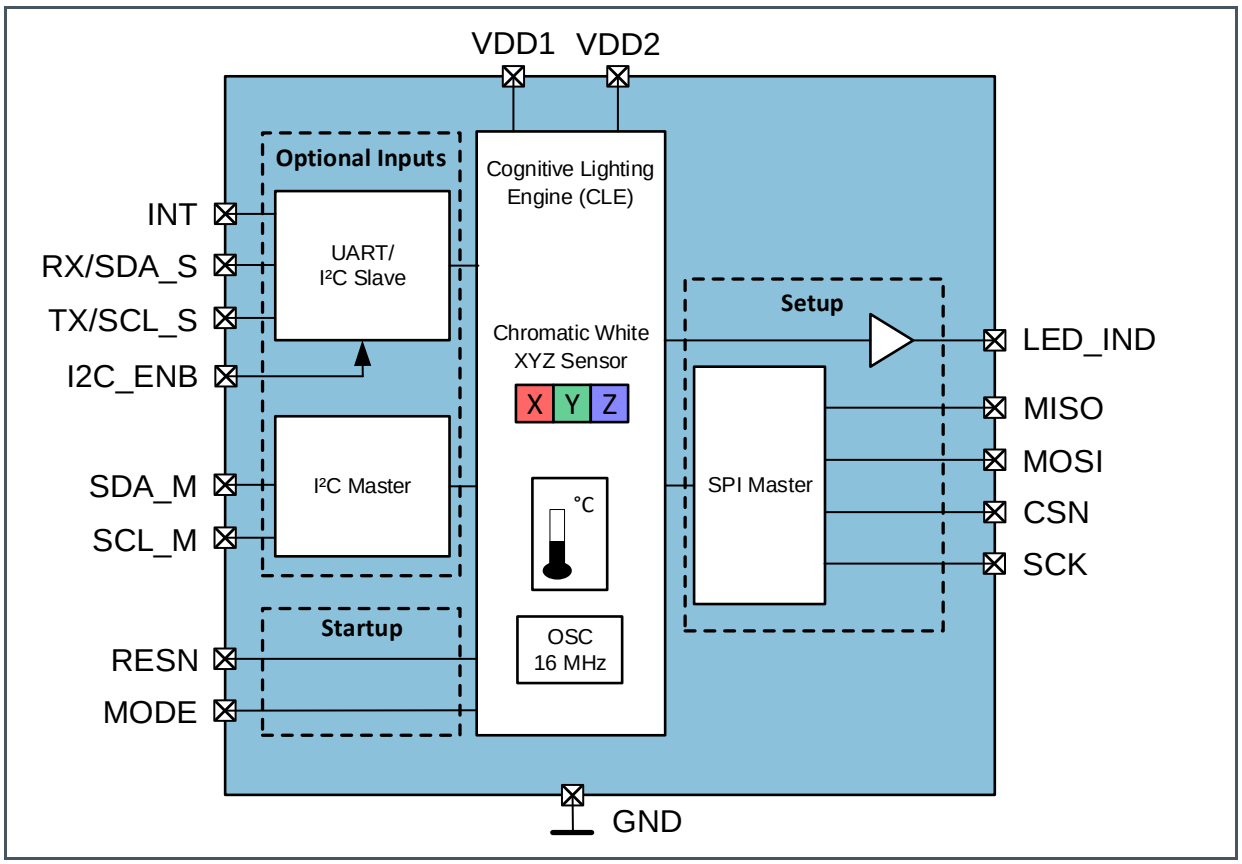
1.2 Applications

- Intelligent, networked solid state lighting director for variable CCT chromatic tuning luminaires systems
- Integrated smart lighting control of variable CCT white lighting solutions
- Luminaires intended to meet California Title 24 daylighting requirements
- Commercial, retail, and residential white/color changing LED lighting systems
- Networked lighting systems with IoT sensor expandability

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS7225



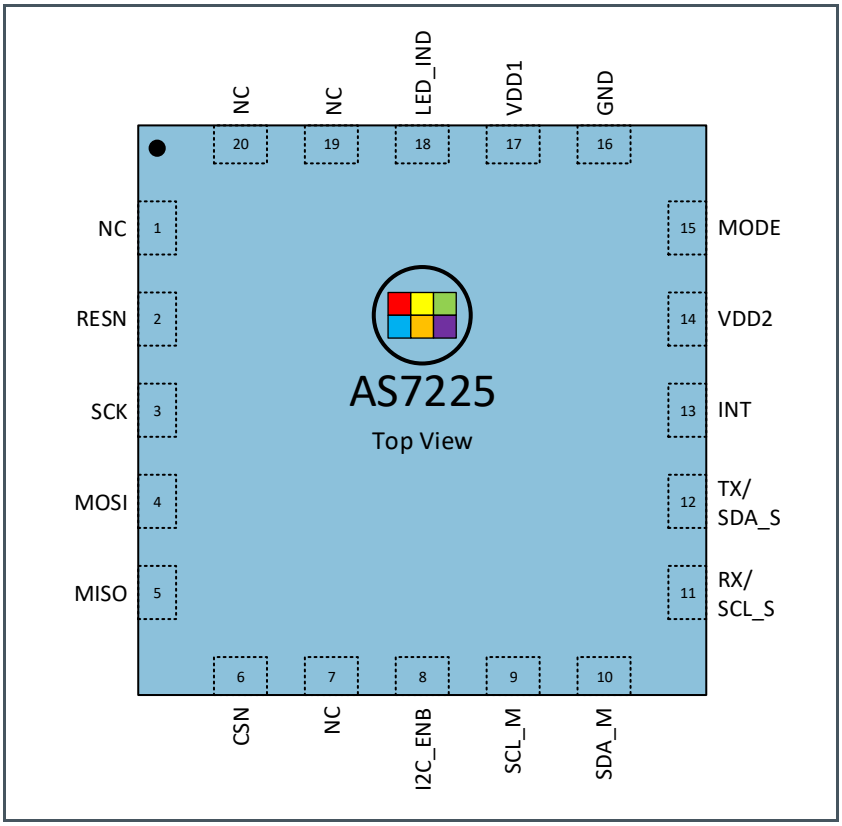
2 Ordering Information

Ordering Code	Description	Package	Marking	Delivery Form	Delivery Quantity
AS7225 – BLGT	Calibrated XYZ Chromatic Smart Lighting Director – Standard Reel	20-Pin LGA	AS7225	13-inch Tape & Reel	2000 pcs/reel
AS7225 – BLGM	Calibrated XYZ Chromatic Smart Lighting Director – Mini Reel	20-Pin LGA	AS7225	7-inch Mini Tape & Reel	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Diagram for AS7225 (Top View)



3.2 Pin Description

Figure 4:
Pin Description of AS7225

Pin Number	Pin Name	Pin Type(1)	Description
1	NC	-	Not connected
2	RESN	DI	Reset pin, active low
3	SCK	DI	SPI serial clock
4	MOSI	DO	SPI MOSI

Pin Number	Pin Name	Pin Type(1)	Description
5	MISO	DI	SPI MISO
6	CSN	DO	Chip select for the required external flash memory, active low
7	NC	-	Not connected
8	I2C_ENB	DI	Select UART (Low) or I2C (High) Operation
9	SCL_M	DI/O	I^2C master clock pin
10	SDA_M	DI/O	I2C master data pin
11	RX/SCL_S	DI/O	RX (UART) or SCL_S (I2C Slave) Depending on I2C_ENB
12	TX/SDA_S	DI/O	TX (UART) or SDA_S (I2C Slave) Depending on I2C_ENB
13	INT	DO	Interrupt, active low
14	VDD2	P	Voltage supply
15	MODE	DI	Mode selection pin. Set to Mode=0 via 100Ohm resistor. Other Modes are reserved.
16	GND	P	Ground
17	VDD1	P	Voltage supply
18	LED_IND	AO	LED Driver output for Indicator LED, current sink.
19	NC	-	Not connected
20	NC	-	Not connected

(1) Explanation of abbreviations:

DI	Digital Input
DO	Digital Output
DI/O	Digital In Out
AO	Analog out
AI	Analog In
P	Power pin

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high-energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long-term optical performance. All voltages with respect to GND. Device parameters are guaranteed at VDD = 3.3V and TAMB = 25°C unless otherwise noted.

Figure 5
Absolute Maximum Ratings of AS7225

Symbol	Parameter	Min	Typ	Max	Unit	Comments
			Electrical Parameters			
V_{DD1_MAX}	Supply Voltage VDD1	-0.3		5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply Voltage VDD2	-0.3		5	V	Pin VDD2 to GND
V_{DD_IO}	Input/Output Pin Voltage	-0.3		VDD + 0.3	V	Low Voltage pins to GND
I_{SCR}	Input Current (latch-up immunity)		± 100		mA	JESD78D
			Electrostatic Discharge			
ESD_{HBM}	Electrostatic Discharge HBM		± 1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM		± 500		V	JEDEC JESD22-C101F Oct 2013
			Temperature Ranges and Storage Conditions			
T_{STRG}	Storage Temperature Range	-40		85	°C	
T_{BODY}	Package Body Temperature			260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5		85	%	
MSL	Moisture Sensitivity Level		3			Represents a 168-hour max. floor lifetime.
			Bump Temperature (soldering)			
T_{PEAK} (1)	Peak Temperature	235		245	°C	Solder Profile

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, TAMB = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. If VDD1 and VDD2 must be sourced by the same 2.97V to 3.6V supply. All voltages with respect to GND.

Figure 6:
Electrical Characteristics of AS7225

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		General Operating Conditions				
VDD1 / VDD2	Voltage Operating Supply		2.97	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
		Internal RC Oscillator				
F_{osc}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER}[1]	Jitter	@25°C			1.2	ns
		Temperature Sensor				
D_{Temp}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
		Indicator LED				
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	V_{DS} of current sink	0.3		VDD	V
		Digital Inputs and Outputs				
I_{IH}, I_{IL}	Logic Input Current	V_{in}=0V or VDD	-1		1	µA
V_{IH}	CMOS Logic High Input		0.7*VDD		VDD	V

[1] Guaranteed, not production tested

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	CMOS Logic Low Input		0		0.3*VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE}	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL}	Current Fall Time	C(Pad)=30pF			5(1)	ns

1 Guaranteed, not production tested

6 Optical Characteristics

The AS7225 contains an integrated tristimulus sensing element designed to meet the XYZ standard observer response compliant with the CIE 1931 standard. The device contains a 16-bit integrating analog-to-digital converter, which integrates current from the photodiodes. To ensure the integrity of the data, upon completion of an integration cycle, results are transferred to double-buffered registers.

Standard observer tristimulus (XYZ) interference filters are applied to the Calibrated XYZ Chromatic Smart Lighting Director optical channels as part of the CMOS process. This unique process enables filter responses that mimic the human eye and is extremely stable over both operating temperature and time. This in turn allows lifetime correlated color temperature (CCT) calibration to be performed as part of the manufacturing process. Calibration is accomplished using standard white LEDs at a variety of CCTs to deliver high accuracy and eliminate the need for light-by-light calibration in most designs. Note the AS7225 LGA package contains an internal aperture that provides a package field of view (PFOV) of ± 20.5°. External optics can be used as needed to expand or reduce this built in PFOV.

Please note that for the data readout the maximum value is limited by the ADC. The Saturation value is 65535 for all sensor data in read cycle.

Figure 7:
AS7225 Optical Characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Color_m[2]	Color Measurement Accuracy	White Light CCT=2700K, 3500K, 4500K and 5700K		0.002		du'v'
Z_count	Z Channel Count Accuracy	White light CCT = 5700K	3.375	4.5	5.625	counts/ (µW/cm²)

(1) Typical values at Lux ≥50, integration time = 400.4ms. Gain = 1x, T_{AMB} = 25°C
(2) Calibration and measurements are made using diffused light

Figure 8:
Normalized Spectral Responsivity

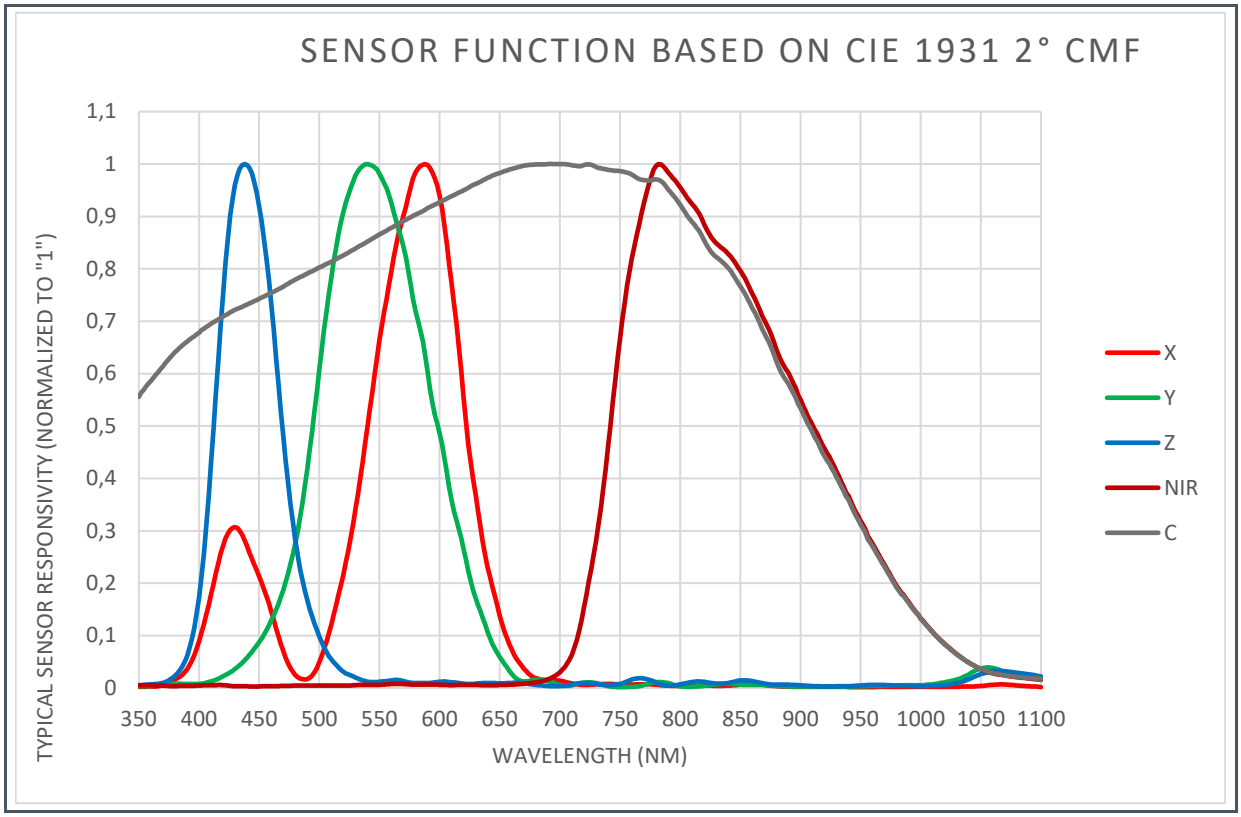


Figure 9:
Typical Spectral Responsivity

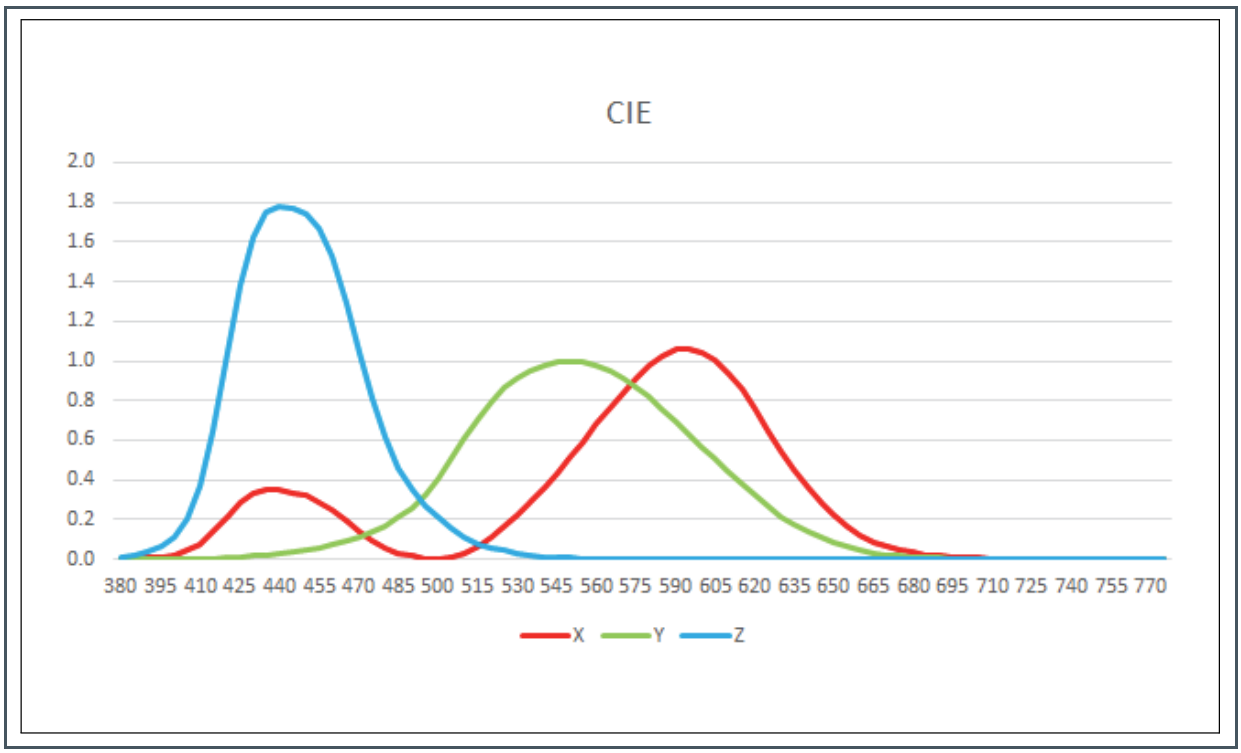
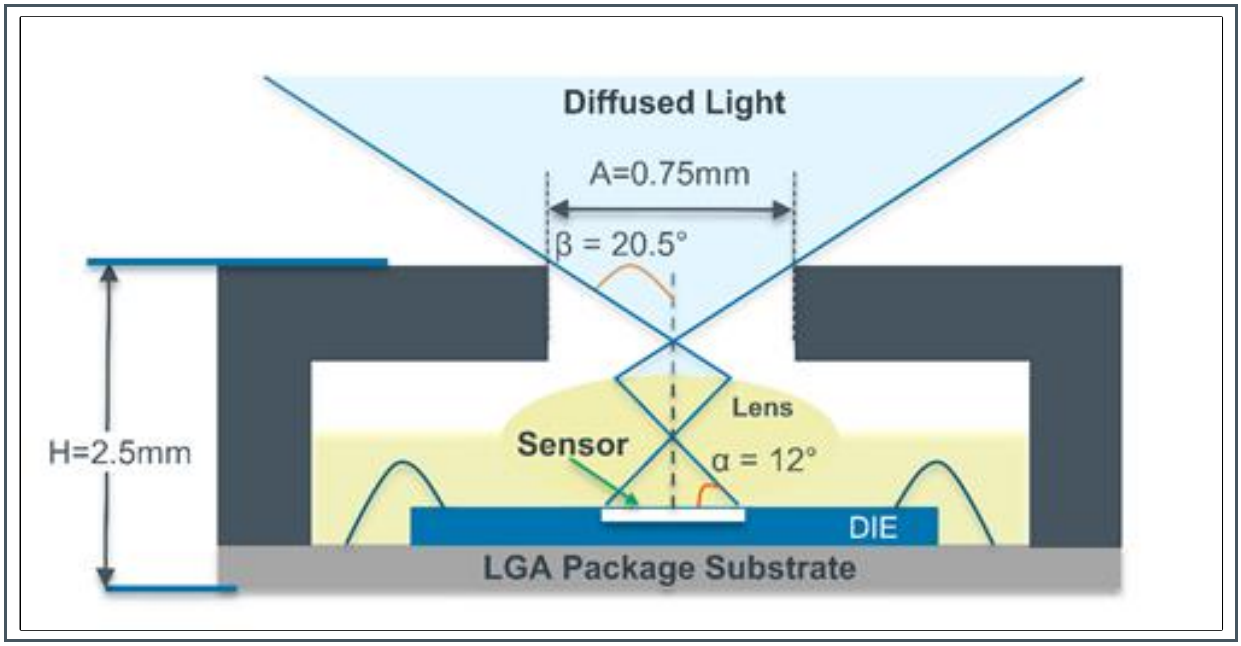


Figure 10:
AS7225 LGA Average Field of View

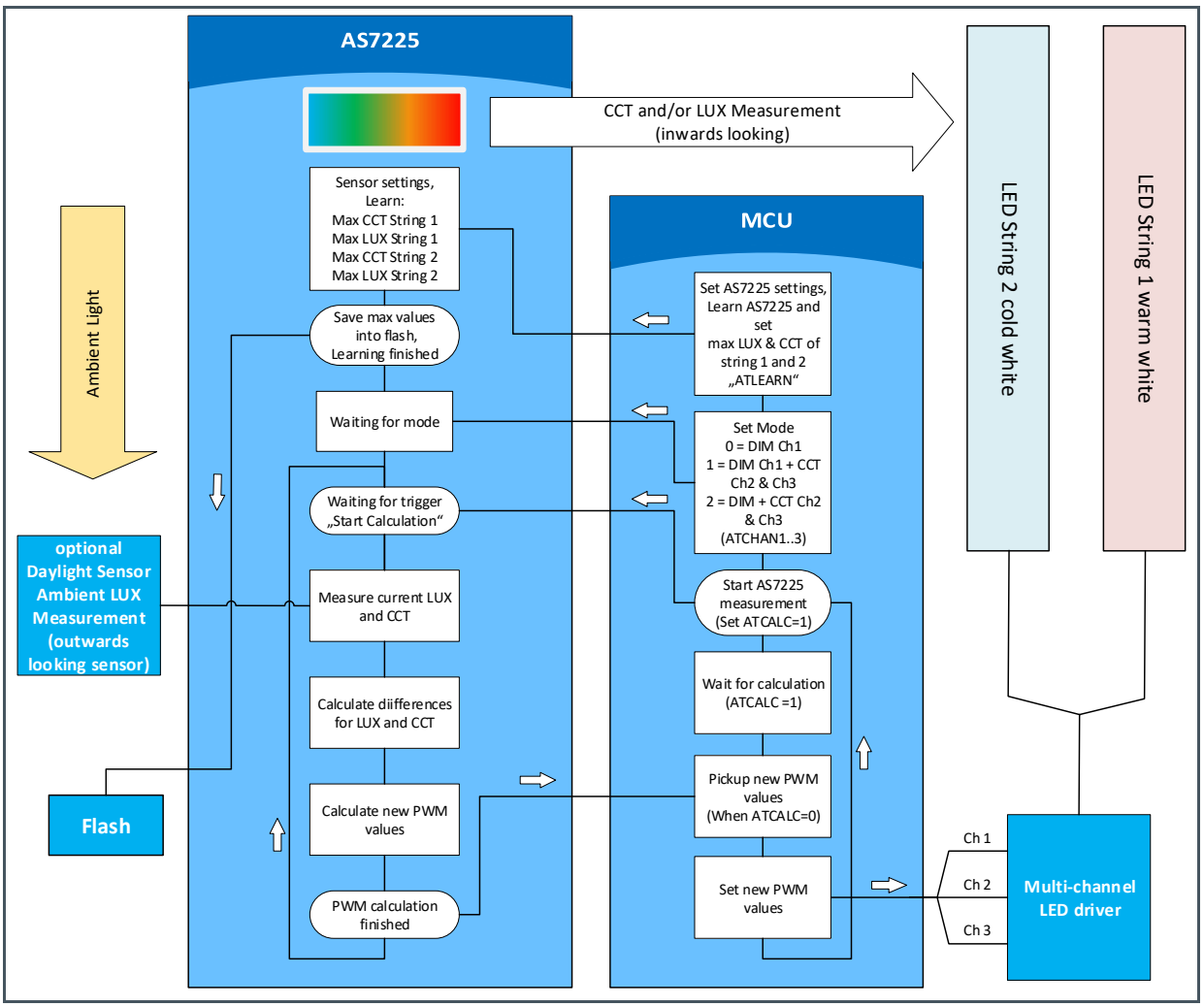


7 Functional Description

7.1 Calibrated XYZ Chromatic Smart Lighting Director – Overview

By sensing a sample of the mixed warm and cool CCTs as either a reflection from the diffuser or other light-guide/optical light gather technique, the AS7225 serves as a calibrated chromatic smart lighting director for a companion host MCU. By usage of a diffuser or a coupled light fiber, the AS7225 gets a homogenous mixed light. This prevents unwished scattered light impacts and provides high level calculated white color tuning control loop information for external LED channel PWM or current controls via I2C registers or UART commands. Director operation also provides selectable dimming information for either PWM-based or current-based luminaire dimming designs.

Figure 11:
AS7225 workflow abstract



The AS7225 initial setup and ongoing parameter storage is automatically done by software within the required external serial Flash memory, via SPI bus. Only ams-verified models of Flash devices can be supported. A subset of supported devices is noted in the UART Command Interface section of this document, which also provides a reference to the current list of supported Flash memory devices. For the Flash memory, overview please refer to Figure 83:
Flash Memory Overview. A SPI Flash device is a required operating companion to the AS7225. Using other devices can cause communication issues and may not be compatible. Flash timing is provided in Figure 81 and Figure 82.

A binary image software configuration tool is available from ams to allow the luminaire, lamp or driver manufacturer to create their own “factory default” conditions that will be integrated with the ams–supplied initial binary image to create a ready-to-program default Flash image. The configuration tool is available from https://download.ams.com/ (see Smart Lighting Command Interface section).

XYZ white color point measurement is accomplished via nano-optic interference filters which deliver a CIE standard-observer type spectral response. As an extension of the CMOS processing of the device, the filters are extremely stable over time and temperature. To minimize off-angle light exposure and ensure accuracy, the AS7225 LGA package contains an internal aperture that limits the sensor field of view (PFOV) of ± 20.5°, as shown in the Figure 1 above. External optics can be used as needed to expand or reduce this built in PFOV.

For daylight operation, the AS7225 can be used two ways. As a standalone device pointing out of the luminaire, or if pointing inward for white color, it can support daylighting operation by using an I^2C master connected **ams** TSL2572 for ambient light sensing. In either case, the AS7225 is the daylighting engine and directs the external MCU.

Overall AS7225 timing generation uses an on chip 16MHz temperature compensated oscillator for master clock timing.

7.2 Inputs

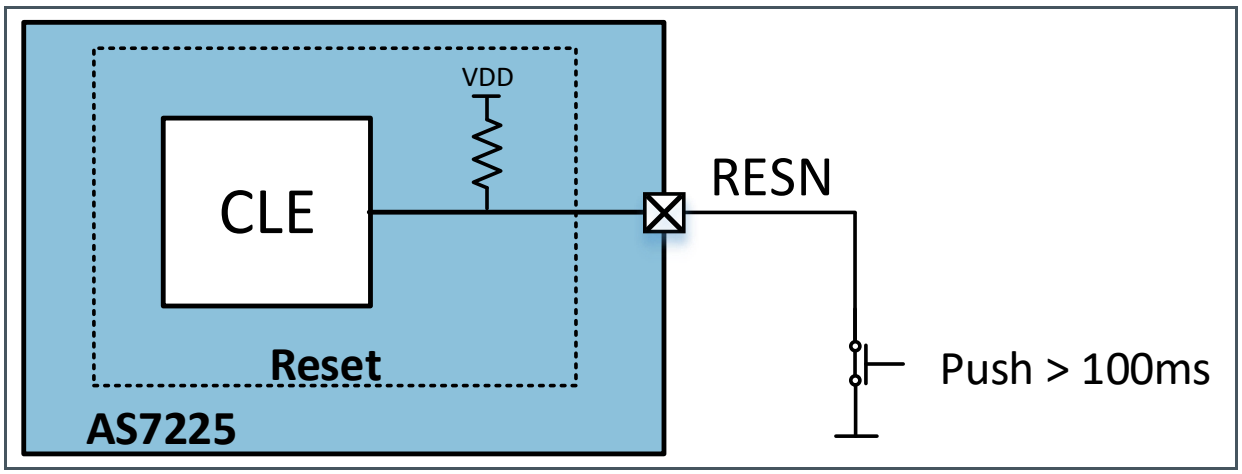
7.2.1 Mode Pin

The AS7225 MODE pin must be connected to ground (GND) via a 100Ω resistor (1%) to set the AS7225 mode of operation. All other MODEs (using other resistor values) are reserved.

7.2.2 Reset

Pulling down the RESN pin for longer than 100ms resets the AS7225.

Figure 12:
Reset Circuit



7.3 Outputs

7.3.1 Indicator LED

An LED, when connected to pin LED_IND, is used to indicate on state and programming progress of the device. During companion SPI Flash programming the AS7225 indicator LED is on. When programming is finished the indicator LED turns off. In case of an error while programming the LED starts a blinking operation. The LED_IND pin is set for 1mA LED operation by the AS7225 factory firmware, and is not under user control. The indicator LED can be enabled or disabled by using the ATLED0 command or the LED_CONFIG register (0x07).

Refer to the separate ams document for a complete description of AS7225 Firmware Update Methodology.

7.3.2 Interrupt Operation

Register bits DATA_RDY give information about finished integration and calculation. The PWM_RDY and the INT pin inform when new calculated PWM dimming percent values are available for the external MCU. If the interrupt register bit for either are enabled (RDY_INT = 1, PWM_INT =1) then when either of these activities become active, indicating available data, the INT pin is pulled low in addition to setting the ready register bit(s). The INT Line is released when the appropriate control register (CONV_Control and/or DIR_ Control) is read. DATA_RDY is cleared to 0 when any of the sensor registers X, Y, Z or RAW[0] data were read. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining get shadow buffer protected in case an integration cycle completes just after the 1st byte is read.

8 I²C Slave Interface

Interface and control can be accomplished through an I²C compatible slave interface to a set of registers that access device control functions and output data. These control and output registers on the AS7225 are, in reality, implemented as virtual registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the pages that follow are explained in pseudocode for external I²C master writes and reads below. A compatible companion Flash device must be incorporated and pre-programmed for I²C virtual-registers to function.

8.1 I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support
- 7+1-bit addressing mode
- Write format: Byte
- Read format: Byte

Figure 13:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit Slave Address	Byte = 1001001x (device address = 49h) x= 1 for Master Read (byte = 93h) x= 0 for Master Write (byte = 92h)
STATUS Register	I²C slave interface STATUS register Read-only	Register Address = 0x00h Bit 1: TX_VALID 0 -> New data may be written to WRITE register 1 -> WRITE register occupied. Do NOT write. Bit 0: RX_VALID 0 -> No data is ready to be read in READ register. 1 -> Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register Write-only	Register Address = 0x01 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both virtual register addresses and write data.
READ Register	I²C slave interface READ register Read-only	Register Address = 0x02 8-Bits of data to be read by the I²C Master.

8.2 I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS7225. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

8.2.1 I²C Virtual Register Byte Write

Pseudocode

```
1    Poll I²C slave STATUS  register;
2    If TX_VALID bit is 0, a write can be performed on the interface;
3    Send a virtual register address and set the MSB of the register address to 1
     to indicate the pending write;
4    Poll I²C slave STATUS register;
5    If TX_VALID bit is 0, the virtual register address for the write has been
     received and the data may now be written;
6    Write the data.
```

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG    0x00

#define I2C_AS72XX_SLAVE_WRITE_REG     0x01

#define I2C_AS72XX_SLAVE_READ_REG      0x02

#define I2C_AS72XX_SLAVE_TX_VALID      0x02

#define I2C_AS72XX_SLAVE_RX_VALID      0x01


void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)

{

       volatile uint8_tstatus ;

       while (1)

       {
```

```
		// Read slave I2C status to see if the write buffer is ready.
		Status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;
		if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
			// No inbound TX pending at slave. Okay to write now.
			break ;
	}
	// Send the virtual register address (setting bit 7 to indicate a pending
write).	i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;
	while (1)
	{
		// Read the slave I2C status to see if the write buffer is ready.
		Status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;
		if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
			// No inbound TX pending at slave. Okay to write data now.
			break ;
	}
	// Send the data to complete the operation.
	i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

8.3 I²C Virtual Register Read Access

I²C Virtual Register Byte Read, detailed below, shows the pseudocode necessary to read virtual registers on the AS7225. Note that in this case, reading a virtual register, the register address is not modified.

8.3.1 I²C Virtual Register Byte Read

Pseudocode

```
1    Poll I²C slave STATUS register;
2    If TX_VALID bit is 0, the virtual register address for the read may be
     written;
3    Send a virtual register address;
4    Poll I²C slave STATUS register;
5    If RX_VALID bit is 1 the read data is ready;
6    Read the data.
```

Sample Code:

```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)

{

       volatile uint8_t status, d;

       while (1)

       {

              // Read slave I2C status to see if the read buffer is ready.

              Status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;


              if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)

                     // No inbound TX pending at slave. Okay to write now.

                     break ;

       }

       // Send the virtual register address (setting bit 7 to indicate a pending
       write).      i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg) ;

       while (1)

       {

              // Read the slave I2C status to see if our read data is available.

              status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;
```

```
            if ((status &  I2C_AS72XX_SLAVE_RX_VALID) !=  0)
                  // Read data is ready.
                  break;
      }
      // Read the data to complete the operation.
      d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
      return d ;s
}
```

The details of the i2cm_read() and i2cm_write() functions in previous Figures are dependent upon the nature and implementation of the external I²C master device.

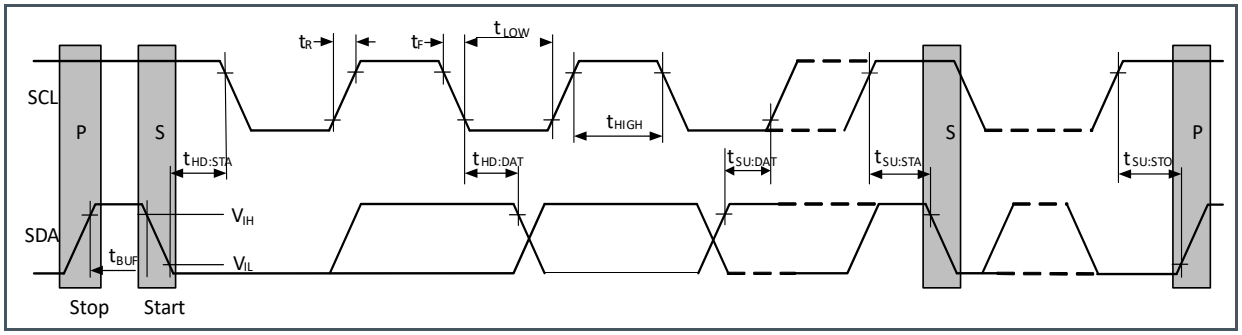
8.4 I²C Slave Timing Characteristics

Figure 14:
Electrical Characteristics of AS7225

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		I²C Interface				
f_{SCLK}	SCL Clock frequency		0	100	400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) Start		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

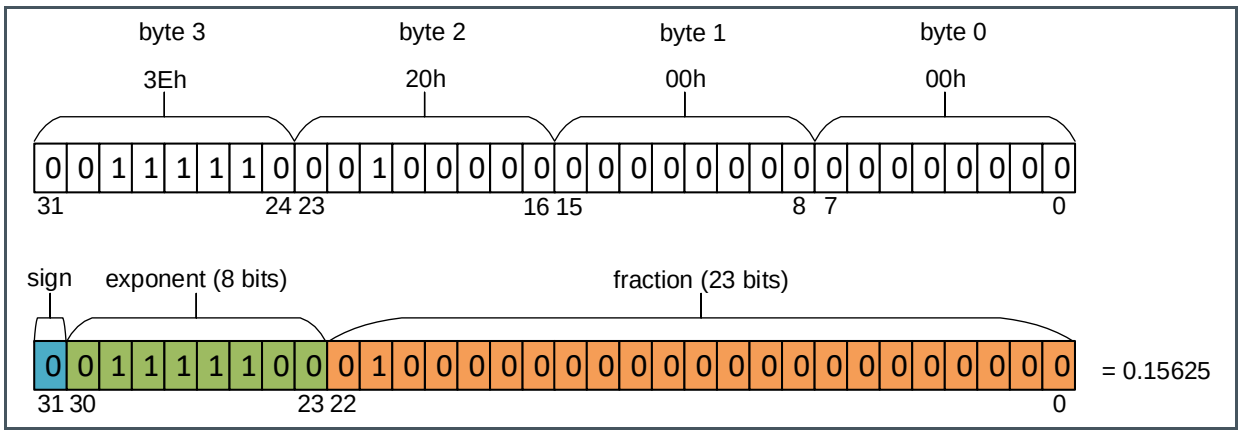
Figure 15:
I²C Slave Timing Diagram



8.5 4-Byte Floating-Point (FP) Registers

In addition to single and two byte, several 4-byte registers (hex) are shown in the tables starting below. Here is an example of how the registers are used to represent floating point data (based on the IEEE 754 standard):

Figure 16:
Example of the IEEE 754 Standard



The floating-point (FP) value assumed by 32 bit binary32 data with a biased exponent e (the 8 bit unsigned integer) and a 23 bit fraction is (for the above example):

Equation 1:

$$FPvalue = (-1)^{sign}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(e-127)}$$

Equation 2:

$$FPvalue = (-1)^{0}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(124-127)}$$

Equation 3:

$$FPvalue = 1 \times (1 + 2^{-2}) \times 2^{(-3)} = 0{,}15625$$

8.6 I²C Virtual Register Set

A register overview and a detailed description of the AS7225 I²C register set you find in chapter 10. All register data are hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Multiple byte registers (2 byte integer or 4 byte floating point) must be read in the order of ascending register addresses (low to high). In addition, if capable of being written to, have to be written in the order of ascending register addresses as well.

9 I²C Master Interface (Local Sensor Interface)

The I²C Master interface can be used to connect external sensors such as the TSL2572 ambient light sensor (or other external sensors with AS7225 native support). Once the AS7225 has detected the supported ambient light sensor, daylight-responsive dimming directives can be activated by using the ATCHANMOD command or DIR_CONF register.

9.1 I²C Feature List

- Clock is set to 400kHz
- 7+1-bit addressing mode.
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Random-Read, Sequential-Read

9.2 I²C Protocol

Figure 17:
I²C Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
SW	Slave address for write	R	Slave address
SR	Slave address for read	R	Slave address
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
Data	Data/write	R	8 bit
Data(n)	Data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Slave increment word address	R	During acknowledge

The above I²C symbol definition table describes the symbols used in the following Read and Write descriptions.

9.3 I²C Write Access

Byte Write and Page Write formats are used to write data to the slave.

Figure 18:
I²C Byte Write

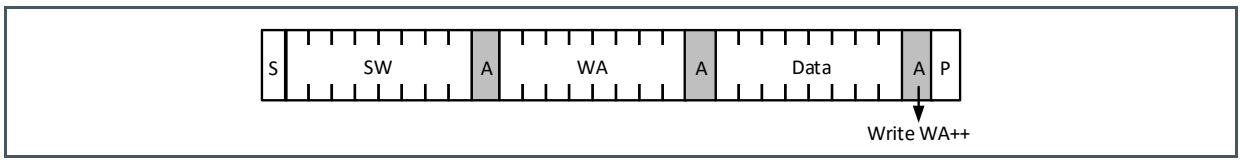
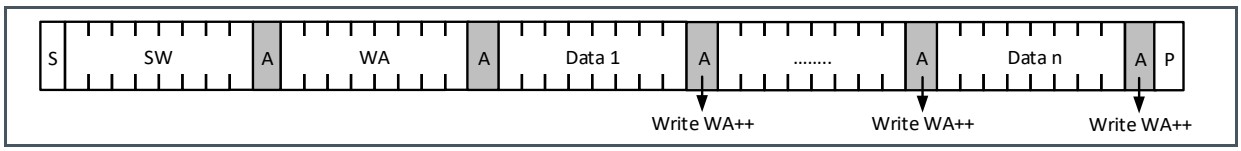


Figure 19:
I²C Page Write



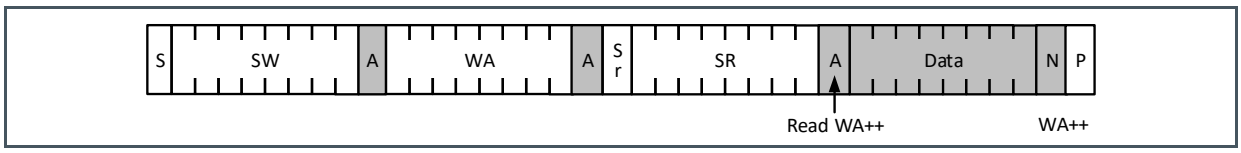
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the first register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

9.4 I²C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 20:
I2C Random Read



Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 21:
I2C Sequential Read

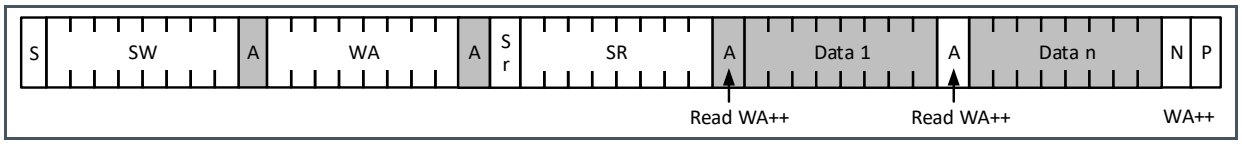


Figure 21 shows the format of an I²C sequential read access. Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledgement from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

The AS7225 is compatible to the NXP two wire specifications.
http://www.nxp.com/documents/user_manual/UM10204.pdf Version 4.0 Feb 2012 for standard mode and fast mode.

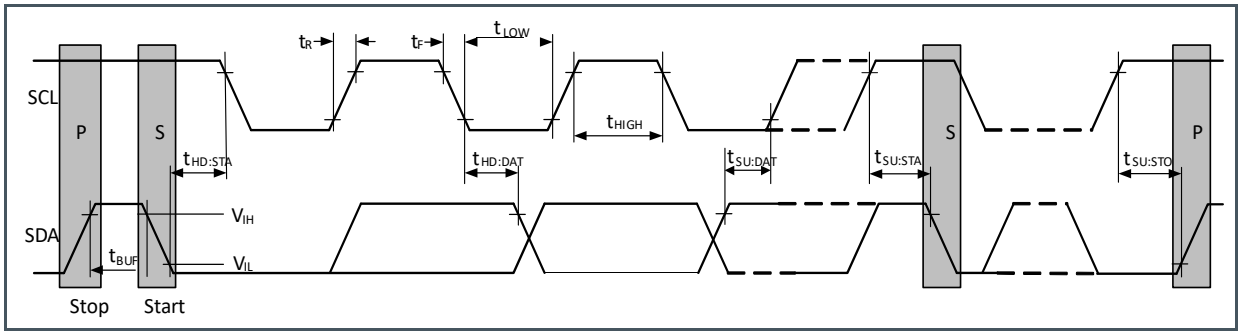
9.5 I²C Master Timing Characteristics

Figure 22:
I²C Master Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		I²C Interface				
f_{SCLK}	SCL Clock Frequency			400	400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB – total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 23:
I2C Master Timing Diagram



10 Register Description

10.1 Register Overview

Figure 24:
I²C Virtual Register Overview

Adress	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
				Device Version Registers					
0x00	HW_V_H								
0x01	HW_V_L								
0x02	FW_V_H								
0x03	FW_V_L								
				General Setup and Control Registers					
0x04	CONFIGURATION	SRST	RSVD		GAIN		RSVD	DATA_RDY	FRST
0x05	INTEGRATION_TIME								
0x06	TEMPERATURE								
0x07	LED_CONFIG								LED_IND
0x4F	ESP								
				Director Operations Register					
0x60	DIR_CONF			CHAN_MODE				INT	LEARN
0x61	DIR_CTRL								START
0x62	DIR_CH_1_H								
0x63	DIR_CH_1_L								
0x64	DIR_CH_2_H								
0x65	DIR_CH_2_L								
0x66	DIR_CH_3_H								
0x67	DIR_CH_3_L								
0x70	DIR_LUXT_H								
0x71	DIR_LUXT_L								
0x72	DIR_CCTT_H								
0x73	DIR_CCTT_L								

Adress	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
	Raw Value Registers								
0x08	RAW_VALUE_0_H								
0x09	RAW_VALUE_0_L								
0x0A	RAW_VALUE_1_H								
0x0B	RAW_VALUE_1_L								
0x0C	RAW_VALUE_2_H								
0x0D	RAW_VALUE_2_L								
0x0E	RAW_VALUE_3_H								
0x0F	RAW_VALUE_3_L								
0x10	RAW_VALUE_4_H								
0x11	RAW_VALUE_4_L								
0x12	RAW_VALUE_5_H								
0x13	RAW_VALUE_5_L								
	Calibration Coefficient registers								
0x50	COEF_DATA_0								
0x51	COEF_DATA_1								
0x52	COEF_DATA_2								
0x53	COEF_DATA_3								
0x54	COEF_READ								
0x55	COEF_WRITE								
	Calibrated Sensor Result Register								
0x14: 0x17	Cal_X								
0x18: 0x1B	Cal_Y								
0x1C: 0x1F	Cal_Z								
0x20: 0x23	Cal_x_1931								

Adress	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x24: 0x27	Cal_y_1931								
0x28: 0x2B	Cal_u_pri								
0x2C: 0x2F	Cal_v_pri								
0x30: 0x33	Cal_u								
0x34: 0x37	Cal_v								
0x38: 0x3B	DUV								
0x3C	LUX_H								
0x3D	LUX_L								
0x3E	CCT_H								
0x3F	CCT_L								
	Firmware Update Registers								
0x48	FW_CNTRL	START	STOP	BYTES_TRANSFERED	LOCK	SWITCH	BANK1	ERROR	CHKSUM
0x49	FW_BYTE_COUNT_H								
0x4A	FW_BYTE_COUNT_L								
0x4B	FW_PAYLOAD								

10.2 Detailed Register Description

10.2.1 Hardware Version Registers (Address 0x00/0x01)

These byte registers are used together as HW_V_H: HW_V_L

Figure 25:
Hardware Version Register High

Addr: 0x00		HW_VERSION_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type	0x40	R	Device type number

Figure 26:
Hardware Version Register Low

Addr: 0x01		HW_VERSION_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version	0x19	R	Hardware version number

10.2.2 Firmware Version Registers (Address 0x02/0x03)

These byte registers are used together as FW_V_H: FW_V_L. Set register 0x02 or 0x03 to 1-3 to get each firmware positions. Other write values set registers 0x02/0x03 to zero.

Figure 27:
Firmware Version Register High

Addr: 0x02 (R/W)		FW_VERSION_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	MAJOR Version	0	R	Major version high byte
15:8	PATCH Version	0	R	Patch version high byte
15:8	BUILD Version	0	R	Build version high byte
7:0	Firmware Position	0	W	FW position setting 1= Read out Major version 2= Read out Patch version 3= Read out Build version

Figure 28:
Firmware Version Register Low

Addr: 0x03 (R/W)		FW_VERSION_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	MAJOR Version	0	R	Major version low byte

Addr: 0x03 (R/W)		FW_VERSION_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PATCH Version	0	R	Patch version low byte
7:0	BUILD Version	0	R	Build version low byte
7:0	Firmware Position	0	W	FW position setting 1= Read out Major version 2= Read out Patch version 3= Read out Build version

10.2.3 Configuration Register (Address 0x04)

Figure 29:
Configuration Register

Addr: 0x04 (R/W)		CONFIGURATION		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SRST	0	R/W	R = gain error W= software reset
6	RSVD	0	-	Reserved, do not use
5:4	GAIN	00	R/W	Gain Setting 00=1x Gain; 01=3.7x; 10=16x; 11=64x
3:2	RSVD	00	-	Reserved, do not use
1	DATA_RDY	0	R	1= Conversion Data Ready to read, sets INT active if interrupt is enabled. Can be polled independent of INT usage. Cleared (=0) after read if set. Cleared (=0) after device reset.
0	FRST	0	W	Soft reset set to 1 for soft reset. Goes to 0 when complete

10.2.4 Integration Time Register (Address 0x05)

Figure 30:
INTEGRATION_TIME Register

Addr: 0x05 (R/W)		INTEGRATION_TIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INTEGRATION_TIME	20	R/W	Sensor integration time = <value>*2.8ms (valid value range 1-255)

10.2.5 Device Temperature Register (Address 0x06)

Figure 31:
Temperature Register

Addr: 0x06		TEMPERATURE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TEMPERATURE	-	R	Device internal temperature (1byte). Byte is a hex integer value, in °C.

10.2.6 LED Configuration Register (Address 0x07)

Figure 32:
LED_CONFIG Register

Addr: 0x07 (R/W)		LED_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LED_CONFIG	0x01	R/W	Enable/disable LED_IND

10.2.7 External Device Status Register (Address 0x4F)

Figure 33:
ESP Register

Addr: 0x4F		ESP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ESP	-	R	Read out the status/availability of external devices

10.2.8 Director Configuration Register (Address 0x60)

Figure 34:
DIR_CONF Register

Addr: 0x60 (R/W)		DIR_CONF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	CHAN_MODE	-	R/W	Select channel mode 0= Daylighting (CH1) 1= Daylighting (CH1) + Color Tuning (CH2/3) 2= Daylighting + Color Tuning (CH2/3) 3-15= reserved, do not use
1	INT	-	R/W	1= enable interrupt pin 0= disable
0	LEARN	-	R/W	1= activate learn mode Cleared by AS7225 automatically after being set and device reset.

10.2.9 Director Control Register (Address 0x61)

Figure 35:
DIR_CTRL Register

Addr: 0x61		DIR_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	START	0	R/W	1 = host MCU has completed last directive and is ready for new AS7225 conversion start. Cleared by AS7225 automatically when PWM target values are ready for the MCU or after a device reset.

10.2.10 Director Channel_1 Result Registers (Addresses 0x62, 0x63)

These byte registers are used together as DIR_CH_1_H: DIR_CH_1_L.

In Color Tuning operation, the registers create a 16 bit integer value from 0 to 65535 representing a PWM (Color + Dimming) tuning percentage between 0.00 and 100.00%.
Example: 0001101001001111 = 1A4F = 6735 = 10.28%

In Daylighting operation, the registers create a 16 bit integer value from 0 to 65535 representing a PWM Lux tuning percentage between 0.00 and 100.00%.

Figure 36:
Director Channel_1 Result Register High

Addr: 0x62		DIR_CH_1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_1_H	00000000	R	Channel 1 high byte CHAN_MODE 0 = Dimming CHAN_MODE 1 = Dimming CHAN_MODE 2 = overall brightness (only for information)

Figure 37:
Director Channel_1 Result Register Low

Addr: 0x63		DIR_CH_1_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_1_L	00000000	R	Channel 1 low byte

10.2.11 Director Channel_2 Result Registers (Addresses 0x64, 0x65)

These byte registers are used together as DIR_CH_2_H: DIR_CH_2_L

The registers create a 16 bit integer value from 0 to 65535 representing a PWM (Color + Dimming) tuning percentage between 0.00 and 100.00%.
Example: 0001101001001111 = 1A4F = 6735 = 10.28%

Figure 38:
Director Channel_2 Result Register High

Addr: 0x64		DIR_CH_2_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_2_H	00000000	R	Channel 2 high byte CHAN_MODE 0 = Disabled (0) CHAN_MODE 1 = String1 COLOR_TUNING CHAN_MODE 2 = String 2 COLOR_TUNING incl. dimming

Figure 39:
Director Channel_2 Result Register Low

Addr: 0x65		DIR_CH_2_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_2_L	00000000	R	Channel 2 low byte

10.2.12 Director Channel_3 Result Registers (Addresses 0x66, 0x67)

These byte registers are used together as DIR_CH_3_H: DIR_CH_3_L

The registers create a 16 bit integer value from 0 to 65535 representing a PWM (Color + Dimming) tuning percentage between 0.00 and 100.00%.
Example: 0001101001001111 = 1A4F = 6735 = 10.28%

Figure 40:
Director Channel_3 Result Register High

Addr: 0x66		DIR_CH_3_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_3_H	00000000	R	Channel 3 high byte CHAN_MODE 0 = Disabled (0) CHAN_MODE 1 = String1 complement COLOR_TUNING CHAN_MODE 2 = String 2 COLOR_TUNING incl. dimming

Figure 41:
Director Channel_3 Result Register Low

Addr: 0x67		DIR_CH_3_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_3_L	00000000	R	Channel 3 low byte

10.2.13 Director Target for LUX Registers (Addresses 0x70, 0x71)

These byte registers are used together as DIR_LUXT_H: DIR_LUXT_L.

They create a 16 bit integer value for LUX target.
Example: 0000001111101000 = 1000 LUX

Figure 42:
Director Target for LUX Register High

Addr: 0x70 (R/W)		DIR_LUXT_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_LUXT_H	00000000	R/W	Director target for LUX high byte

Figure 43:
Director Target for LUX Register Low

Addr: 0x71 (R/W)		DIR_LUXT_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_LUXT_L	00000000	R/W	Director target for LUX low byte

10.2.14 Director Target for CCT Registers (Addresses 0x72, 0x73)

These byte registers are used together as DIR_CCTT_H: DIR_CCTT_L.

They create a 16 bit integer value for CCT target (Kelvin).
Example: 0000101110111000 = 3000 °K

Figure 44:
Director Target for CCT Register High

Addr: 0x72 (R/W)		DIR_CCTT_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CCTT_H	00000000	R/W	Director target for CCT high byte

Figure 45:
Director Target for CCT Register Low

Addr: 0x73 (R/W)		DIR_CCTT_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CCTT_L	00000000	R/W	Director target for CCT low byte

10.2.15 Raw Value Registers (Addresses 0x08:0x13)

These byte registers are used together as RAW_VALUE_x_H: RAW_VALUE_x_L.

Figure 46:
Raw Value X Register High

Addr: 0x08		RAW_VALUE_0_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_0_H	-	R	Raw Value X Channel high byte

Figure 47:
Raw Value X Register Low

Addr: 0x09		RAW_VALUE_0_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_0_L	-	R	Raw Value X Channel low byte

Figure 48:
Raw Value Y Register High

Addr: 0x0A		RAW_VALUE_1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_1_H	-	R	Raw Value Y Channel high byte

Figure 49:
Raw Value Y Register Low

Addr: 0x0B		RAW_VALUE_1_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_1_L	-	R	Raw Value Y Channel low byte

Figure 50:
Raw Value Z Register High

Addr: 0x0C		RAW_VALUE_2_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_2_H	-	R	Raw Value Z Channel high byte

Figure 51:
Raw Value Z Register Low

Addr: 0x0D		RAW_VALUE_2_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_2_L	-	R	Raw Value Z Channel low byte

Figure 52:
Raw Value NIR Register High

Addr: 0x0E		RAW_VALUE_3_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_3_H	-	R	Raw Value NIR Channel high byte

Figure 53:
Raw Value NIR Register Low

Addr: 0x0F		RAW_VALUE_3_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_3_L	-	R	Raw Value NIR Channel low byte

Figure 54:
Raw Value DK Register High

Addr: 0x10		RAW_VALUE_4_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_4_H	-	R	Raw Value Dark Channel high byte

Figure 55:
Raw Value DK Register Low

Addr: 0x11		RAW_VALUE_4_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_4_L	-	R	Raw Value Dark Channel low byte

Figure 56:
Raw Value CL Register High

Addr: 0x12		RAW_VALUE_5_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_5_H	-	R	Raw Value Clear Channel high byte

Figure 57:
Raw Value CL Register Low

Addr: 0x13		RAW_VALUE_5_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RAW_VALUE_5_L	-	R	Raw Value Clear Channel low byte

10.2.16 Calibration Coefficient Registers (Addresses 0x50:0x53, 0x54, 0x55)

If the requirements of the factory calibration cannot fulfilled or the factory calibration do not match the application requirements, these registers enable settings of an additional calibration coefficient for a customized calibration to improve the accuracy of the light system.

These 4 byte floating point registers can be used as needed by the MCU to individually scale the calibration coefficient data registers.

Figure 58:
COEF_DATA Register

Addr: 0x50:0x53 (R/W)		COEF_DATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	COEF_DATA	-	R/W	Calibration coefficient (4 byte floating point)

Figure 59:
COEF_READ Register

Addr: 0x54 (R/W)		COEF_READ		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	COEF_READ	-	R/W	Set sub addresses to read different calibration data from COEF_DATA registers 0x00 - 0x08: production matrix 0x10 - 0x18: application matrix 0x30: norm gain (UINT8 - ADDR 0x50) 0x31: norm integration time (UINT8 - ADDR 0x50) 0x32: Set IR scalar X 0x33: Set IR scalar Y 0x34: Set IR scalar Z value out of range: 0xFFFFFFFF - NaN (Error)

Figure 60:
COEF_WRITE Register

Addr: 0x55 (R/W)		COEF_WRITE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	COEF_WRITE	-	R/W	Set sub addresses to write different calibration data from COEF_DATA registers to persistent memory 0x00 - 0x08: production matrix 0x10 - 0x18: application matrix 0x30: norm gain (UINT8 - ADDR 0x50) 0x31: norm integration time (UINT8 - ADDR 0x50) 0x32: Set IR scalar X 0x33: Set IR scalar Y 0x34: Set IR scalar Z value out of range: 0xFFFFFFFF - NaN (Error)

10.2.17 Calibrated XYZ Result Registers (Addresses 0x14:0x17, 0x18:0x1B, 0x1C:0x1F)

Figure 61:
Calibrated X Result Register

Addr: 0x14:0x17		Cal_X		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_X	-	R	Calibrated X data (4 byte floating point)

Figure 62:
Calibrated Y Result Register

Addr: 0x18:0x1B		Cal_Y		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_Y	-	R	Calibrated Y data (4 byte floating point)

Figure 63:
Calibrated Z Result Register

Addr: 0x1C:0x1F		Cal_Z		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_Z	-	R	Calibrated Z data (4 byte floating point)

10.2.18 Calibrated CIE 1931 x and y Result Registers (Addresses 0x20:0x23, 0x24:0x27)

Figure 64:
Calibrated CIE 1931 x Result Register

Addr: 0x20:0x23		Cal_SMALL_X		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_SMALL_X	-	R	Calibrated x data (4 byte floating point)

Figure 65:
Calibrated CIE 1931 y Result Register

Addr: 0x24:0x27		Cal_SMALL_Y		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_SMALL_Y	-	R	Calibrated y data (4 byte floating point)

10.2.19 Calibrated CIE 1976 u', v', u, v Result Registers (Addresses 0x28;0x2B, 0x2C:0x2F, 0x30:0x33, 0x34:0x37)

Figure 66:
Calibrated CIE 1976 u' Result Register

Addr: 0x28:0x2B		Cal_U_PRIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_U_PRIME	-	R	Calibrated u' data (4 byte floating point)

Figure 67:
Calibrated CIE 1976 v' Result Register

Addr: 0x2C:0x2F		Cal_V_PRIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_V_PRIME	-	R	Calibrated v' data (4 byte floating point)

Figure 68:
Calibrated CIE 1976 u Result Register

Addr: 0x30:0x33		Cal_SMALL_U		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_SMALL_U	-	R	Calibrated u data (4 byte floating point)

Figure 69:
Calibrated CIE 1976 v Result Register

Addr: 0x34:0x37		Cal_SMALL_V		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	Cal_SMALL_V	-	R	Calibrated v data (4 byte floating point)

10.2.20 Calibrated DUV Result Register (Address 0x38:0x3B)

Figure 70:
Calibrated DUV Result Register

Addr: 0x38:0x3B		DUV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	DUV	-	R	Calibrated DUV data (4 byte floating point)

10.2.21 Calibrated LUX Result Registers (Addresses 0x3C, 0x3D)

These byte registers are used together as LUX_H: LUX_L.

They create a 16 bit integer value for calibrated LUX.
Example 0000001111101000 = 1000 Lux

Figure 71:
Calibrated LUX Result Register High

Addr: 0x3C		LUX_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LUX_H	-	R	Calibrated LUX data, high byte

Figure 72:
Calibrated LUX Result Register Low

Addr: 0x3D		LUX_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LUX_L	-	R	Calibrated LUX data, low byte

10.2.22 Calibrated CCT Result Registers (Addresses 0x3E, 0x3F)

These byte registers are used together as CCT_H: CCT_L.

They create a 16 bit integer value for sensed CCT in Kelvin.
Example: 0000101110111000 = 3000 K

Figure 73:
Calibrated CCT Result Register High

Addr: 0x3E		CCT_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CCT_H	-	R	Calibrated CCT data, high byte

Figure 74:
Calibrated CCT Result Register Low

Addr: 0x3F		CCT_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CCT_L	-	R	Calibrated CCT data, low byte

10.2.23 Firmware Update Registers (Addresses 0x48:0x4B)

The firmware handles two independent images in the flash device: the first one is located on address 0x12000 and the second is on address 0x22000 available. The firmware file has a size of 56k bytes.

Figure 75:
Firmware Control Register

Addr: 0x48 (R/W)		FW_CNTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	START	-	R/W	Set bit once to configure the device for firmware update
6	STOP	-	W	Reset firmware update state machine
5	BYTES_TRANSFERED	-	R	All 56k bytes are transferred
4	LOCK	-	R/W	Lock this firmware for next start
3	SWITCH	-	W	Switch between both firmware versions

Addr: 0x48 (R/W)		FW_CNTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	BANK1	-	R	Set if bank1 is active, else bank2
1	ERROR	-	R	Error occurred while firmware update
0	CHKSUM	-	R	Checksum of other bank is valid

Figure 76:
Firmware Byte Counter Register High

Addr: 0x49		FW_BYTE_COUNT_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FW_BYTE_COUNT_H	0	R	Byte counter of transferred image high byte

Figure 77:
Firmware Byte Counter Register Low

Addr: 0x4A		FW_BYTE_COUNT_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FW_BYTE_COUNT_L	0	R	Byte counter of transferred image low byte

Figure 78:
Firmware Payload Register

Addr: 0x4B (R/W)		FW_PAYLOAD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FW_PAYLOAD	0	R/W	Transfer of the firmware byte

11 UART Command Interface

The UART block implements the TX and RX signals as defined in the RS-232 / V.24 standard communication protocol. A SPI Flash is a required operating companion device for the AS7225 to function or to communicate via the UART interface. Using other devices can cause communication issues and may not be compatible. See Figure 83 for supported devices, which are tested by **ams**. The “xx” in the serial flash name stands for alternative packages. Flash timing is provided in Figure 81 and Figure 82 for debug purposes.

11.1.1 UART Feature List

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Factory set to 115.2k Baud
- Supports Serial Frames with 8 Data Bits, no Parity and 1 Stop Bit.

11.1.2 Operation

Transmission

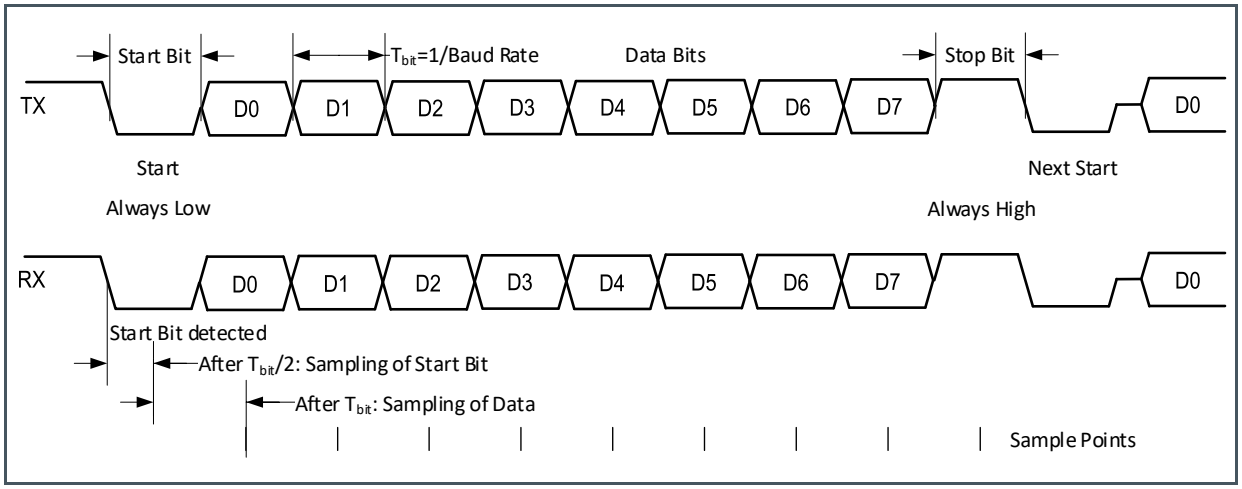
If data is available, it will be moved into the output shift register and the data will be transmitted at the Baud Rate, starting with a Start Bit (logic zero) and followed by a Stop Bit (logic one).

Reception

At any time, with the receiver being idle, if a falling edge of a start bit is detected on the input, a byte will be received. The following Stop Bit will be checked to be logic one.

11.2 UART Protocol

Figure 79:
UART Protocol



11.3 SPI Timing Characteristics

The AS7225 contains a serial UART interface to connect to a flash memory. An Overview can be found in Figure 83. The required timing characteristics for a serial interface is shown in Figure 81 and in Figure 82 accordingly. If a Flash memory is used which is not listed in Figure 83 it should be ensured that the SPI timing is achieved (for debug purposes). Contact **ams** for requests to support/verify additional flash devices beyond those listed in the most current device verification listing.

Figure 80:
SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		SPI Interface				
f_{SCK}	Clock frequency		0		16	MHz
t_{SCK_H}	Clock high time		40			ns
t_{SCK_L}	Clock low time		40			ns
t_{SCK_RISE}	SCK rise time		5			ns
t_{SCK_FALL}	SCK fall time		5			ns
t_{CSN_S}	CSN setup time	Time between CSN high-low transition to first SCK high transition	5			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSN_H}	CSN hold time	Time between last SCK falling edge and CSN low-high transition	5			ns
t_{CSN_DIS}	CSN disable time		10			ns
t_{DO_S}	Data-out setup time		5			ns
t_{DO_H}	Data-out hold time		5			ns
t_{DI_V}	Data-in valid		10			ns

Figure 81:
SPI Master Write Timing

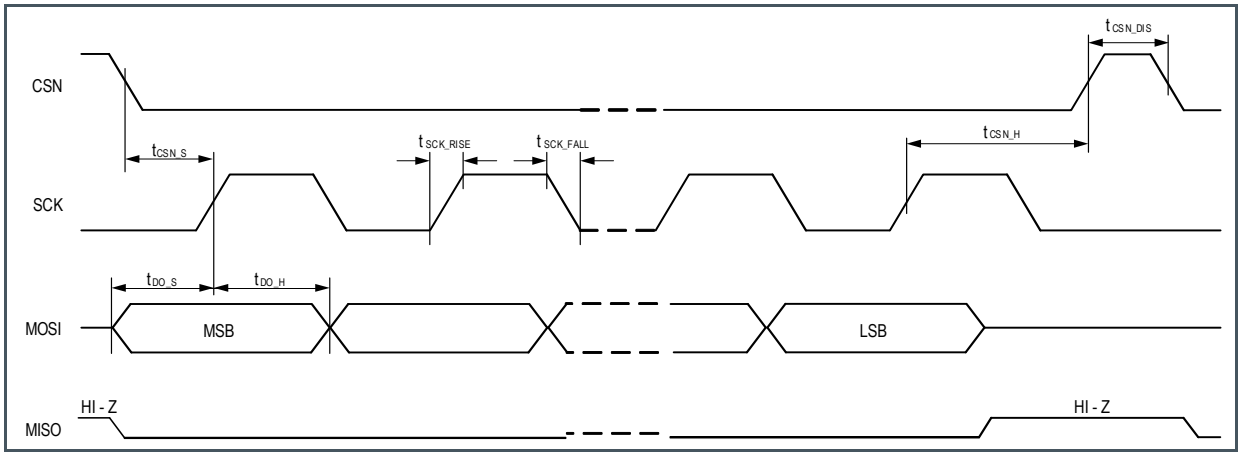
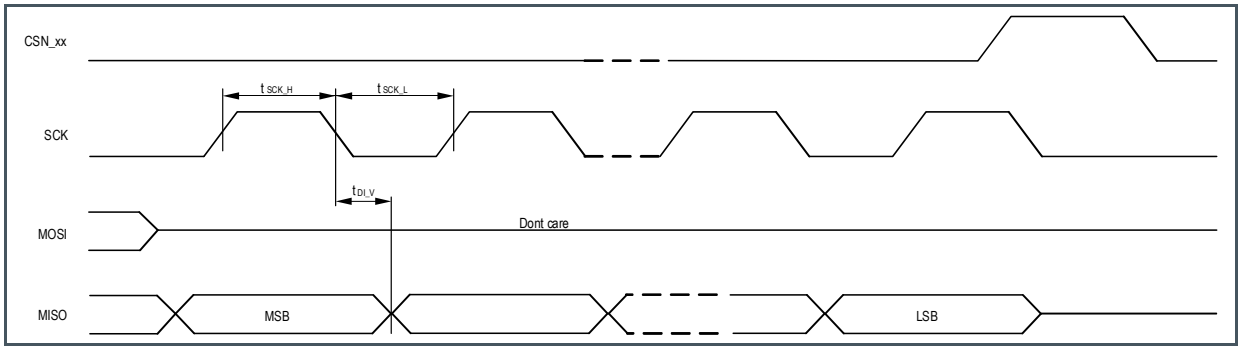


Figure 82:
SPI Master Read Timing



11.4 Serial Flash

A SPI Flash device is a required operating companion to the AS7225. See Figure 83 for supported devices, which are tested by **ams**. Using other devices can cause communication issues and may not be compatible. Flash timing is provided in Figure 81 and Figure 82 for debug purposes.

Figure 83:
Flash Memory Overview

Serial Flash	Manufacturer
AT25SF041xx	Adesto Technologies
AT25DF041xx	Adesto Technologies
MX25L4006ExxI-12G	Macronix
SST25PF040C	Microchip Technology
W25X40CLSNIG	Winbond Electronics
LE25U40CMD	ON Semiconductor
GD25Q40C	GigaDevice
FS25Q004F1	Foresee

Additional devices may have been added to this list after publication of this datasheet. See “AS72xx External Flash program and update” application note available on the **ams** AS7225 product document section of the **ams** website.

12 Smart Lighting Command Interface

The Smart Lighting Director supports a high-level, driverless text control interface using its Smart Lighting Command Set (SLCS) communicated through the UART interface. The Smart Lighting Director provides a rich configuration and control interface to speed the time-to-design and time-to-market for luminaire, replacement lamp and driver manufacturers. The Smart Lighting Director uses a variation of an “AT command model” as popularized by early Hayes modems. The SLCS is integrated into the required binary operating image that is included on the USB memory stick provided with the AS7225 Smart Lighting Demo Kit, or it can be downloaded via https://download.ams.com/ . Login is required and a login can be obtained through the email address provided on the download site.

A configuration tool is available from **ams** to allow the luminaire, lamp or driver manufacturer to create their own “factory default” conditions that will be integrated with the **ams** -supplied initial binary image to create a ready-to-program default Flash image. The configuration tool is also available from https://download.ams.com/ .

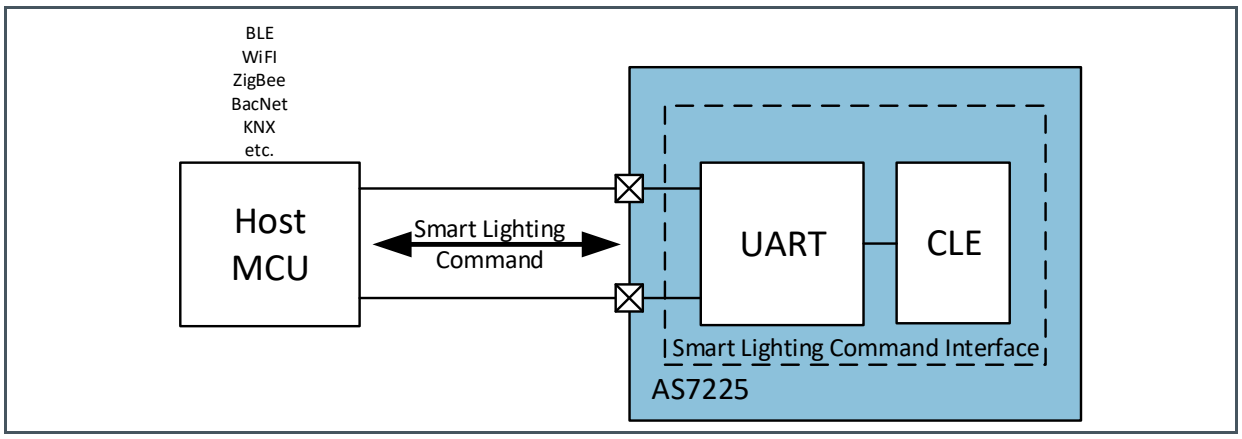
Write commands are constructed in the format “ATcmd=xxx” with the SLD returning the requested data value followed by the “OK” text reply. Commands that are unsuccessfully interpreted or are otherwise invalid will return an “ERROR” text reply.

For example:

- Set the desired daylight LUX level target: ATLUXT=500 <OK>
- Read current lux target set point: ATLUXT <500 OK>
- Read current calibrated lux level as observed by the sensor: ATLUXC <497 OK>

The “Smart Lighting Command Interface”, shown below between the network interface and the core of the system, provides access to the Smart Lighting Director’s lighting control and configuration functions.

Figure 84:
Smart Lighting Command Interface



12.1 AT Commands

The command interface to control the AS7225 is via the UART, using AT commands across the UART interface. The AT command interface block diagram, shown in Figure 84 between the network interface and the core of the system, provides access to the AS7225's Cognitive Light Engine's control and configuration functions (see also chapter UART Command Interface).

In the command description below, numeric values may be specified with no leading prefix, in which case they will be interpreted as decimals, with leading "0x" to indicate that they are hexadecimal numbers, or with a leading "b" to indicate, that they are binary numbers. The commands are grouped into functional areas Texts appearing between angle brackets ('<' and '>') are commands or response argument. A carriage return character, a linefeed character, or both may terminate commands to the SLD. The SLD command output is a response followed by a linefeed character. Note that any command that cannot interpreted or which encounters an error will generate "ERROR" response.

Figure 85:
AT Commands

Command	Direction	Description	Format	Value range	Default
Status					
AT	R	NOP	-	-	-
ATVERSW	R	Return the current software version number	DEZ	<MAJOR.MINOR.PATCH>	-
ATVERHW	R	Returns the system hardware version as a HEX value of the form PRDTx where are P=PartID and R=ChipRevision and DT=DeviceType .	HEX	<0xPRDT> PR = 40 DT = 19 (AS7225)	0x4019
ATTEMP	R	Read the current device temperature in degrees Celsius	DEZ	-	-
ATXYZC	R	Read calibrated X, Y and Z data	DEZ	<XXX.X, YYY.Y, ZZZ.Z>	-
ATSMALLXYC	R	Read calibrated x and y for CIE 1931 color gamut	DEZ	<xxxx.xxxx, yyyy.yyyy>	-

Command	Direction	Description	Format	Value range	Default
ATUVPRIMEC	R	Read calibrated u', v' and u, v for CIE 1976 color gamut	DEZ	<u'u'u'u'.u'u'u'u',v'v'v'v'v'.v'v'v', uuuuu.uuuu,vvvvv.vvvv>	-
ATDATA	R	Read all six raw values: red, green, blue, ir, dark, clear	DEZ	<r, g, b, ir, d, c>	-
ATDUVC	R	Read delta uv values	DEZ	XXXXX.XXXX	-
ATESP	R	Read the single 16 bit sum of ESP1 board device available	HEX	Bit0 = TSL2572	-
Director Config					
ATCHAN1	R	CHAN_MODE 0: Dimming CHAN_MODE1: Dimming CHAN_MODE 2: overall brightness (only for information)	DEZ		0
ATCHAN2	R	CHAN_MODE 0: disabled (0) CHAN_MODE 1: STRING1 COLOR_TUNING CHAN_MODE 2: STRING1 COLOR_TUNING with DIMMING	DEZ		0
ATCHAN3	R	CHAN_MODE 0: disabled (0) CHAN_MODE 1: STRING1 complement COLOR_TUNING CHAN_MODE 2: STRING2 COLOR_TUNING with DIMMING	DEZ		0

Command	Direction	Description	Format	Value range	Default
ATCHANMOD	R/W	Select the channel mode. After channel switch, learning is again necessary	DEZ	CHAN_MODE: 0: DIMMING (CH1) 1: DIMMING (CH1) + COLOR_TUNING (CH2/3) 2: DIMMING + COLOR_TUNING (CH2/3) 3 - 15: reserved, not used yet	0
ATLEARN	R/W	Enables the channel learn mode. The maximum ratings will be saved internally. On software reset or power cycle the data will be available again and learn mode will be disabled	DEZ	R: 1 - learn mode is active W: only 1 for activate learn mode	1
ATINTRP	R/W	Enable/Disable Interrupt Pin, Default pin state: low (pin disabled) or high (pin enabled), Goes to low when new channel values are available. Will be reset to high, if channel data were read	DEZ	0 - disable, 1 - enable Interrupt pin functionality	0
ATCALC	R/W	Starts new calculation	DEZ	R: 1 – calculation is running W: only 1 for start calculation	0
Control					
ATINTTIME	R/W	Set sensor integration time. Integration time = <value> x ~2.8msecs.	DEZ	1-255	20
ATGAIN	R/W	Set sensor gain: 0=1x gain, 1=3.7x, 2=16x, 3=64x	DEZ	0-3	1
ATLED0	R/W	Enables or disables the indication LED	DEZ	0 - LED off / 1 – LED on	1

Command	Direction	Description	Format	Value range	Default
ATSRST	W	Software reset	-	-	-
ATFRST	W	Factory Reset. Stored values are reset to 'Factory' defaults. Afterwards a software reset is started.	-	-	-
Correlated Color Temperature (CCT)					
ATCCTT	R/W	Set the color control target value in integer (in Kelvin)	DEZ	400-15000	2700
ATCCTC	R	Return the calibrated CCT value	DEZ	400-15000	-
Daylight Harvesting / Illumination Control					
ATLUXT	R/W	Set illumination target LUX value	DEZ	0-64000	400
ATLUXC	R	Read the illumination in LUX (if external TSL2572, use this)	DEZ	0-64000	-
Calibration Values					
ATNORMGAIN	R/W	Set/Get the gain which the calibration values were measured	DEZ	Same as ATGAIN	1
ATNORMINTT	R/W	Set/Get the integration time which the calibration values were measured	DEZ	Same as ATINTTIME	59
ATIRXS	R/W	Write IR scalar for value X	DEZ	-	p2ram value 0.0
ATIRYS	R/W	Write IR scalar for value Y	DEZ	-	p2ram value 0.0
ATIRZS	R/W	Write IR scalar for value Z	DEZ	-	p2ram value 0.0

Command	Direction	Description	Format	Value range	Default
ATCMxy	R/W	Write 3x3 color matrix to flash, x,y = [0..2]	DEZ	-	p2ram value 1,0,0 0,1,0 0,0,1
ATAMxy	R/W	Write 3x3 application matrix to flash, x,y = [0..2]	DEZ	-	1,0,0 0,1,0 0,0,1
Firmware Update					
ATFWU	W	Starts firmware update process and transfer the bin file checksum	-	-	-
ATFW	W	Download new firmware Up to 10 bytes of firmware image at a time (20 hex bytes with no leading or trailing 0x) Repeat command till all 56k bytes of firmware are downloaded	-	HEX STRING (without 0x), max 10 bytes	-

Command	Direction	Description	Format	Value range	Default
ATFWS	W	Test the checksum on the non-active FW partition and if correct switches active partition. This is a toggle and can be used to toggle between 2 firmware partitions. Note, the first 5 bytes in page 0 are not touched. It is only temporary switch and must be used to check the new firmware whether the communication works!	-	-	-
ATFWL	W	This command locks the current firmware to start on power cycles. It rewrites the first 5 bytes in page 0!	-	-	-
ATFWC	R	This command gives information about the current firmware state	HEX	Bit0 – checksum of non-active firmware ok Bit1 – error occurred Bit2 – is bank 1 active Bit3 – not used Bit4 – current firmware is locked Bit5 – 56k bytes transferred Bit6 – not used Bit7 – Firmware update active	-

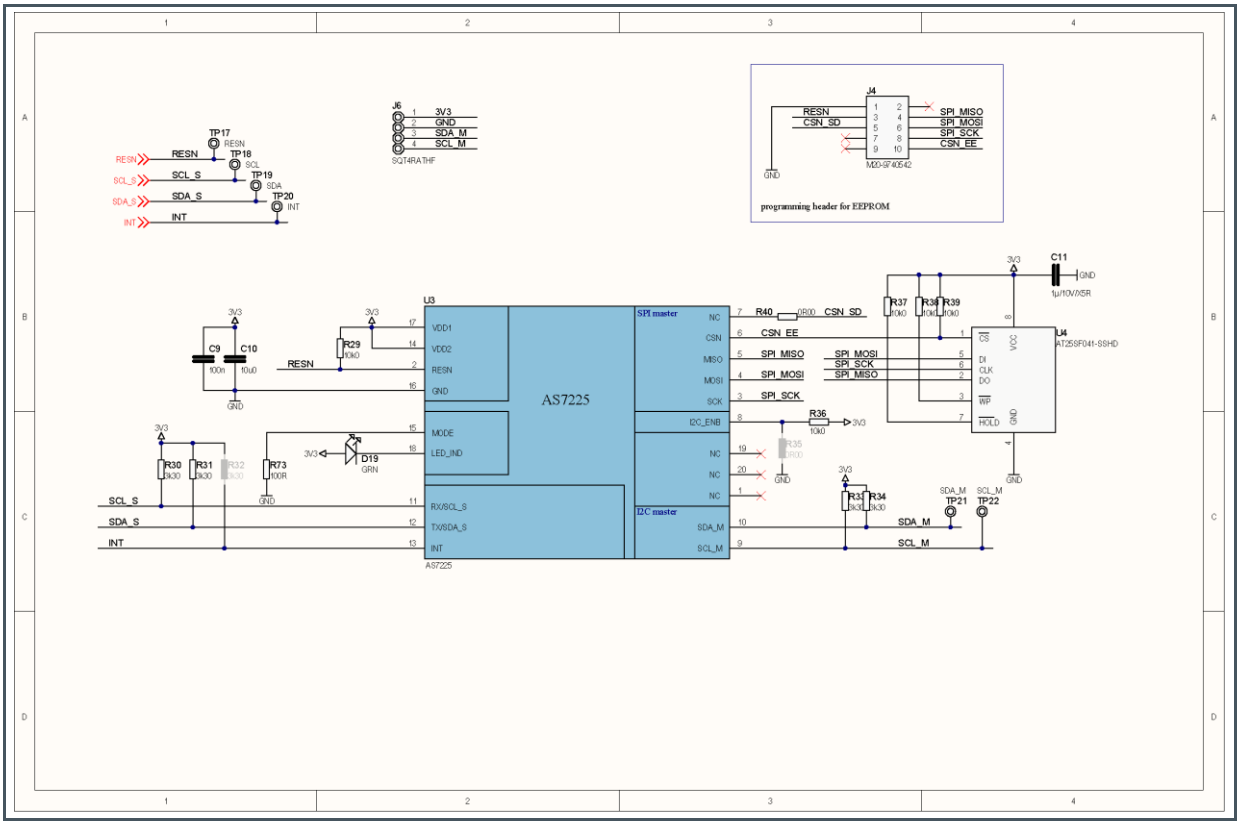
Command	Direction	Description	Format	Value range	Default
ATFWA	W	Only for backward compatibility to support old firmware update mechanism. Always returns with OK. Because of flash devices, it is not possible to increment the address separately (Page erase necessary!)	-	-	-

13 Application Information

Figure 86, Figure 87 and Figure 88 show typical application schematics for the AS7225. Figure 89 illustrates a routing example for the device and Figure 90 gives the recommended pad layout for the LGA package.

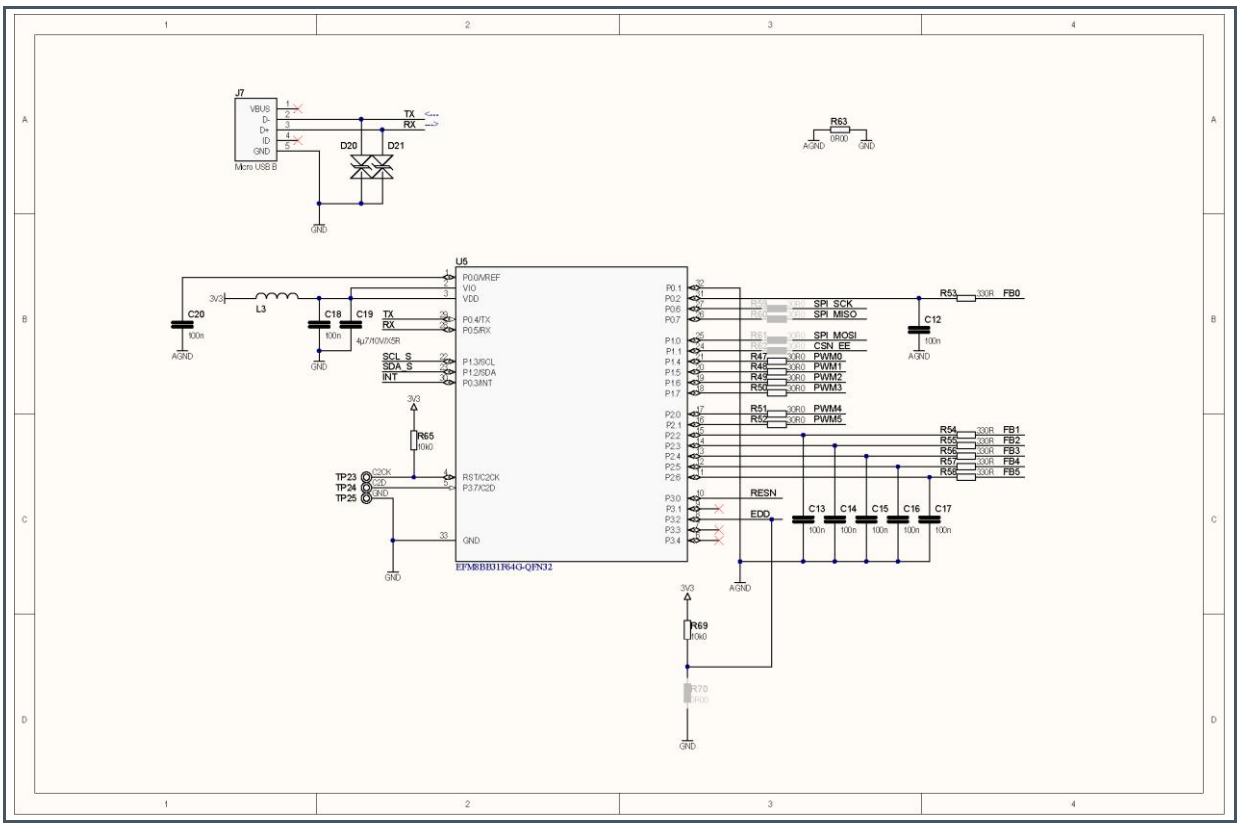
13.1 Schematic

Figure 86:
AS7225 Color Tuning and Daylighting Application



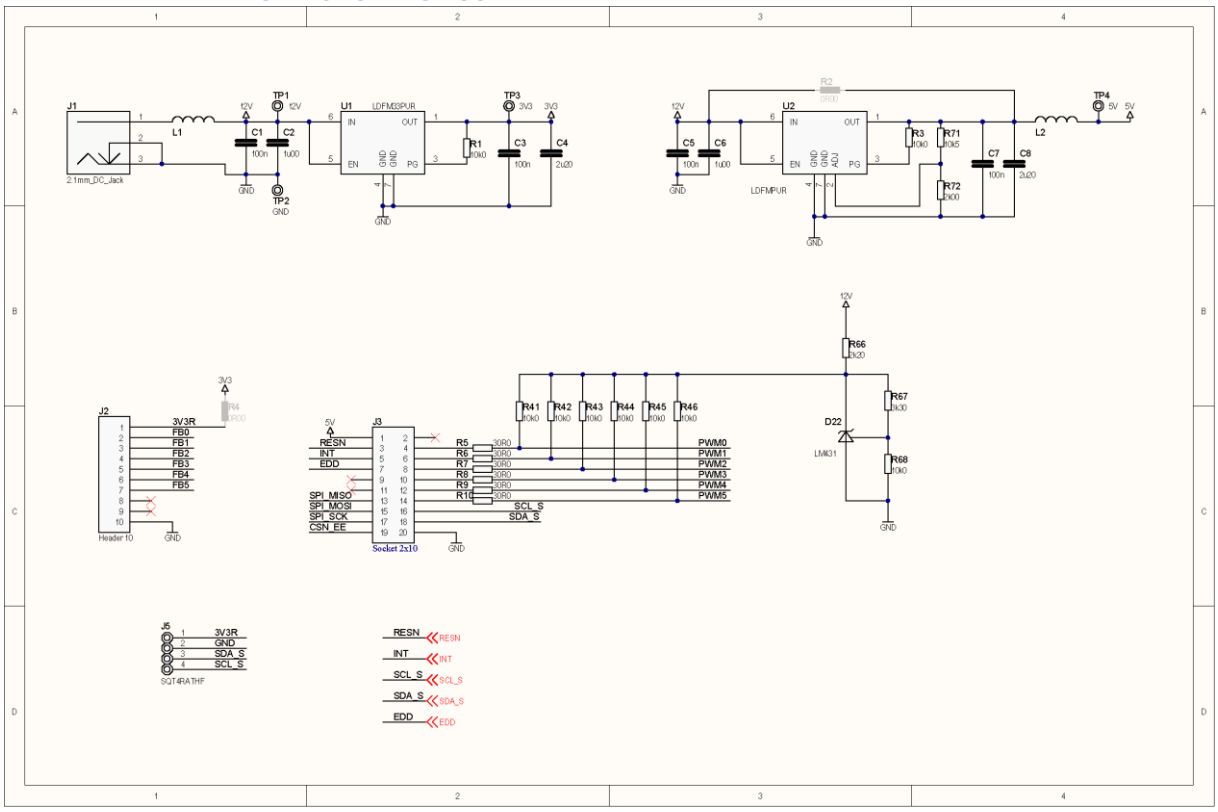
AS7225 Color Tuning and Daylighting Application: AS7225 Inward-looking luminaire integration requires additional supported sensor via I²C for daylighting.

Figure 87:
AS7225 Color Tuning, Daylighting Application



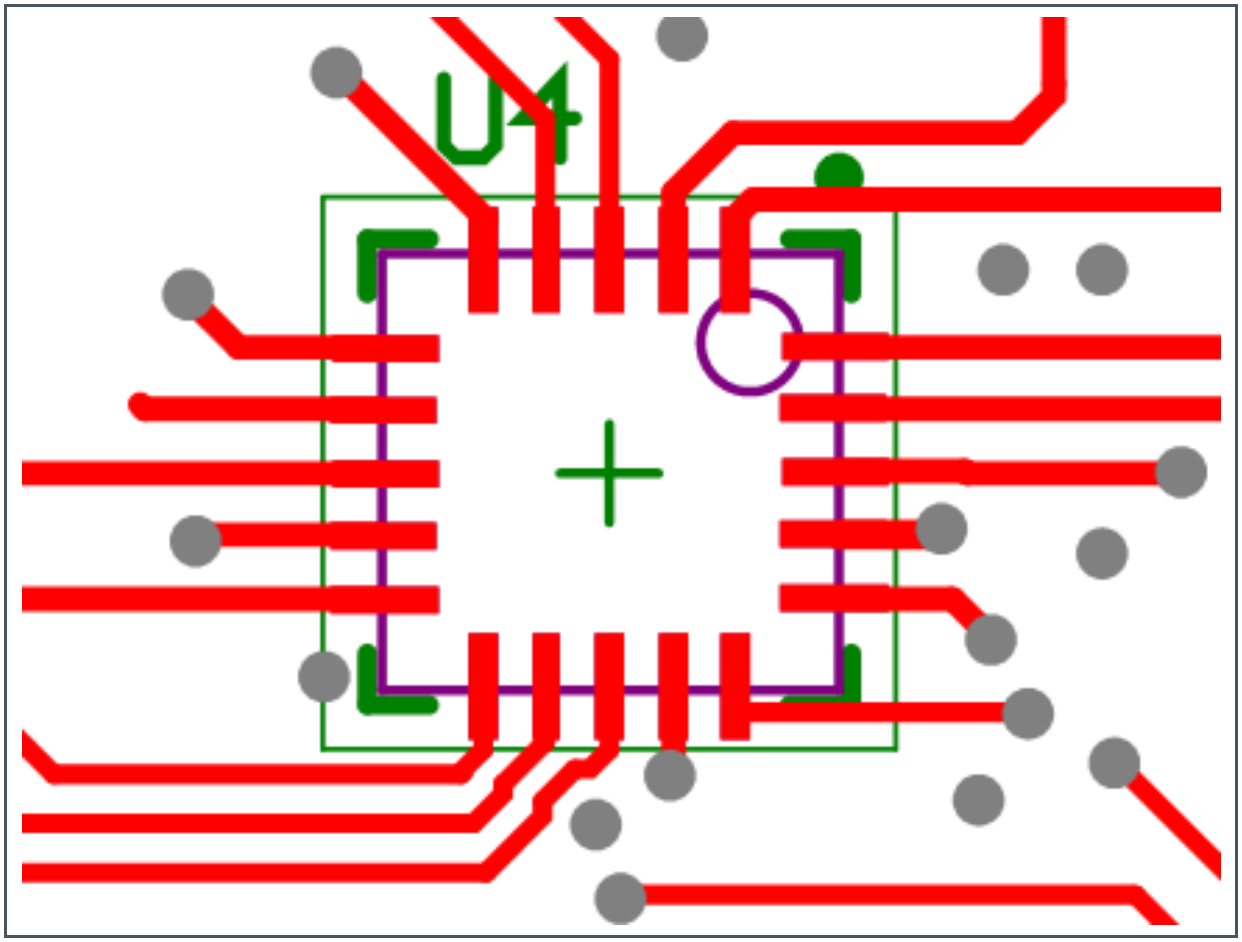
AS7225 Daylighting Application: AS7225 Outward-looking luminaire integration uses the integrated sensor for daylighting. CCT-tuning is not supported for outward looking configurations.

Figure 88:
AS7225 Color Tuning, Daylighting Application



13.2 PCB Layout

Figure 89:
Typical Layout Routing



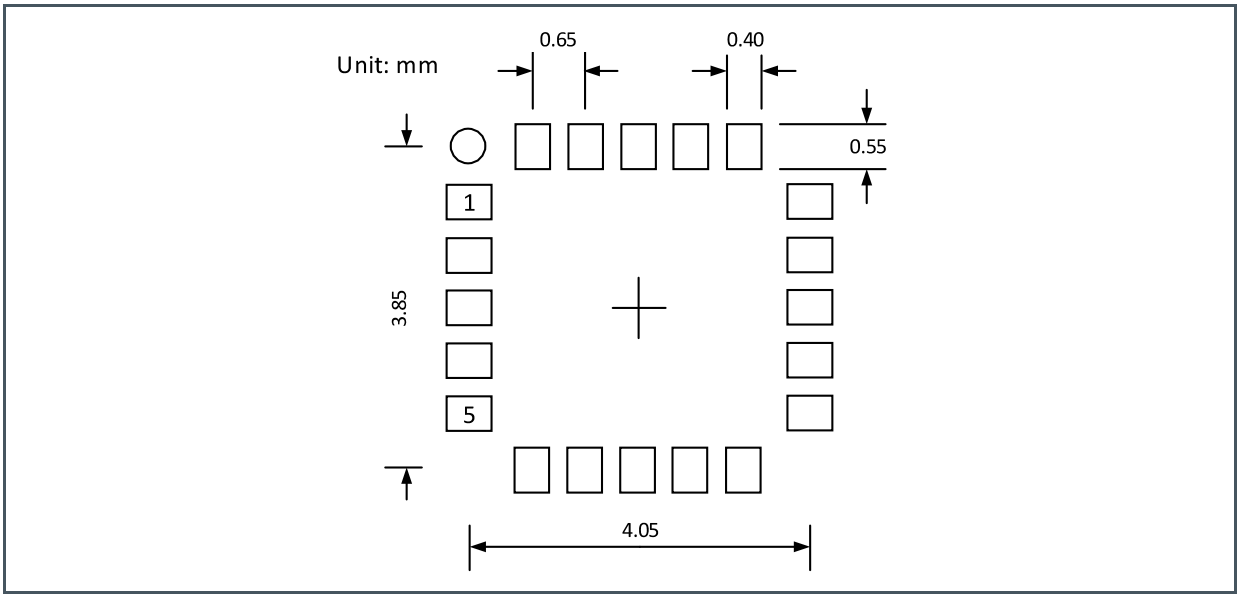
In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7225. An example routing is illustrated in the diagram.

The AS7225 Smart Lighting Integration Kit (SLIK) demo board with schematic and PCB layout documentation is available from **ams** for additional design information.

13.3 PCB Pad Layout

Suggested PCB pad layout guidelines for the LGA package are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 90:
Recommended PCB Pad Layout (Top View)



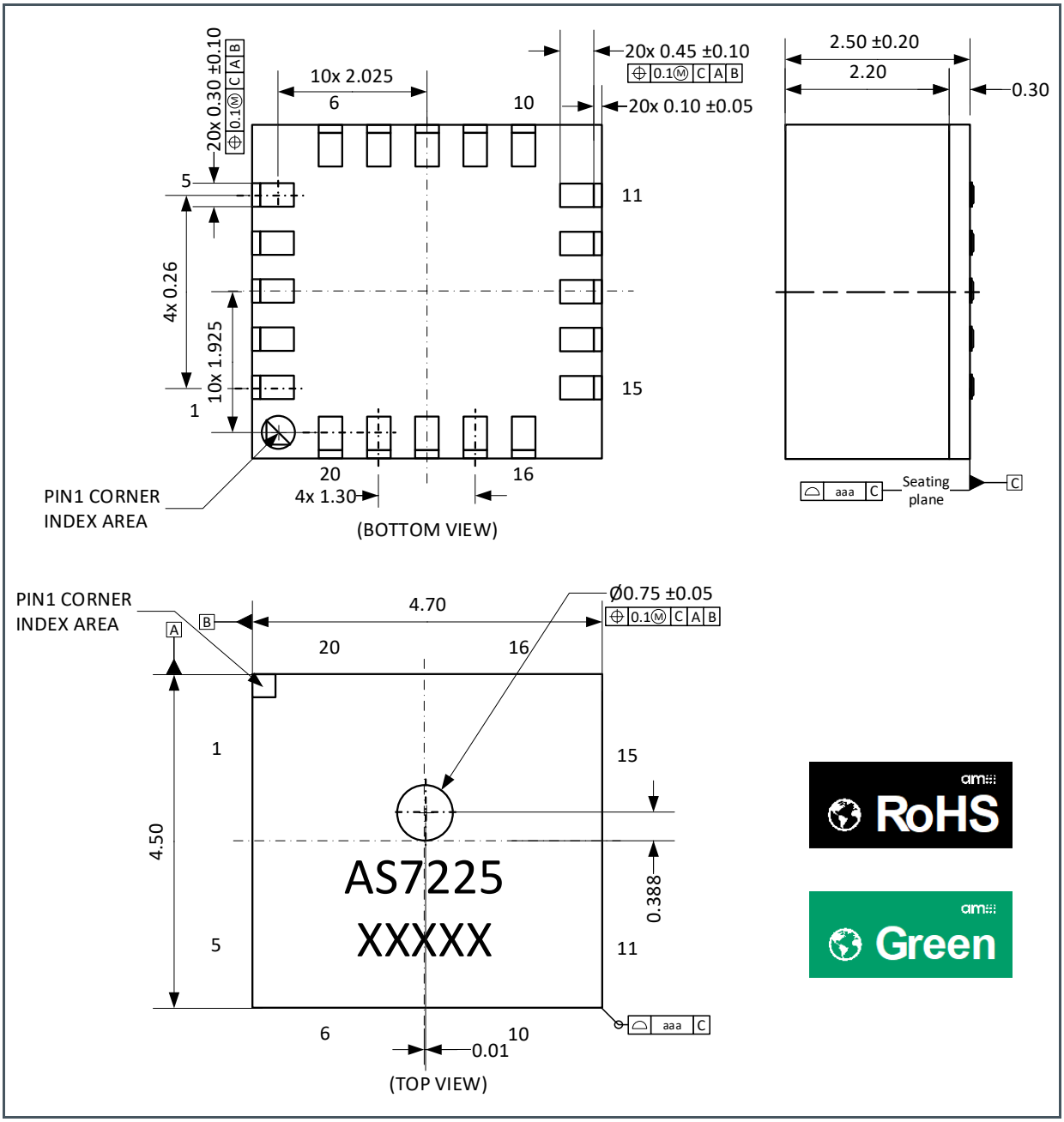
Unless otherwise specified, all dimensions are in millimeters.

Add 0.05mm all around the nominal lead width and length for the PCB pad land pattern.

This drawing is subject to change without notice.

14 Package Drawings & Markings

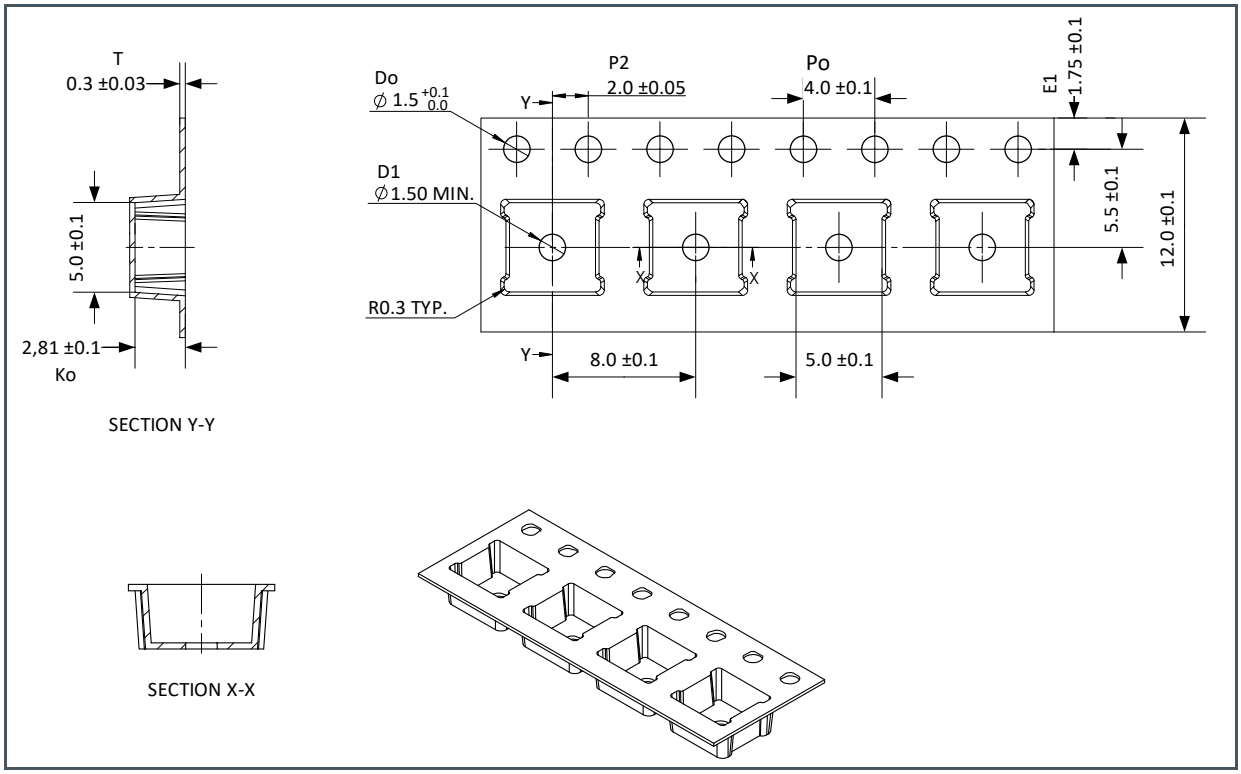
Figure 91:
20-Pin LGA Package Outline Drawing



(3) All dimensions are in millimeters. Angles in degrees.
(4) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(5) N is the total number of terminals.
(6) This package contains no lead (Pb).
(7) This drawing is subject to change without notice.

15 Tape & Reel Information

Figure 92:
Tape Dimensions



(1) All dimensions are in millimeters. Angles in degrees.

(2) Geometric dimensioning and tolerancing conform to ASME Y14.5M-1994.

(3) This drawing is subject to change without notice.

16 Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of the component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 93:
Solder Reflow Profile Graph

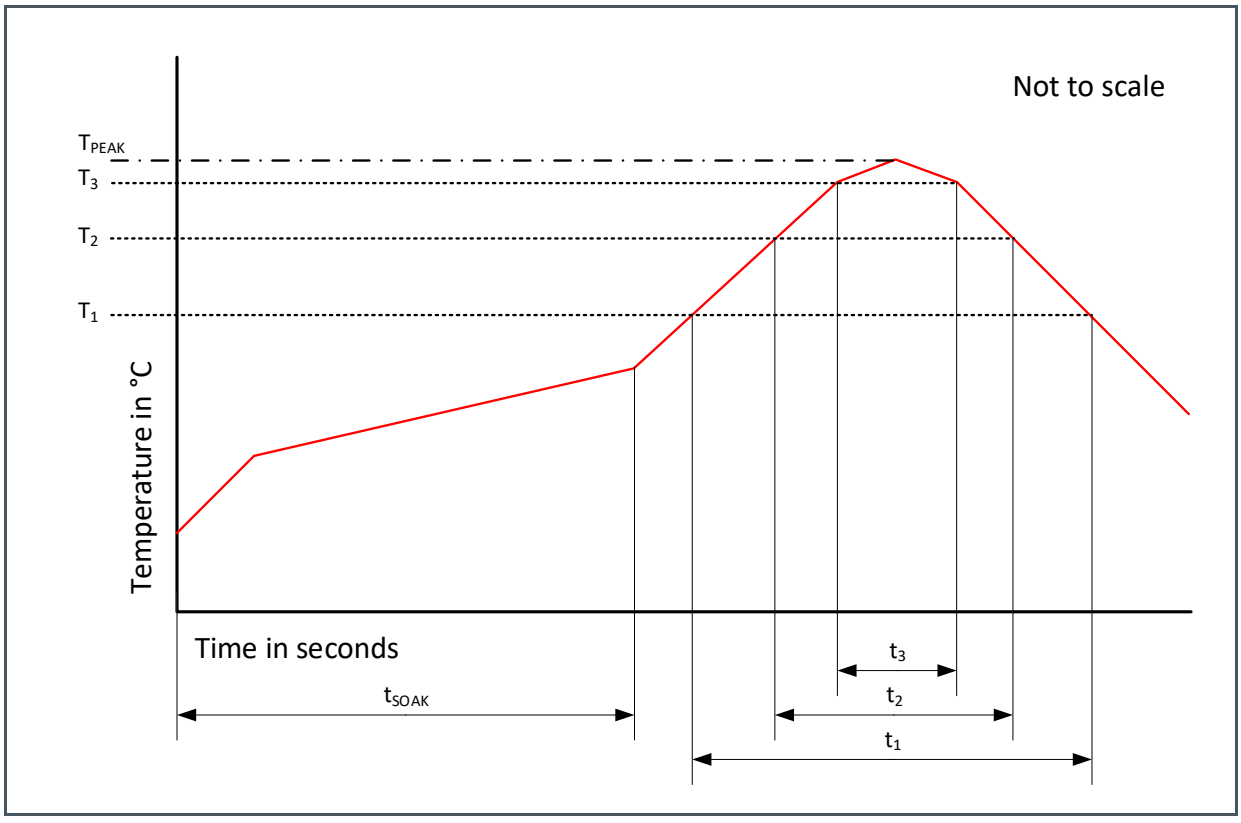


Figure 94:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s

Parameter	Reference	Device
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

16.1 Manufacturing Process Considerations

The AS7225 package is compatible with standard reflow no-clean and cleaning processes including aqueous, solvent or ultrasonic techniques. However, as an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing. Temporary covering of the aperture is allowed. To avoid degradation of accuracy or performance in the end product, care should be taken that any temporary covering and associated sealants/debris are thoroughly removed prior to any optical testing or final packaging.

16.2 Storage Information

Moisture sensitivity optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

16.2.1 Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

16.2.2 Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

16.3 Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

17 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

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1.3 Block Diagram updated	5
2 Ordering Information updated	6
3.1 Pin Diagram updated	7
3.2 Pin Description updated	7, 8
4 Absolute Maximum Ratings updated	9
5 Electrical Characteristics updated	10
6 Optical Characteristics updated	12, 13
7.1 Calibrated XYZ Chromatic Smart Lighting Director – Overview updated	15
7.3.1 Indicator LED updated	16
8.4 I²C Slave Timing Characteristics updated	21
8.6.1 I²C Virtual Registers section headline “XYZ Scale Registers” added	24
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12 Smart Lighting Command Interface chapter added	50
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13.1 Schematic figures 72, 73, 74 updated	57, 58, 59
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- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

18 Legal Information

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