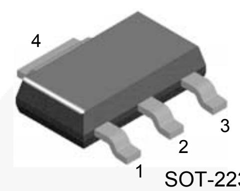
FAIRCHILD

October 2014

NZT560 / NZT560A
NPN Low-Saturation Transistor

Features

- These devices are designed with high-current gain and low-saturation voltage with collector currents up to 3 A continuous.



1. Base   2,4. Collector   3. Emitter

Ordering Information

Part Number	Marking	Package	Packing Method
NZT560	560	SOT-223 4L	Tape and Reel
NZT560A	560A	SOT-223 4L	Tape and Reel

Absolute Maximum Ratings(1),(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	60	V
V_{CBO}	Collector-Base Voltage	80	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current - Continuous	3	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Notes:

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

Thermal Characteristics[3]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Max.	Unit
P_D	Total Power Dissipation	1	W
	Derate Above 25°C	8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	125	°C/W

Note:

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Max.	Unit
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0		60		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 µA, I_E = 0		80		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 µA, I_C = 0		5		V
I_{CBO}	Collector Cut-Off Current	V_{CB} = 30 V, I_E = 0			100	nA
		V_{CB} = 30 V, I_E = 0, T_A = 100°C			10	µA
I_{EBO}	Emitter Cut-Off Current	V_{EB} = 4 V, I_C = 0			100	nA
h_{FE}	DC Current Gain[4]	I_C = 100 mA, V_{CE} = 2 V		70		
		I_C = 500 mA, V_{CE} = 2 V	NZT560	100	300	
			NZT560A	250	550	
		I_C = 1 A, V_{CE} = 2 V		80		
		I_C = 3 A, V_{CE} = 2 V		25		
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage[4]	I_C = 1 A, I_B = 100 mA			300	mV
		I_C = 3 A, I_B = 300 mA	NZT560		450	
			NZT560A		400	
$V_{BE}(sat)$	Base-Emitter Saturation Voltage[4]	I_C = 1 A, I_B = 100 mA			1.25	V
$V_{BE}(on)$	Base-Emitter On Voltage[4]	I_C = 1 A, V_{CE} = 2 V			1	V
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz			30	pF
f_T	Transition Frequency	I_C = 100 mA, V_{CE} = 5 V, f = 100 MHz		75		MHz

Note:

4. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2.0%

Typical Performance Characteristics

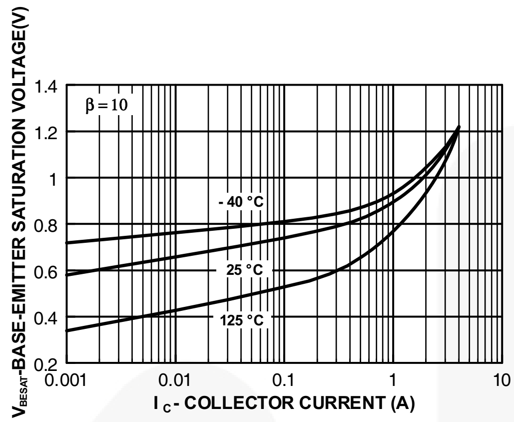


Figure 1. Base-Emitter Saturation Voltage vs. Collector Current

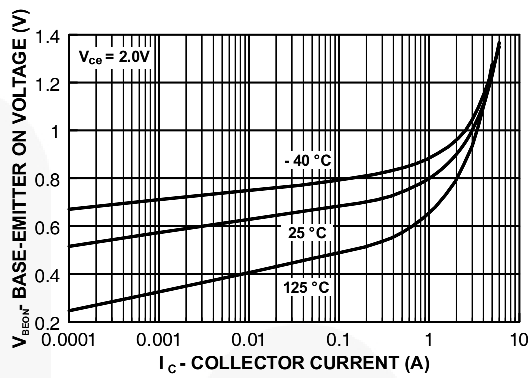


Figure 2. Base-Emitter On Voltage vs. Collector Current

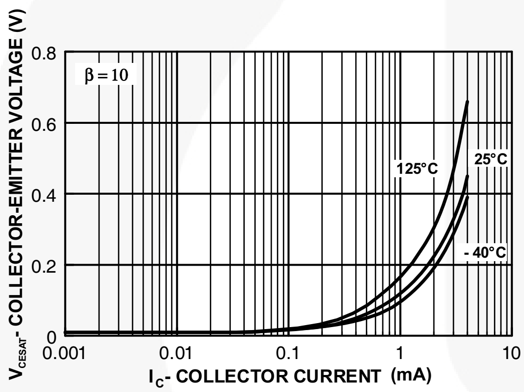


Figure 3. Collector-Emitter Saturation Voltage vs. Collector Current

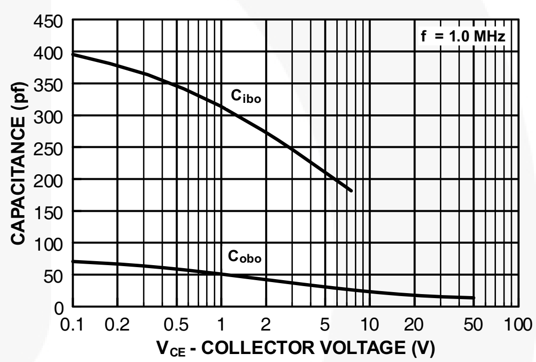


Figure 4. Input / Output Capacitance vs. Reverse Bias Voltage

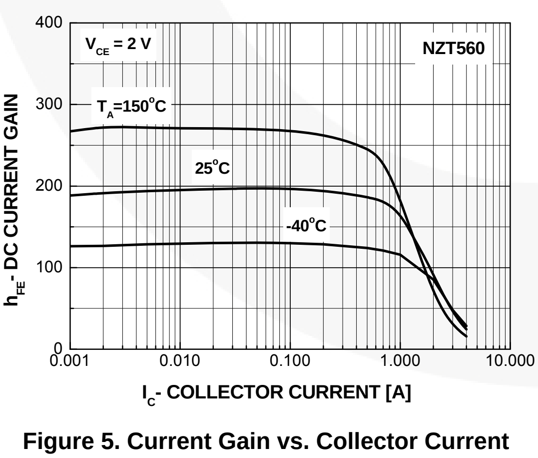


Figure 5. Current Gain vs. Collector Current

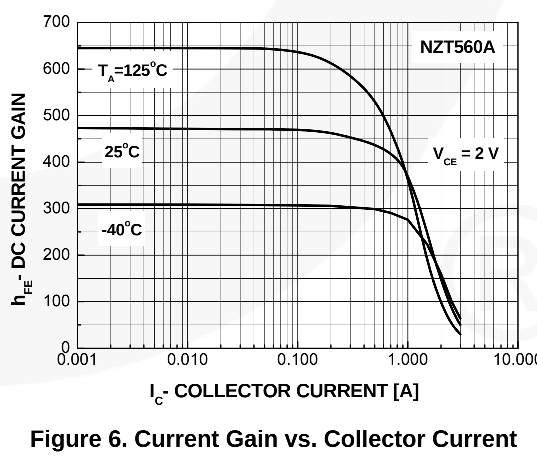
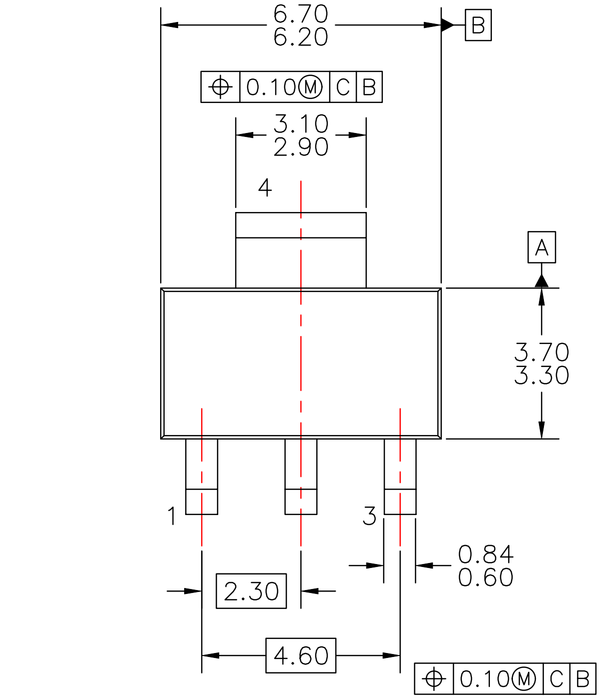


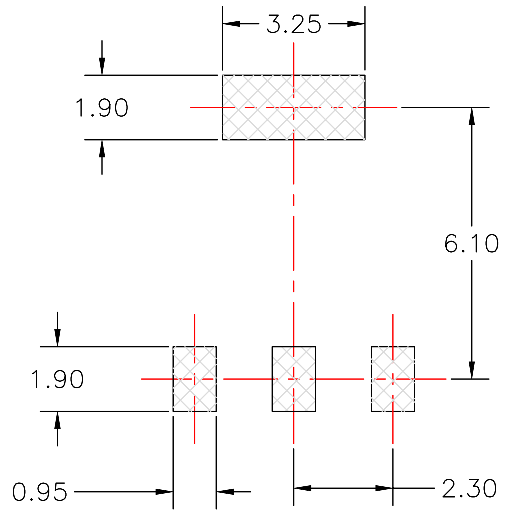
Figure 6. Current Gain vs. Collector Current

APPROVED
July-14-2008

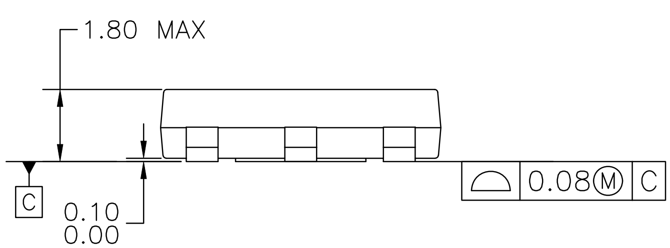
REVISIONS

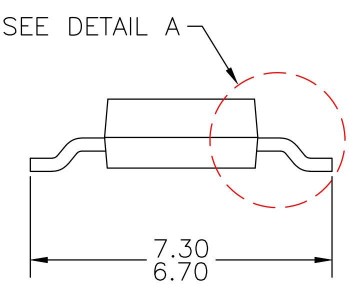
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR $0.74^{+0.05}_{-0.07}$ TO 0.60–0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR $^{1.80}_{1.55}$ TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR $0.3^{+0.02}_{-0.07}$ TO 0.20–0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC: CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR $3.56^{+0.15}_{-0.25}$ TO $^{3.70}_{3.30}$; CHG BODY LN FR $6.5^{+0.2}_{-0.2}$ TO $^{6.70}_{6.20}$; CHG TOTAL PKG WID FR $6.96^{+0.33}_{-0.25}$ TO $^{7.30}_{6.70}$; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP

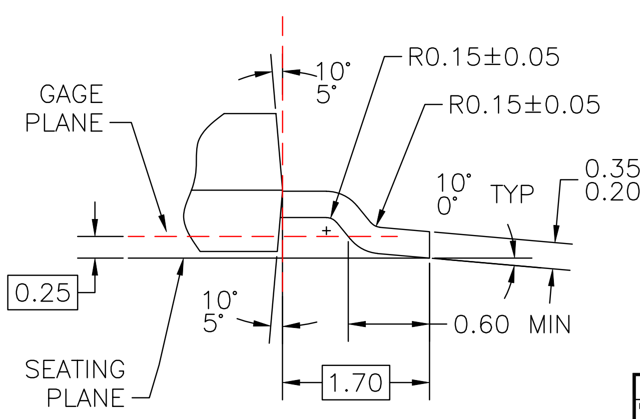




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING BASED ON JEDEC REGISTRATION TO–261, VARIATION AA.
B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
C) ALL DIMENSIONS ARE IN MILLIMETERS.
D) DRAWING CONFORMS TO ASME Y14.5M–1994.
E) LANDPATTERN NAME: SOT230P700X180–4BN
F) DRAWING FILENAME: MKT–MA04AREV2

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	26FEB2008
CHECKED: L.Z. STA CRUZ	
APPROVED: M.R. GESTOLE	
G.S. BAJE	
PROJECTION	

FAIRCHILD SEMICONDUCTOR™

MOLDED PACKAGE
SOT–223, 4 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
1:1	A3	MKT–MA04A	2

FORMERLY: N/A SHEET : 1 OF 1

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