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ON Semiconductor®

# FDC5612

## 60V N-Channel PowerTrench® MOSFET

### General Description

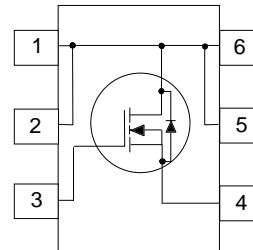
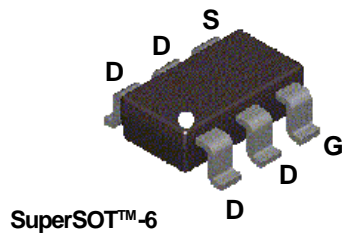
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 4.3 A, 60 V.  $R_{DS(ON)} = 0.055 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.064 \Omega @ V_{GS} = 6 \text{ V}$
- Low gate charge (12.5nC typical).
- Fast switching speed.
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	4.3	A
	Drain Current - Pulsed	20	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.6	W
		0.8	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

### Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.562	FDC5612	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		58		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	2.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}, I_D = 4\text{ A}$		0.042 0.072 0.048	0.055 0.094 0.064	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 4.3\text{ A}$		14		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		650		pF
$C_{oss}$	Output Capacitance			80		pF
$C_{rss}$	Reverse Transfer Capacitance			35		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		11	20	ns
$t_r$	Turn-On Rise Time			8	18	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
$t_f$	Turn-Off Fall Time			6	15	ns
$Q_g$	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 4.3\text{ A},$ $V_{GS} = 10\text{ V}$		12.5	18	nC
$Q_{gs}$	Gate-Source Charge			2.4		nC
$Q_{gd}$	Gate-Drain Charge			2.6		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			1.3		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.75	1.2	V

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.
  - $78^\circ\text{C/W}$  when mounted on a  $1.0\text{ in}^2$  pad of 2 oz. copper.
  - $156^\circ\text{C/W}$  when mounted on a minimum pad.
- Pulse Test: Pulse Width  $\leq 300\text{ ms}$ , Duty Cycle  $\leq 2.0\%$

Typical Characteristics

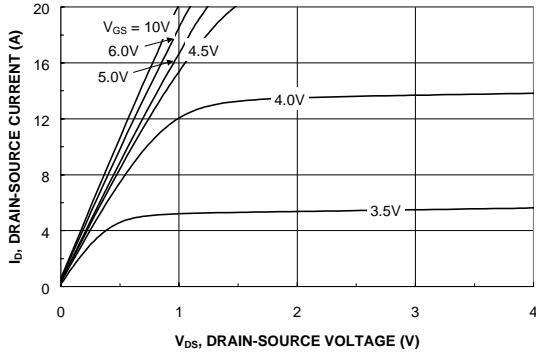


Figure 1. On-Region Characteristics.

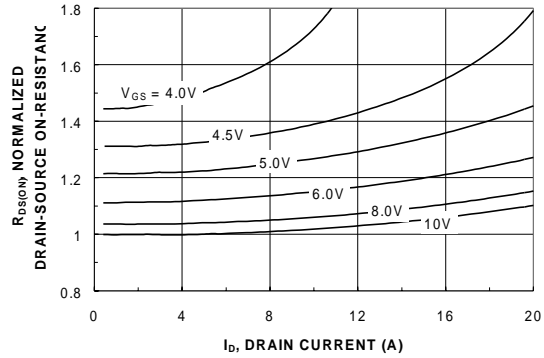


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

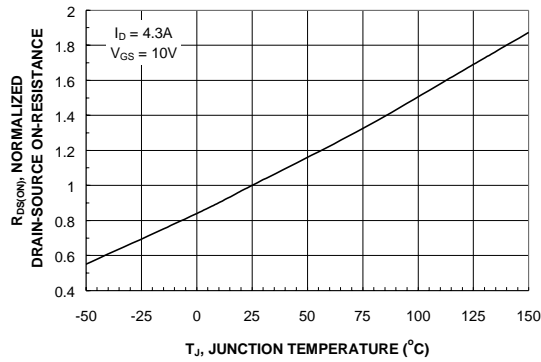


Figure 3. On-Resistance Variation with Temperature.

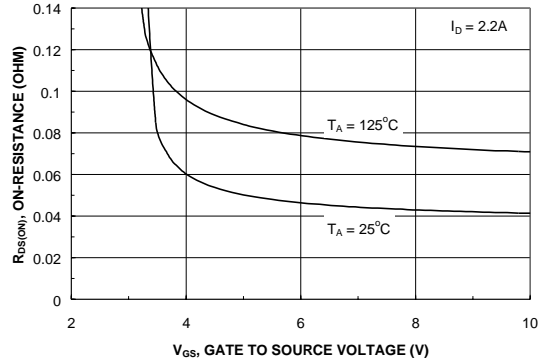


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

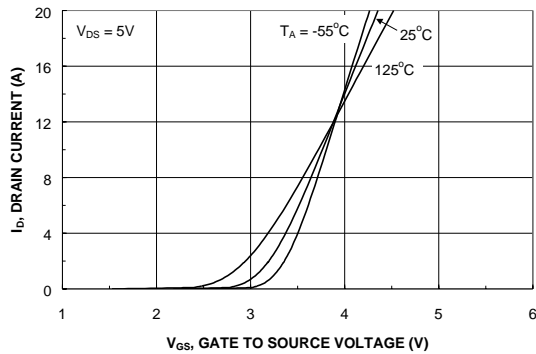


Figure 5. Transfer Characteristics.

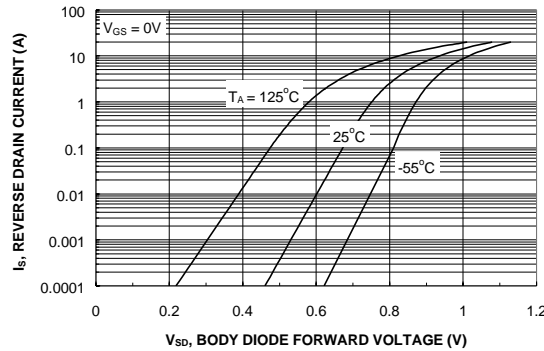
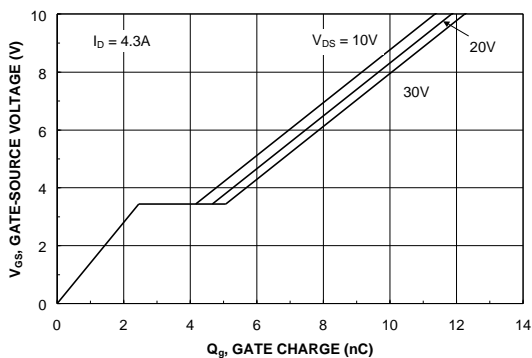
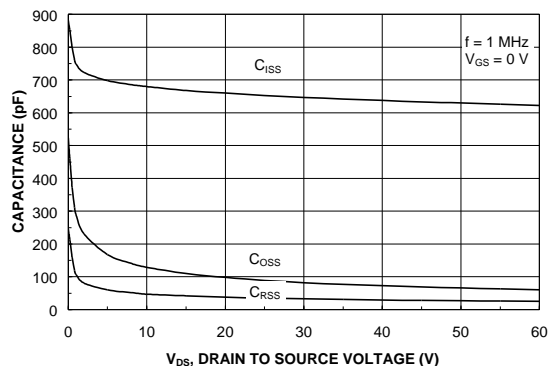


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

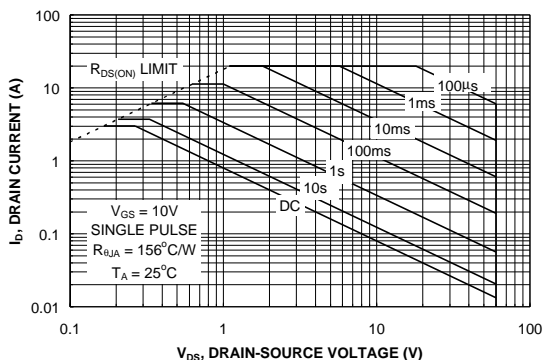
## Typical Characteristics



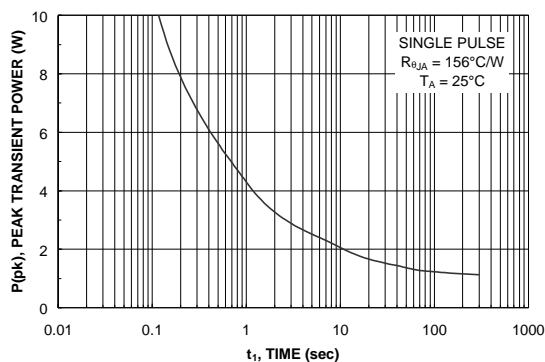
**Figure 7. Gate Charge Characteristics.**



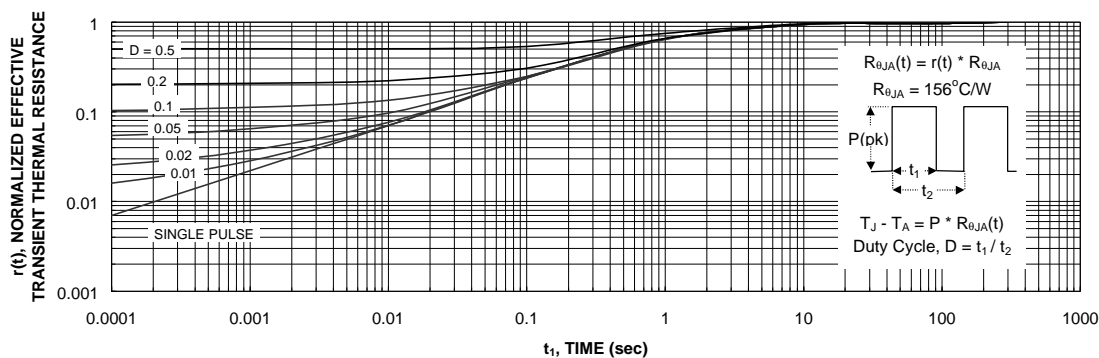
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

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