MCP60821/1U/3

25 MHz Precision Operational Amplifiers

Features

- Gain Bandwidth Product: 25 MHz (typical)
- Slew Rate: 30 V/µs (typical at V_{DD} = 5.5V)
- Total Harmonic Distortion (THD):
  -106 dBc (typical) at 1 kHz and 2 V_{P-P}
- Input Offset Voltage:
  ±50 µV (maximum, V_{CM} = 0.1V)
- Input Offset Voltage Drift:
  ±0.5 µV/°C (maximum, V_{CM} = 0.1V)
- Rail-to-Rail: Input/Output (I/O)
- Power Supply: 2.2V to 5.5V
  - Single or Dual (Split) Supplies
  - Quiescent Current: 2.5 mA/channel (typical)
  - Shutdown Pin (MCP60823 only)
- Enhanced Electromagnetic Interference (EMI) Protection:
  - EMI Rejection Ratio (EMIRR):
    85 dB at 2.4 GHz (typical)
- Extended Temperature Range: -40 °C to +125 °C
- Packaging:
  - 5-Lead SOT-23 (MCP60821 only)
  - 5-Lead SC70 (MCP60821U only)
  - 6-Lead SOT-23 (MCP60823 only)

Typical Applications

- Communications
- Test and Measurement
- Communications
- Medical
- Active Filters
- High Speed Amplifiers
- Wireless Networking
- Analog-to-Digital Converter (ADC) Driver
- Digital-to-Analog Converter (DAC) Buffer

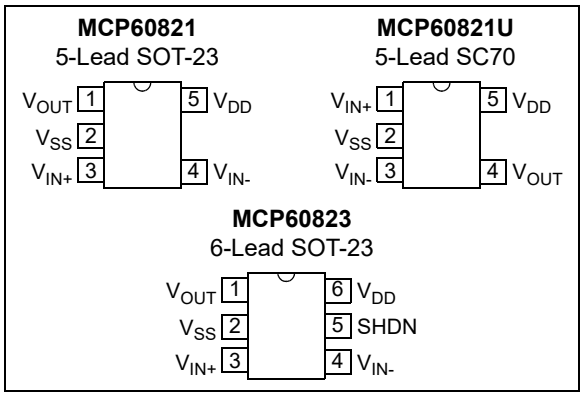
Description

The MCP60821/1U/3 operational amplifiers operate on a power supply voltage between 2.2V and 5.5V over the extended temperature range of -40 °C to +125 °C. The input offset voltage is trimmed at +25 °C and V_{DD} = 3.5V.

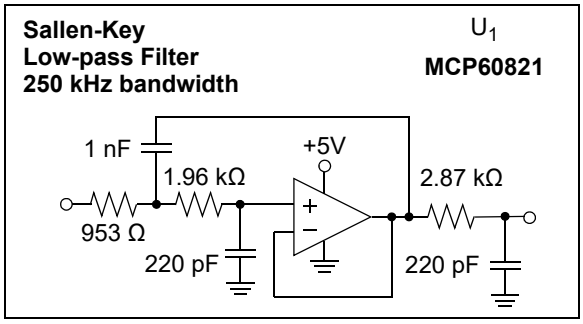
Related Operational Amplifiers

- MCP6051/2/4: 385 kHz, Low Offset Voltage
- MCP6061/2/4: 730 kHz, Low Offset Voltage
- MCP6071/2/4: 1.2 MHz, Low Offset Voltage
- MCP60711/1U/3: 2.5 mA, 10 MHz, Low Offset Voltage
- MCP60811/1U/3: 25 MHz, Low Offset Voltage

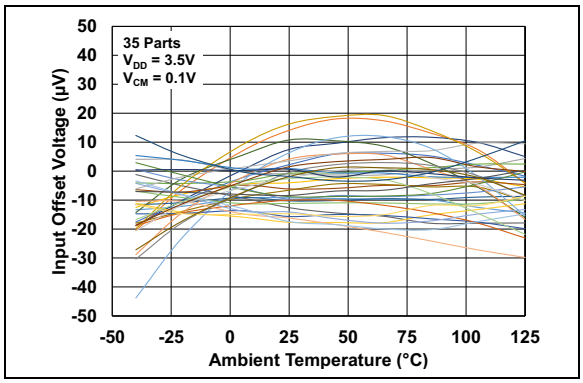
Package Types



Typical Application Circuit



Input Offset Voltage vs. Temperature



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings

$V_{DD} – V_{SS}$ .....-0.3V to +6.0V
Current at Input Pins .....±2 mA
Inputs and Outputs..... V_{SS} – 0.5V to V_{DD} + 0.5V
Input Difference Voltage ($V_{IN+} – V_{IN-}$) ..... (intermittent) ±V_{DD}
.....(continuous) ±0.5V
Output Short Circuit Current.....±60 mA
Current at Output and Supply Pins.....(continuous) ±30 mA
Storage Temperature.....-65 °C to +150 °C
Maximum Junction Temperature .....+150 °C
ESD Protection (HBM, CDM) .....≥ 4 kV, 2 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF. See Figure 1-6.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage						
Input Offset Voltage	V_{OS}	-50	±15	50	µV	V_{CM} = 0.1V, T_A = +5°C
		-60	±20	60		V_{CM} = V_{DD} – 0.5V, T_A = +5°C
		-70	±35	70		V_{CM} = 0.1V, TA = +25°C (Note 3)
		-80	±40	80		V_{CM} = V_{DD} – 0.5V, TA = +25°C (Note 3)
Input Offset Drift with Temperature Coefficient	TC_1	-0.5	±0.08	0.5	µV/°C	T_A = +5°C to +105°C, V_{CM} = 0.1V (Note 3)
		-0.6	±0.1	0.6		T_A = +5°C to +105°C, V_{CM} = V_{DD} – 0.5V (Note 3)
		—	±0.18	—		V_{CM} = 0.1V, T_A = -40°C to +125°C
		—	±0.20	—		V_{CM} = V_{DD} – 0.5V, T_A = -40°C to +125°C
Input Offset Quadratic Temperature Coefficient	TC_2	—	±1.8	—	nV/°C^2	T_A = -40 °C to +125 °C, V_{CM} = 0.1V
		—	±2.3	—		T_A = -40 °C to +125 °C, V_{CM} = V_{DD} – 0.5V
Power Supply Rejection Ratio	PSRR	80	95	—	dB	V_{DD} = 2.2V to 5.5V, V_{CM} = 0.1V
		76	92	—		V_{DD} = 2.2V to 5.5V, V_{CM} = V_{DD} – 0.5V
Input Current and Impedance						
Input Bias Current	I_B	-20	±0.4	20	pA	V_{DD}= 5.5V, V_{CM} = 2.75V, T_A= +25 °C
		—	40	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +85 °C
		—	420	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +125 °C
Input Offset Current	I_{OS}	-20	±1	20	pA	V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +25 °C
		—	±10	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +85 °C
		-400	±180	400		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +125 °C

Note 1: V_{CML}, V_{CMH}, V_{OL} and V_{OH} change with temperature. See Figure 2-19 and Figure 2-21.
2: POR must be on for the time t_{PON_TR} before SHDN function is enabled. It is disabled when POR is off.
3: By design and characterization only; not tested in production.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF. See Figure 1-6.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Current and Impedance (cont.)						
Common Mode Input Impedance	Z_{CM}	—	10^{11}||6.5	—	Ω||pF	
Differential Mode Input Impedance	Z_{DM}	—	10^{11}||2.4	—	Ω||pF	
Input Common Mode Voltage						
Common Mode Voltage Range (Note 1)	V_{CML}	—	-0.4	-0.3	V	T_A = +25 °C
	V_{CMH}	V_{DD} + 0.3	V_{DD} + 0.4	—		T_A = +25 °C
Common Mode Rejection Ratio	CMRR	80	95	—	dB	V_{CM} = -0.3V to V_{DD} + 0.3V
Open-Loop Gain						
DC Open-Loop Gain	A_{OL}	97	112	—	dB	V_{OUT} = 0.2V to V_{DD} – 0.2V, V_{CM} = 0.1V
		97	112	—		V_{OUT} = 0.2V to V_{DD} – 0.2V, V_{CM} = V_{DD} – 0.5V
Output						
Output Voltage Swing – Low (Note 1)	$V_{OL} – V_{SS}$	—	12	—	mV	Input Overdrive = -0.5V, V_{DD} = 2.2V
		—	20	—		Input Overdrive = -0.5V, V_{DD} = 5.5V
		25	115	500		Input Overdrive = -0.5V, V_{DD} = 5.5V, R_L = 200Ω
Output Voltage Swing – High (Note 1)	$V_{OH} – V_{DD}$	—	-10	—		Input Overdrive = 0.5V, V_{DD} = 2.2V
		—	-18	—		Input Overdrive = 0.5V, V_{DD} = 5.5V
		-450	-100	-25		Input Overdrive = 0.5V, V_{DD} = 5.5V, R_L = 200Ω
Output Short Circuit Current	I_{SCP}	—	12	—	mA	V_{DD} = 2.2V
		—	47	—		V_{DD} = 5.5V
	I_{SCM}	—	-18	—		V_{DD} = 2.2V
		—	-57	—		V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.2	—	5.5	V	
Quiescent Current per Amplifier	I_Q	2.2	2.5	2.9	mA	I_O = 0A, t > t_{PON_TR}
	I_{Q_TR}	—	3.3	—		I_O = 0A, t_{PON} < t < t_{PON_TR} (power-on current)
POR Trip Voltages	V_{PRHL}	1.45	1.61	—	V	POR turns off (V_{DD} ↓), V_L = 0V
	V_{PRLH}	—	1.76	1.95		POR turns on (V_{DD} ↑), V_L = 0V
POR Trip Voltage Drift with Temperature	$\Delta V_{PRHL}/\Delta T_A$	—	0.90	—	mV/°C	
	$\Delta V_{PRLH}/\Delta T_A$	—	0.85	—		
Shutdown Logic Threshold, Low	V_{SDL}	0	—	0.55	V	At SHDN pin
Shutdown Logic Threshold, High	V_{SDH}	1.3	—	V_{DD}		
Shutdown Logic Hysteresis	V_{SDHYST}	—	0.12	—		
Shutdown Current per Amplifier	I_{SS_SD}	-15	-4	-1.5	µA	I_O = 0A, t > t_{PON_TR}, SHDN high
Shutdown Pull-Down Resistor	R_{SD}	—	2	—	MΩ	At the SHDN pin

Note 1: V_{CML}, V_{CMH}, V_{OL} and V_{OH} change with temperature. See Figure 2-19 and Figure 2-21.

2: POR must be on for the time t_{PON_TR} before SHDN function is enabled. It is disabled when POR is off.

3: By design and characterization only; not tested in production.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF. See Figure 1-6.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain-Bandwidth Product	GBWP	—	25	—	MHz	V_{OUT} = 0.1 V_{P-P}, G_N > +2 V/V
Full Power Bandwidth	FPBW	—	1.9	—	MHz	V_{DD} = 5V, V_{CM} = 2.5V, V_{OUT} = 4.6 V_{P-P}, Gain = -1 V/V
Phase Margin	PM	—	52	—	°	G = +1 V/V, V_{OUT} = 0.1 V_{P-P}
		—	30	—		G = +1 V/V, V_{OUT} = 0.1 V_{P-P}, C_L = 100 pF
Step Response						
Settling Time	t_{settle}	—	45	—	ns	G = +1 V/V, V_{CM} = 0.5V, +0.1V step and 1% settling
		—	45	—		G = +1 V/V, V_{CM} = V_{DD} – 0.5V, +0.1V step and 1% settling
Slew Rate	SR	—	6.5	—	V/µs	G = +1 V/V, V_{DD} = 2.2V
		—	30	—		G = +1 V/V, V_{DD} = 5.5V
Output Overdrive Recovery Time (Note 1)	t_{ODR}	—	0.37	—	µs	G = -10 V/V, V_{DD} = 3.5V, V_{CM} = V_{DD}/2, ±0.5V output overdrive (V_{IN} = V_{CM} ± 0.225V to V_{CM}), 90% of V_{OUT} change
Noise						
Input Noise Voltage	E_{ni}	—	3.6	—	µV_{P-P}	f = 0.1 Hz to 10 Hz, V_{CM} = 0.1V
		—	6.9	—		f = 0.1 Hz to 10 Hz, V_{CM} = V_{DD} – 0.5V
Input Noise Voltage Density	e_{ni}	—	3.9	—	nV/√Hz	f = 100 kHz, V_{CM} = 0.1V
		—	4.7	—		f = 100 kHz, V_{CM} = V_{DD} – 0.5V
Input Current Noise Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz, V_{CM} = 0.1V
		—	0.6	—		f = 1 kHz, V_{CM} = V_{DD} – 0.5V
Harmonic Distortion – Output Nonlinearity						
Total Harmonic Distortion and Noise	THD+N	—	-106	—	dBc	G_N = +1 V/V, f = 1 kHz, V_{OUT} = 2 V_{P-P}, V_{DD} = 5V, V_{CM} = 2V
EMI Protection						
EMI Rejection Ratio	EMIRR	—	36	—	dB	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	53	—		V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	69	—		V_{IN} = 0.1 V_{PK}, f = 1800 MHz
		—	85	—		V_{IN} = 0.1 V_{PK}, f = 2400 MHz
		—	117	—		V_{IN} = 0.1 V_{PK}, f = 6000 MHz
Shutdown						
Shutdown V_{OUT} Turn On Time	t_{SD_ON}	—	1.2	—	µs	I_O = 0A, V_L = 0V, SHDN = +3.5V to 0V step, 90% of V_{OUT} change (Note 2)
Shutdown V_{OUT} Turn Off Time	t_{SD_OFF}	—	0.2	—		I_O = 0A, V_L = 0V, SHDN = 0V to +3.5V step, 90% of V_{OUT} change (Note 2)
Shutdown Setup Time	t_{SD_SU}	—	0.2	—		Minimum setup time between SHDN events (Note 2)

Note 1: t_{ODR} includes some uncertainty due to clock edge timing.

2: POR must be on for the time t_{PON_TR} before SHDN function is enabled. It is disabled when POR is off. See Section 3.3, Shutdown Digital Input for more details.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF. See Figure 1-6.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Up/Down						
POR Off Time	t_{PRHL}	—	0.4	—	µs	V_L = 0V, V_{DD} = +2.2V to 0V step, 90% of V_{OUT} change, G = +1V/V
POR On Time	t_{PRLH}	—	0.4	—		V_L = 0V, V_{DD} = 0V to 2.2V step, 90% of V_{OUT} change, G = +1V/V
V_{OUT} Power On Time (V_{DD}↑)	t_{PON}	—	9	—		V_{DD} = 0V to +3.5V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of V_{OUT} change, SHDN is low
		—	21	—		V_{DD} = 0V to +3.5V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of V_{OUT} change, SHDN is low, T_A = -40 °C
V_{OUT} Power Off Time (V_{DD}↓)	t_{POFF}	—	0.1	—		V_{DD} = +3.5V to 0V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of V_{OUT} change, SHDN is low
I_Q Power On Time (V_{DD}↑)	t_{PONIQ}	—	8	—		V_{DD} = 0V to +3.5V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of I_Q change, SHDN is low
		—	24	—		V_{DD} = 0V to +3.5V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of I_Q change, SHDN is low, T_A = -40 °C
I_Q Power Off Time (V_{DD}↓)	t_{POFFIQ}	—	0.1	—		V_{DD} = +3.5V to 0V, V_{CM} = 0.1V, V_L = 0V, G = +1 V/V, 90% of I_Q change, SHDN is low
Trim Power On Time (V_{DD}↑) (Note 2)	t_{PON_TR}	—	235	285		Singles, V_{DD} = 0V to +3.5V, V_{CM} = 0.1V, G = +1 V/V, All trims to 100% (time when I_{DD} changes from ≥ I_{Q_TR} to ≥ I_Q), SHDN is disabled until after this time

Note 1: t_{ODR} includes some uncertainty due to clock edge timing.

2: POR must be on for the time t_{PON_TR} before SHDN function is enabled. It is disabled when POR is off. See Section 3.3, Shutdown Digital Input for more details.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +2.2V to +5.5V and V_{SS} = GND.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range		-40	—	+150		(Note 1)
Storage Temperature Range		-65	—	+150		Powered off
Thermal Package Resistances						
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	209	—	°C/W	
Thermal Resistance, 5-Lead SOT-23		—	201	—		
Thermal Resistance, 6-Lead SOT-23		—	191	—		

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature Rating (+150 °C).

1.3 Timing Diagrams

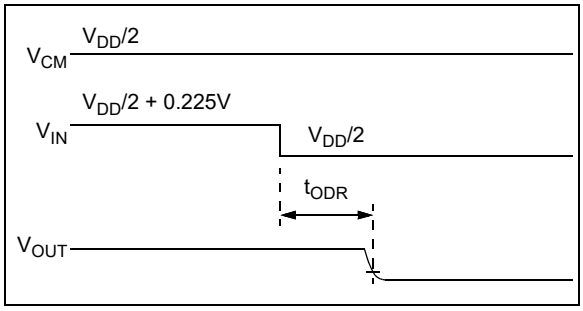


FIGURE 1-1: *Output Overdrive Recovery Timing Diagram.*

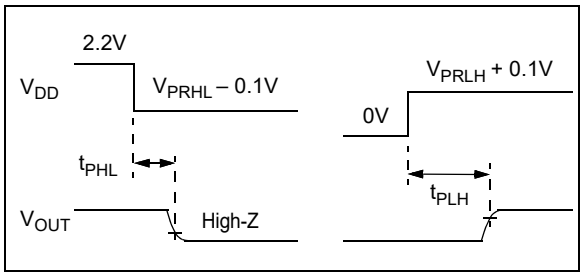


FIGURE 1-2: *POR Timing Diagram.*

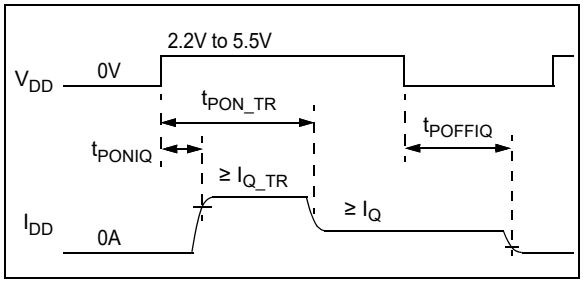


FIGURE 1-3: *Supply Current Power Up/Down Timing Diagram with SHDN Low.*

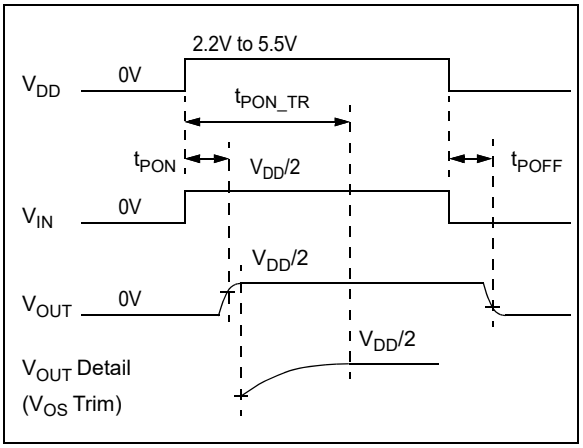


FIGURE 1-4: *Output Voltage Power Up/Down Timing Diagram with V_L = 0V and SHDN Low.*

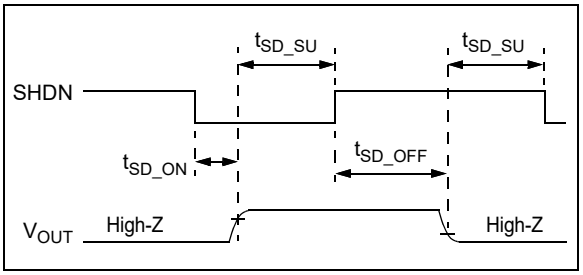


FIGURE 1-5: *SHDN Timing Diagram with 2.2V ≤ V_{DD} ≤ 5.5V (POR must be on for t_{PON_TR} before SHDN is enabled; see Figure 1-3).*

1.4 Test Circuits

Figure 1-6 shows the circuit used for many DC tests. It sets the Common Mode Input Voltage (V_{CM}) and the Output Voltage (V_{OUT}), as shown in Equation 1-1.

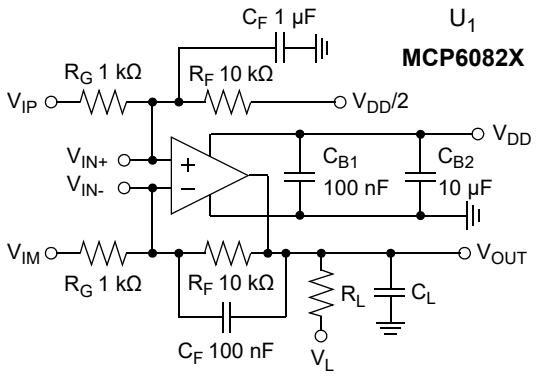


FIGURE 1-6: *DC Bench Test Circuit.*

EQUATION 1-1:

$$G_{DM} = \frac{R_F}{R_G}$$

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2}$$

$$V_{CM} \approx \frac{V_{IP} \cdot G_{DM} + \frac{V_{DD}}{2}}{G_{DM} + 1}$$

$$V_{OST} = V_{IN-} - V_{IN+}$$

$$V_{OUT} = \frac{V_{DD}}{2} + (V_{IP} - V_{IM}) \cdot G_{DM} + V_{OST} \cdot (G_{DM} + 1)$$

Where:

G_{DM}	=	Differential-mode Gain (V/V)
R_F	=	Feedback Resistance (kΩ)
R_G	=	Gain Resistance (kΩ)
V_{CM}	=	Common Mode Input Voltage (V)
V_{IN+}	=	Noninverting Input Voltage (V)
V_{IN-}	=	Inverting Input Voltage (V)
V_{IP}	=	Positive Signal Input (V)
V_{DD}	=	Supply Voltage (V)
V_{OST}	=	Total Input Offset Voltage (mV)
V_{OUT}	=	Output Voltage (V)
V_{IM}	=	Negative Signal Input (V)

The total Input Offset Voltage (V_{OST}) includes the input offset voltage (V_{OS}) and temperature, Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR) and DC Open-Loop Gain (A_{OL}) effects. V_{CM} is the operational amplifier's common mode input voltage. The circuit's common mode input voltage is V_{CMX}, as shown in Equation 1-2.

EQUATION 1-2:

$$V_{CMX} = \frac{V_{IP} + V_{IM}}{2}$$

Where:

V_{CMX}	=	Common Mode Input Voltage (V)
V_{IP}	=	Positive Signal Input (V)
V_{IM}	=	Negative Signal Input (V)

Figure 1-7 shows the circuit used for many AC tests. Ground V_{IM} to make the gain noninverting or ground V_{IP} to make the gain inverting. Keep the operational amplifier stable and fast by making the R-C poles caused by the input capacitances faster than the designed bandwidth (see Equation 1-3).

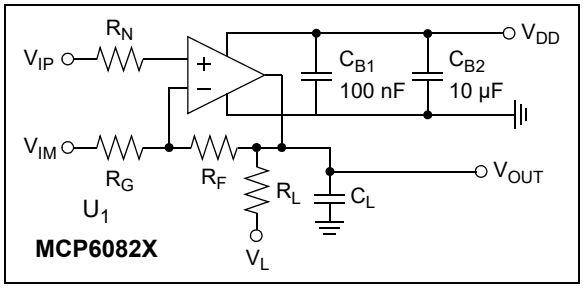


FIGURE 1-7: *AC Bench Test Circuit.*

EQUATION 1-3:

$$G_N = 1 + \frac{R_F}{R_G}$$

$$f_{BW} \approx \frac{GBWP}{G_N}, \text{ where } G_N > +2$$

$$\text{For Speed: } R_N < \frac{1}{4\pi f_{BW} \cdot (C_{CM} + C_{DM})}$$

$$\text{For Stability: } R_F \| R_G < \frac{1}{4\pi f_{BW} \cdot (C_{CM} + C_{DM})}$$

Where:

G_N	=	Noise Gain (V/V)
R_F	=	Feedback Resistance (kΩ)
R_G	=	Gain Resistance (kΩ)
f_{BW}	=	Bandwidth Frequency (MHz)
$GBWP$	=	Gain-Bandwidth Product (MHz)
R_N	=	Noise Resistance (Ω)
C_{CM}	=	Common Mode Input Capacitance (pF)
C_{DM}	=	Differential Mode Input Capacitance (pF)

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

2.1 DC Input Precision

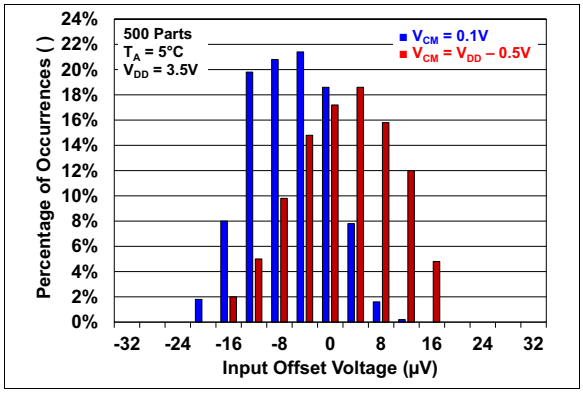


FIGURE 2-1: *Input Offset Voltage.*

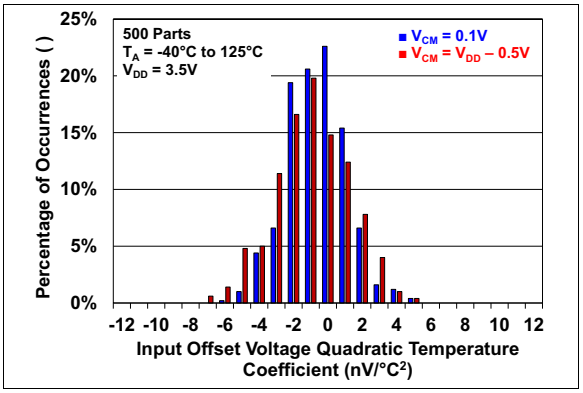


FIGURE 2-3: *Input Offset Voltage Quadratic Temperature Coefficient.*

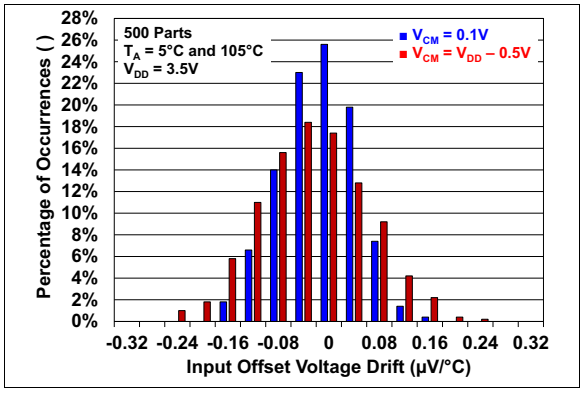


FIGURE 2-2: *Input Offset Voltage Drift.*

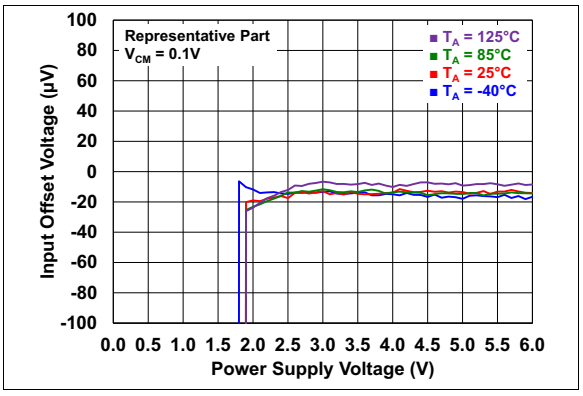


FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0.1V.*

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

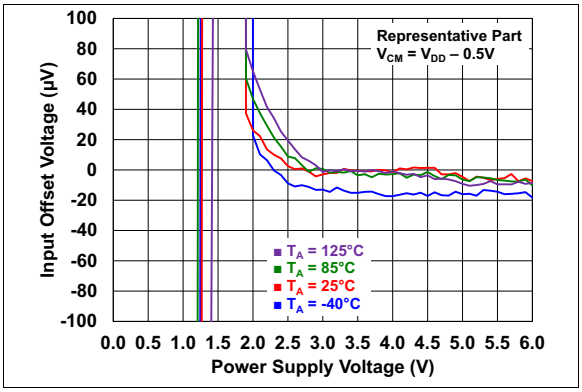


FIGURE 2-5: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} – 0.5V.*

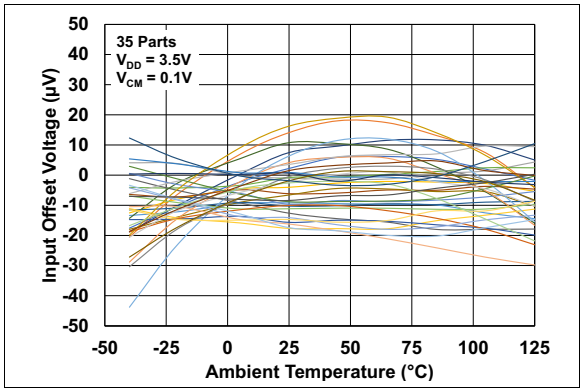


FIGURE 2-8: *Input Offset Voltage vs. Temperature, with V_{DD} = 3.5V and V_{CM} = 0.1V.*

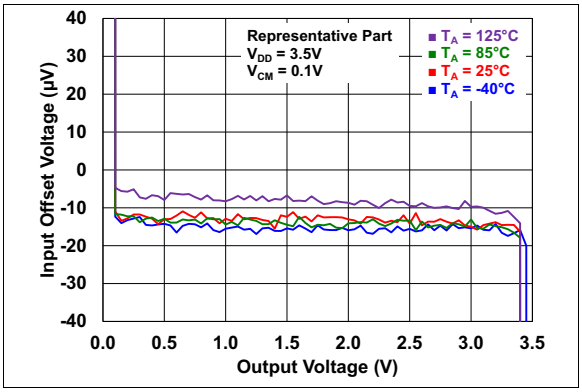


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage, with V_{DD} = 3.5V.*

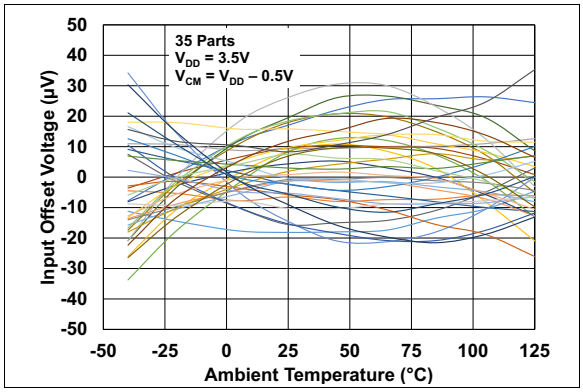


FIGURE 2-9: *Input Offset Voltage vs. Temperature, with V_{DD} = 3.5V, V_{CM} = V_{DD} – 0.5V.*

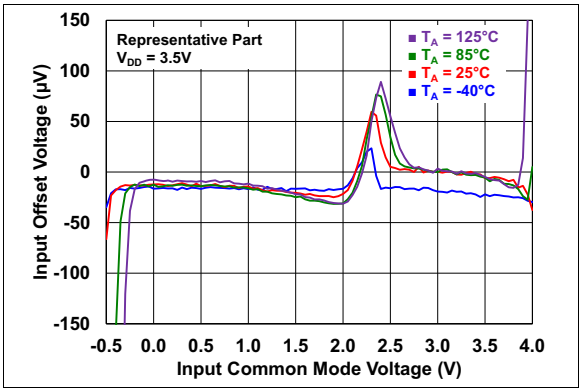


FIGURE 2-7: *Input Offset Voltage vs. Input Common Mode Voltage, with V_{DD} = 3.5V.*

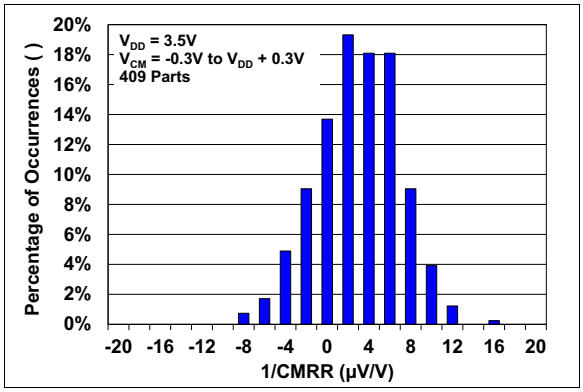


FIGURE 2-10: *Common Mode Rejection Ratio, with V_{DD} = 3.5V.*

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

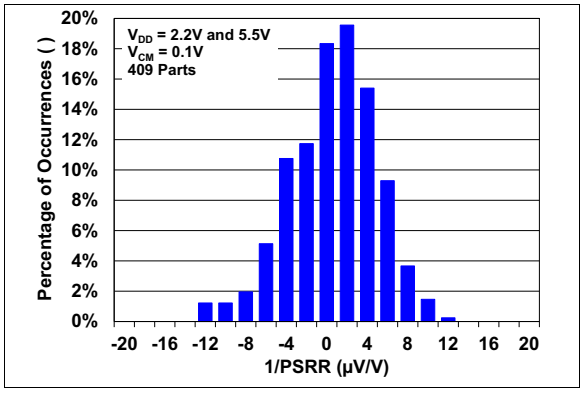


FIGURE 2-11: *Power Supply Rejection Ratio, with V_{CM} = 0.1V.*

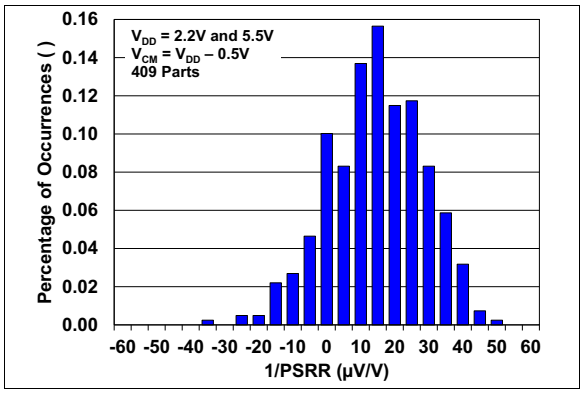


FIGURE 2-12: *Power Supply Rejection Ratio, with V_{CM} = V_{DD} – 0.5V.*

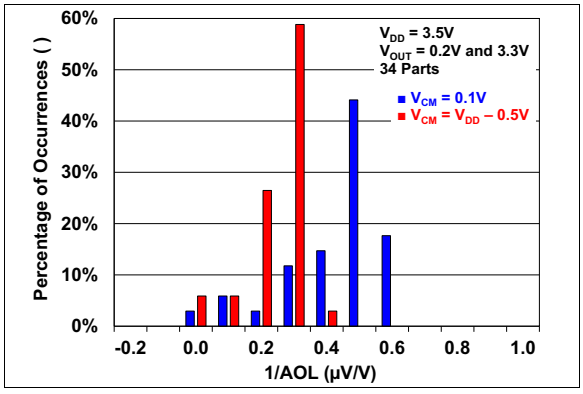


FIGURE 2-13: *DC Open-Loop Gain, with V_{CM} = 0.1V and V_{DD} – 0.5V.*

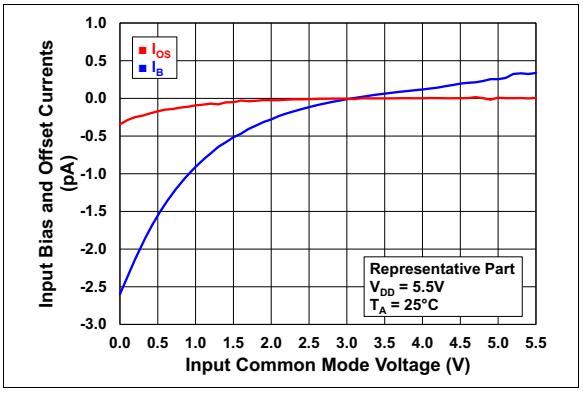


FIGURE 2-14: *Input Bias and Offset Currents vs. V_{CM}, with T_A = 25 °C.*

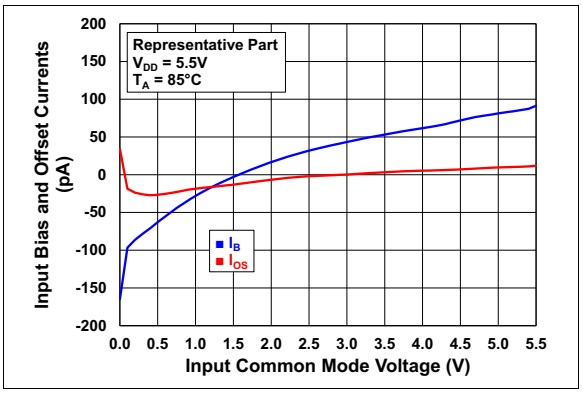


FIGURE 2-15: *Input Bias and Offset Currents vs. V_{CM}, with T_A = 85 °C.*

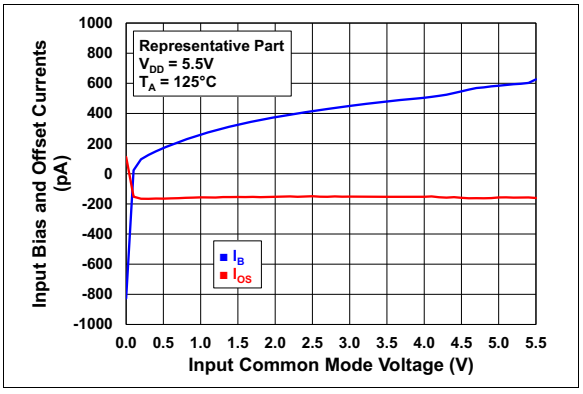


FIGURE 2-16: *Input Bias and Offset Currents vs. V_{CM}, with T_A = 125 °C.*

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

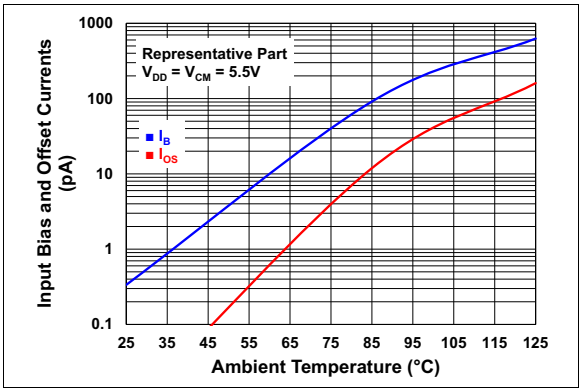


FIGURE 2-17: *Input Bias and Offset Currents vs. Ambient Temperature, with V_{DD} = 5.5V.*

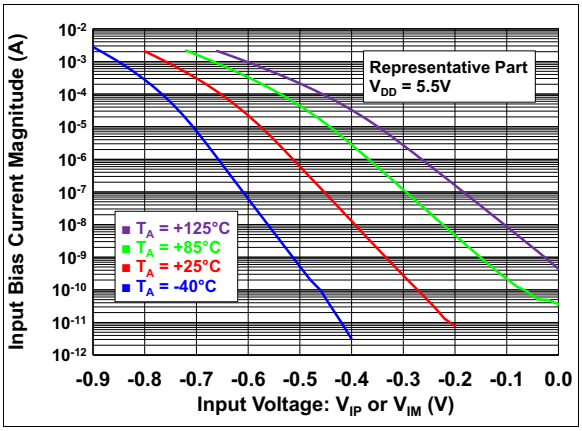


FIGURE 2-18: *Input Bias Current vs. Input Voltage (below V_{SS}).*

2.2 Other DC Voltages and Currents

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

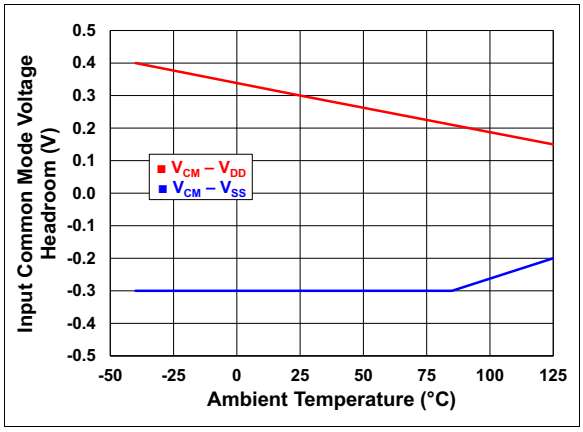


FIGURE 2-19: *V_{CM} Headroom (Range) vs. Ambient Temperature.*

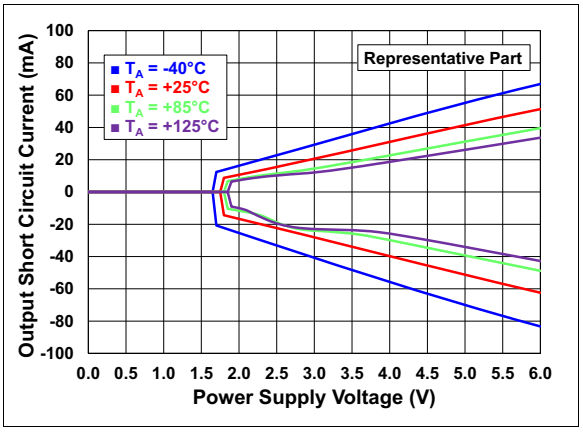


FIGURE 2-22: *Output Short Circuit Current vs. Power Supply Voltage.*

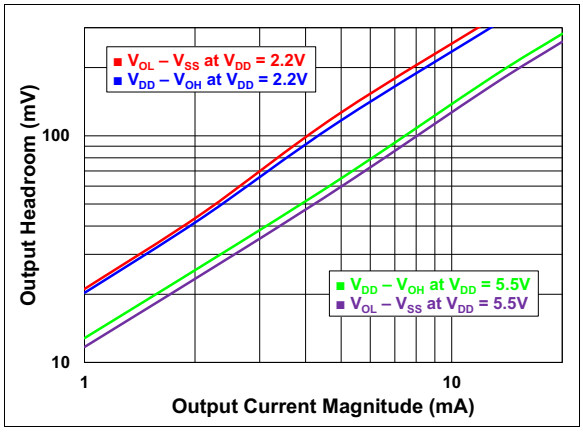


FIGURE 2-20: *Output Voltage Headroom vs. Output Current.*

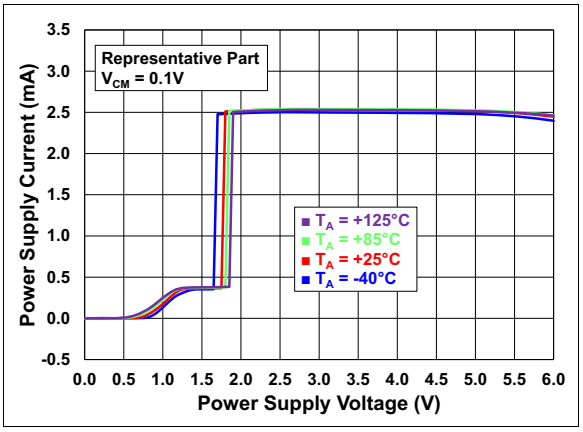


FIGURE 2-23: *Power Supply Current vs. Power Supply Voltage.*

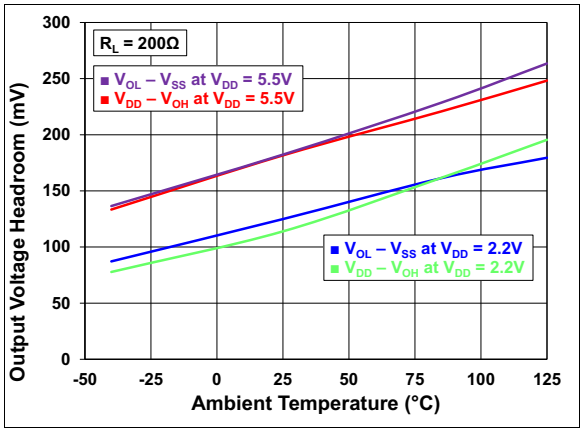


FIGURE 2-21: *Output Voltage Headroom vs. Ambient Temperature.*

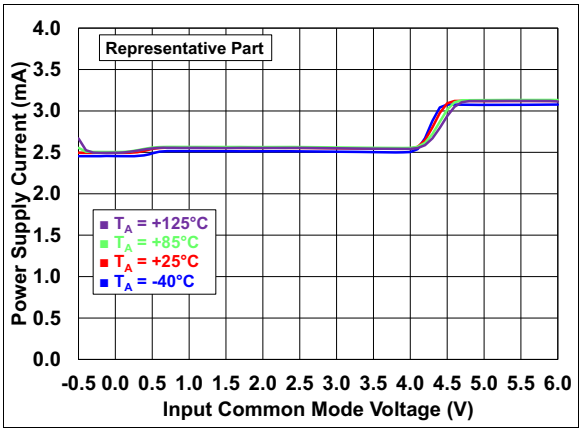


FIGURE 2-24: *Supply Current vs. V_{CM}, with V_{DD}=5.5V.*

2.3 Frequency Response

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

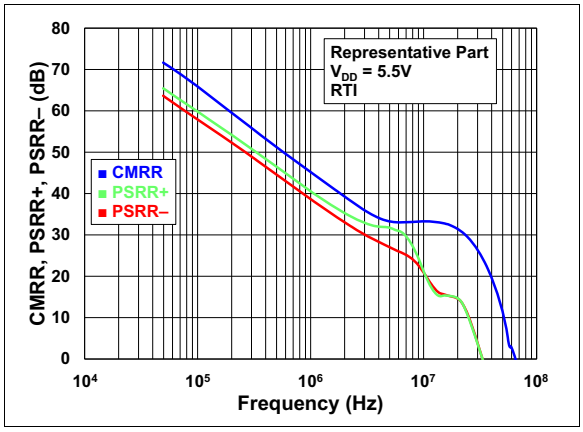


FIGURE 2-25: *CMRR and PSRR vs. Frequency.*

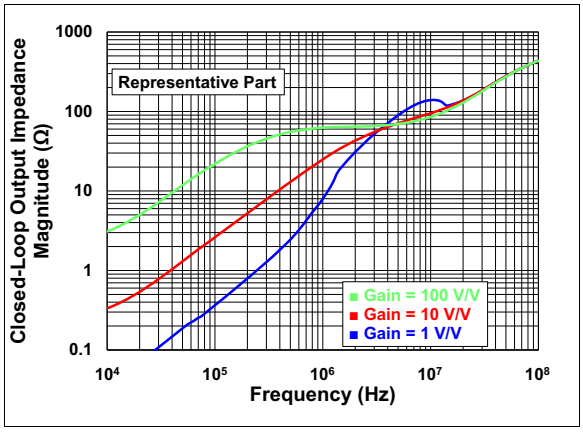


FIGURE 2-28: *Closed-Loop Output Impedance vs. Frequency.*

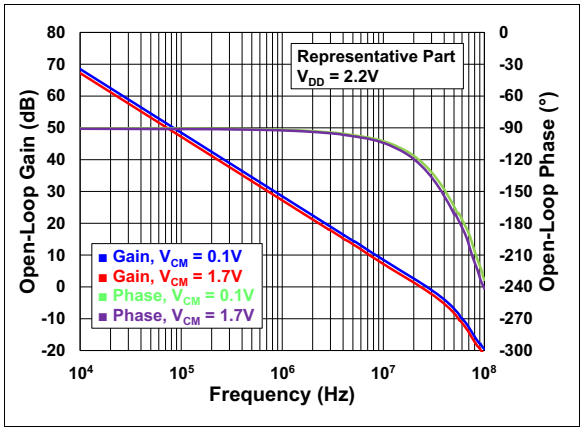


FIGURE 2-26: *Open-Loop Gain vs. Frequency, with V_{DD} = 2.2V.*

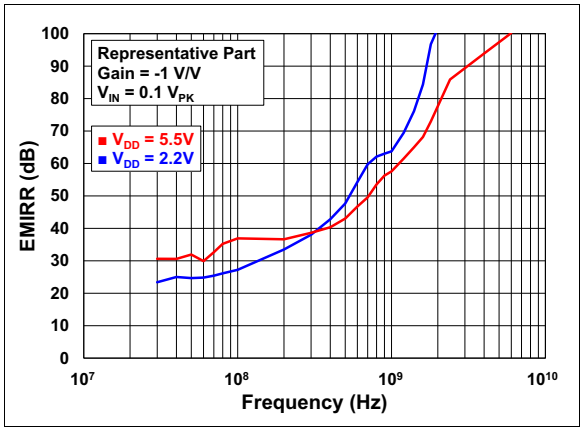


FIGURE 2-29: *EMIRR vs. Frequency.*

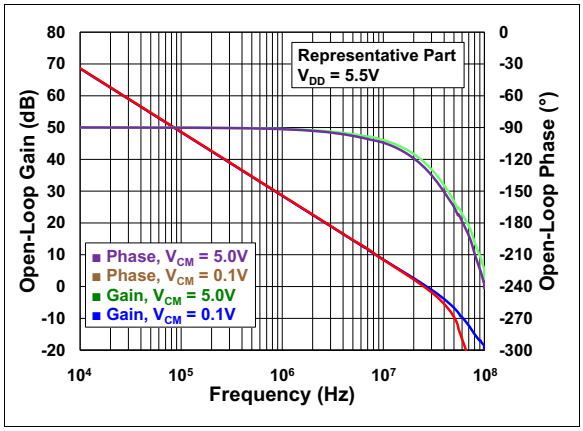


FIGURE 2-27: *Open-Loop Gain vs. Frequency, with V_{DD} = 5.5V.*

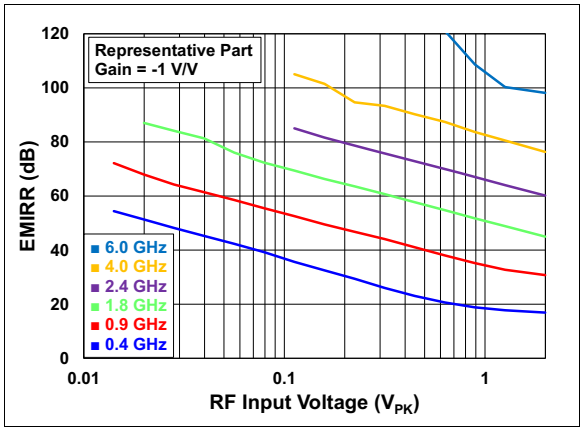


FIGURE 2-30: *EMIRR vs. RF Input Voltage.*

2.4 Input Noise and Distortion

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

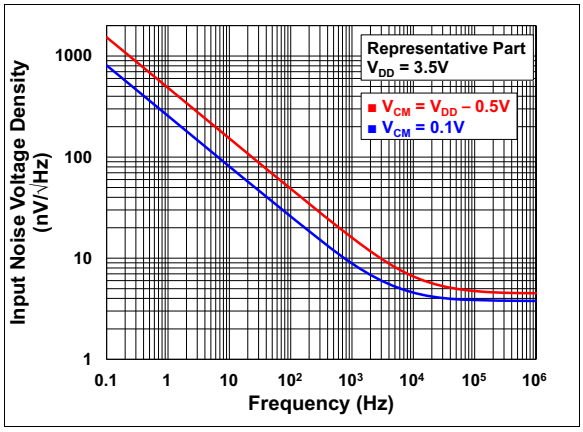


FIGURE 2-31: *Input Noise Voltage Density vs. Frequency.*

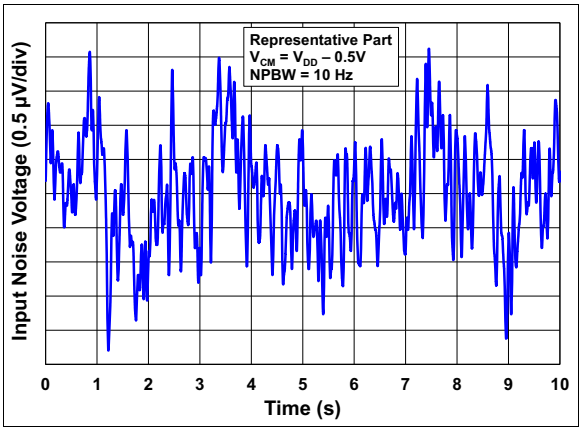


FIGURE 2-33: *Input Noise vs. Time, with a 0.1 Hz to 10 Hz Band-pass Filter and V_{CM} = V_{DD} – 0.5V.*

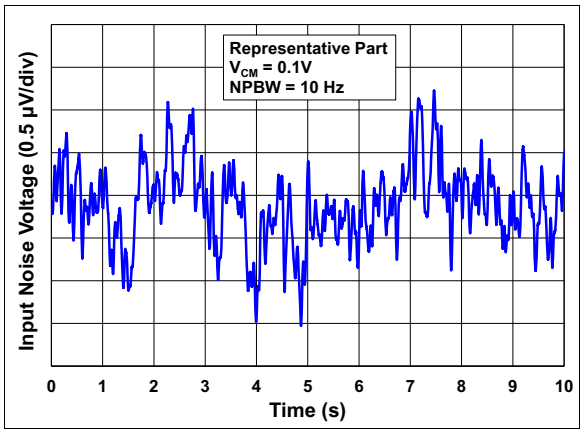


FIGURE 2-32: *Input Noise vs. Time, with a 0.1 Hz to 10 Hz Band-pass Filter and V_{CM} = 0.1V.*

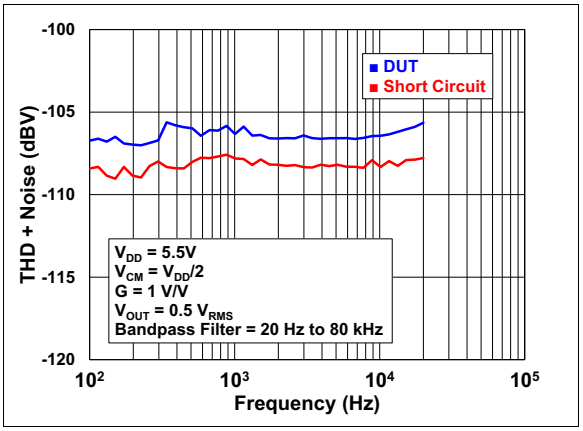


FIGURE 2-34: *Total Harmonic Distortion (THD) + Noise vs. Frequency.*

2.5 Time Response

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

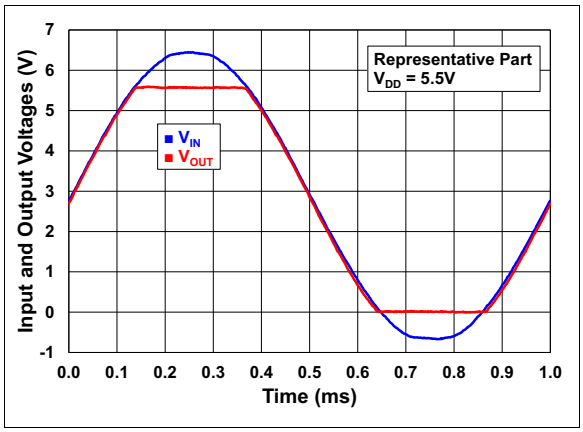


FIGURE 2-35: *MCP60821/1U/3 Shows no Input Phase Reversal with Overdrive.*

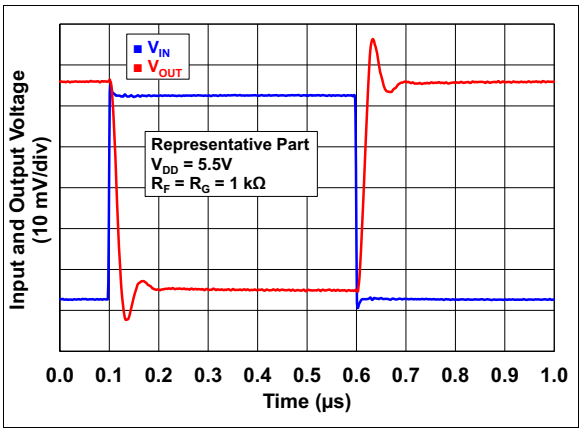


FIGURE 2-38: *Inverting Small Signal Step Response.*

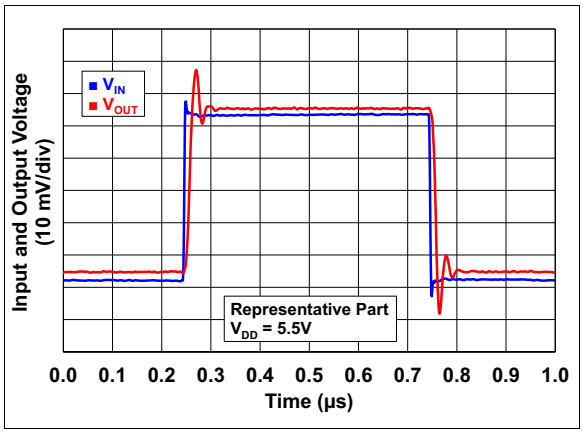


FIGURE 2-36: *Noninverting Small Signal Step Response.*

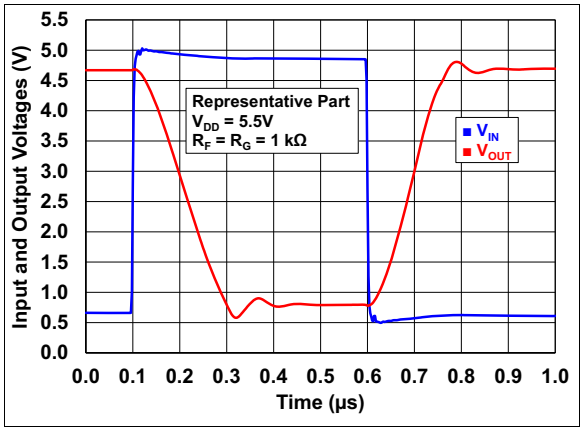


FIGURE 2-39: *Inverting Large Signal Step Response.*

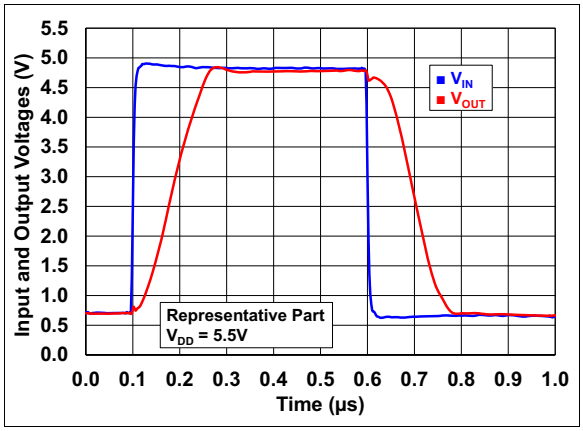


FIGURE 2-37: *Noninverting Large Signal Step Response.*

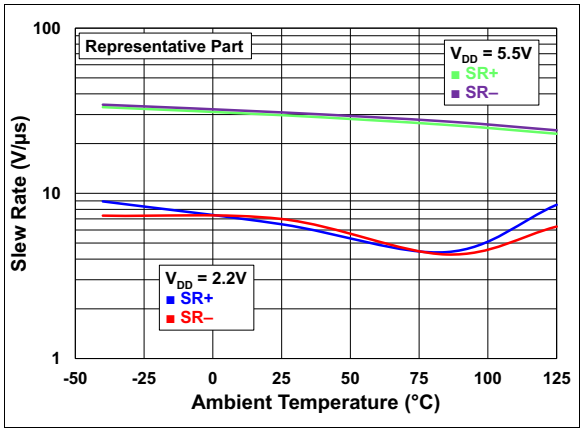


FIGURE 2-40: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

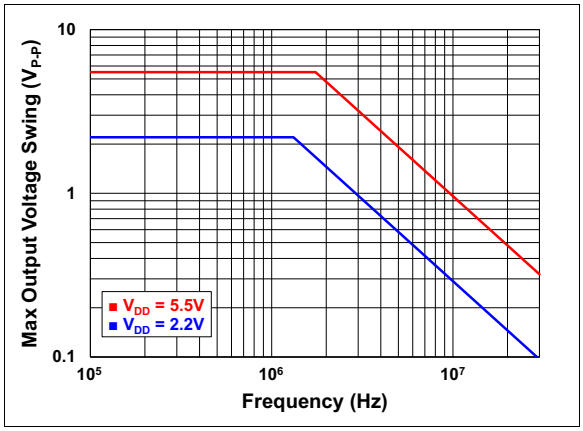


FIGURE 2-41: *Maximum Output Voltage Swing vs. Frequency.*

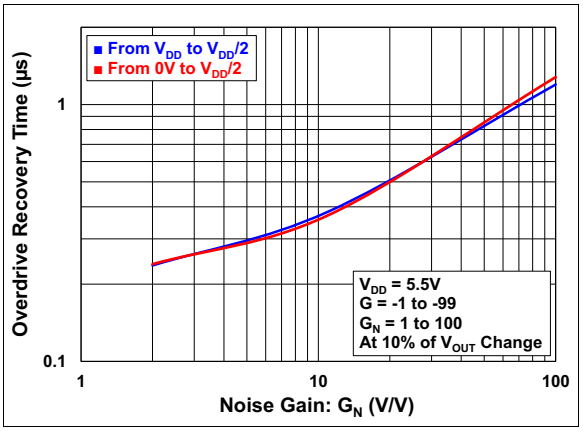


FIGURE 2-42: *Output Overdrive Recovery Time vs. Noise Gain.*

2.6 Capacitive Loads

Note: Unless otherwise indicated, T_A = 25 °C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 2 kΩ to V_L and C_L = 20 pF.

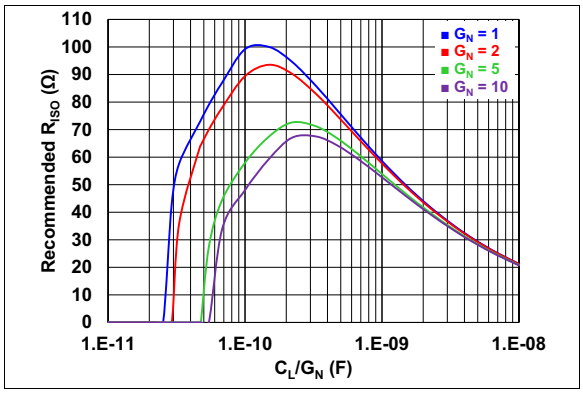


FIGURE 2-43: *Recommended R_{ISO} vs. Normalized Capacitive Load (see Section 4.2.4, Stabilizing Amplifier Circuits).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP60821	MCP60821U	MCP60823	Symbol	Description
SOT-23	SC70	SOT-23		
1	4	1	V_{OUT}	Output
4	3	4	V_{IN-}	Inverting Input
3	1	3	V_{IN+}	Noninverting Input
5	5	6	V_{DD}	Positive Power Supply
2	2	2	V_{SS}	Negative Power Supply
—	—	5	SHDN	Shut Down

3.1 Analog Outputs

Output pin is a low-impedance voltage source.

3.2 Analog Inputs

Noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Shutdown Digital Input

This is a CMOS, Schmitt-triggered input that places MCP6082X into a Low-Power standby mode. The internal trim values are kept active, but the operational amplifier is disabled. Power-on Reset (POR) must be on (power is up) for t_{PON_TR}, to read out the internal registers (the part is on and SHDN is disabled during this time). Once the read out is complete, the part's operation mode depends on SHDN pin. This cycle starts again if POR goes low.

3.4 Power Supply Pins

For normal operation, the positive power supply (V_{DD}) is from 2.2V to 5.5V higher than the negative power supply (V_{SS}). Also, the output voltage (V_{OUT}) is between V_{SS} and V_{DD}, while the common mode input voltage (V_{CM}) range is larger (see V_{CML} and V_{CMH} specifications and Figure 2-19).

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} needs a bypass capacitor.

Dual (or split) supply configurations connect the V_{DD} and V_{SS} pins to their respective supply voltages. The supply also has a circuit ground connection. Both V_{DD} and V_{SS} need bypass capacitors.

4.0 APPLICATION INFORMATION

The MCP6082X family of operational amplifiers is manufactured using a state-of-the-art complementary metal-oxide semiconductor (CMOS) process and is specifically designed for low-cost, high speed and DC precision.

4.1 Operational Amplifier Operation

4.1.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are independent of each other. All of them must be enforced by the user. Being at, or near, two or more absolute maximum ratings at the same time may decrease MCP6082X reliability. For more details, see Section 1.1, Absolute Maximum Ratings.

4.1.2 RAIL-TO-RAIL INPUTS

4.1.2.1 Phase Reversal

MCP6082X is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-35 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2.2 Input Voltage and Current Limits

Electrostatic discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was selected to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than a single diode drop below V_{SS} or more than a single diode drop above V_{DD}.

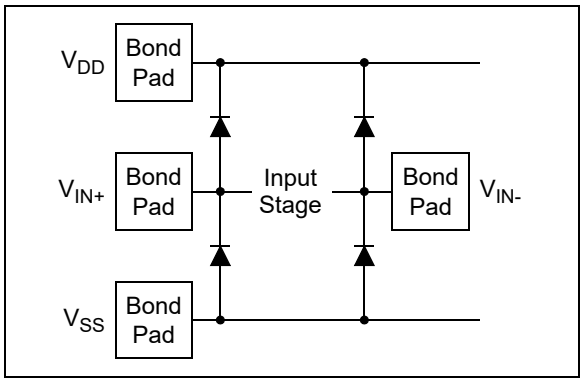


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

To prevent damage and/or improper operation of the MCP6082X amplifiers, the circuit must limit the currents (and voltages) at the input pins (see Section 1.1, Absolute Maximum Ratings). Figure 4-2 shows the recommended approach to protecting these inputs. Resistors R_1 and R_2 limit the possible currents at the input pins.

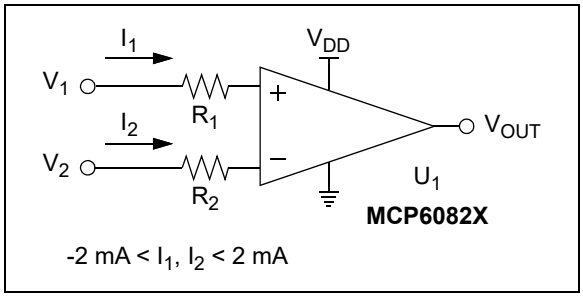


FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs (through the ESD diodes) when V_{CM} is below V_{SS} (see Figure 2-18).

The differential input voltage ($V_{DM} = V_{IN+} – V_{IN-}$) needs to be limited for normal operations. Keep its magnitude below 0.5V. Reasons that this limit may be exceeded include operating voltages outside of their operating limits and input signals with very fast rise or fall rates.

4.1.3 INPUT ERRORS

The input offset voltage (V_{OS}) is trimmed at V_{CM} = 0.1V and $V_{CM} = V_{DD} – 0.5V$, which gives good V_{OS} and CMRR.

Reducing stresses (mechanical, thermal and electrical) improves input offset aging. This benefits applications with long lifetimes and calibration requirements benefit.

The input bias current (I_B) and input offset current (I_{OS}) are low across temperature. They support many applications.

4.1.4 RAIL-TO-RAIL OUTPUTS

4.1.4.1 Output Voltage Limits

Figure 2-20 and Figure 2-21 show typical values of output headroom versus output current and temperature. Figure 2-42 shows the output overdrive versus temperature behavior of these parts.

4.1.4.2 Output Current Limits

Large output currents, in some cases, may increase the internal junction temperature (T_J) of the output stage too high. For reliable operations, limit the circuit's output current. For details, see Section 1.1, Absolute Maximum Ratings.

Figure 4-3 show the quantities used in the following power calculations for a single operational amplifier. R_{SER} is 0Ω in most applications. Higher values can be used to limit I_{OUT}. V_{OUT} is the operational amplifier's output voltage, V_L is the voltage at the load and V_{LG} is the load's ground point. V_{SS} is usually ground (0V). The input currents are assumed to be negligible.

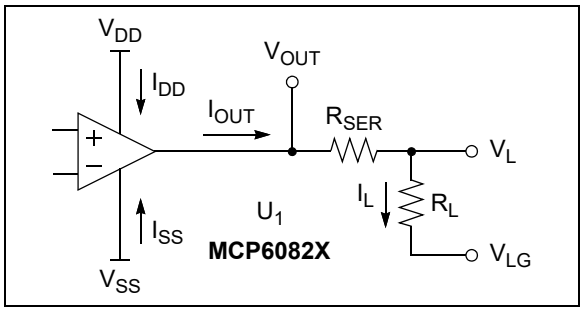


FIGURE 4-3: *Diagram for Power Calculations.*

The currents shown in Figure 4-3 are calculated using Equation 4-1.

EQUATION 4-1:

$$I_{OUT} = I_L = \frac{V_{OUT} - V_{LG}}{R_{SER} + R_L}$$

$$I_{DD} \approx I_Q + \max\,(0, I_{OUT})$$

$$I_{SS} \approx -I_Q + \min\,(0, I_{OUT})$$

Where:

I_{OUT} = Output Current (mA)
I_L = Load Current (mA)
V_{OUT} = Output Voltage (V)
V_{LG} = Load Ground Point Voltage (V)
R_{SER} = Series Resistance (kΩ)
R_L = Load Resistance (kΩ)
I_{DD} = Positive Supply Current (mA)
I_Q = Quiescent Supply Current (mA)
I_{SS} = Negative Supply Current (mA)

The instantaneous operational amplifier power ($P_{OA}(t)$), R_{SER} power ($P_{RSER}(t)$) and load power ($P_L(t)$) are determined as shown in Equation 4-2.

EQUATION 4-2:

$$P_{OA}(t) = I_{DD}(V_{DD} - V_{OUT}) + I_{SS}(V_{SS} - V_{OUT})$$

$$P_{RSER}(t) = I_{OUT}^2 \times R_{SER}$$

$$P_L(t) = I_L^2 \times R_L$$

Where:

$P_{OA}(t)$ = Instantaneous Operational Amplifier Power (W)
I_{DD} = Positive Supply Current (mA)
V_{DD} = Positive Supply Voltage (V)
V_{OUT} = Output Voltage (V)
I_{SS} = Negative Supply Current (mA)
V_{SS} = Negative Supply Voltage (V)
$P_{RSER}(t)$ = R_{SER} Power (W)
R_{SER} = Series Resistance (kΩ)
$P_L(t)$ = Load Power (W)
I_L = Load Current (mA)
R_L = Load Resistance (kΩ)

The maximum operational amplifier power dissipation, with resistive loads, occurs when V_{OUT} is halfway between V_{DD} and V_{LG} or halfway between V_{SS} and V_{LG}, as shown in Equation 4-3.

EQUATION 4-3:

$$P_{OAmax} \leq \frac{max^2(V_{DD} - V_{LG}, V_{LG} - V_{SS})}{4(R_{SER} + R_L)}$$

Where:

P_{OAmax} = Maximum Power Dissipation (W)
V_{DD} = Positive Supply Voltage (V)
V_{LG} = Load Ground Point Voltage (V)
V_{SS} = Negative Supply Voltage (V)
R_{SER} = Series Resistance (kΩ)
R_L = Load Resistance (kΩ)

The maximum ambient to junction temperature rise (ΔT_{JA}) and junction temperature (T_J) is calculated by summing the power dissipation for all operational amplifiers in the same package (ΣP_{OAmax}), the ambient temperature (T_A) and the package thermal resistance (θ_{JA}) found in Table 1-3. The calculation is show in Equation 4-4.

EQUATION 4-4:

$$\Delta T_{JA} = \theta_{JA} \times \sum P_{OAmax}$$

$$T_J = T_A + \Delta T_{JA}$$

Where:

ΔT_{JA} = Maximum Ambient To Junction Temperature Rise (°C)

θ_{JA} = Package Thermal Resistance (°C/W)

P_{OAmax} = Maximum Operational Amplifier Power Dissipation (W)

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

4.1.5 TRIMMED I_Q

I_Q is trimmed and is reasonably flat across temperature (T_A) and supply voltage ($V_{DD} – V_{SS}$) as shown in Figure 2-23. This reduces P_{OAmax} in an application. I_Q increases at higher V_{CM} levels (see Figure 2-24).

4.1.6 EMI REJECTION RATIO (EMIRR)

Electromagnetic interference (EMI) is the disturbance that affects an electrical circuit, due to either electromagnetic induction or radiation, emitted from an external source.

EMIRR helps describe the EMI robustness of an operational amplifier to an interfering radio frequency (RF) signal. The common errors caused by EMI in circuits are a shift in input offset voltage (V_{OS}), due to nonlinearities at the input and interference at high frequencies. EMIRR compares the change in V_{OS} to the RF signal's peak voltage as shown in Equation 4-5.

EQUATION 4-5:

$$EMIRR(dB) = 20 \cdot \log \frac{V_{RF}}{\Delta V_{OS}}$$

Where:

$EMIRR$ = Electromagnetic Interference Rejection Ratio (dB)

V_{RF} = Interfering RF Signal's peak voltage (V_{PK}) (V)

ΔV_{OS} = Input Offset Voltage Aging

Internal passive filters improve EMIRR, but proper PCB layout techniques are also necessary for best overall performance.

4.2 Circuit Design

4.2.1 SUPPLY BYPASS

For a positive single supply (V_{SS} = 0V and V_{DD} > V_{SS}), the V_{DD} pin needs a local bypass capacitor (usually 10 nF to 100 nF) within 2 mm of the V_{DD} pin. This gives good high-frequency performance. It also needs a bulk capacitor (usually 1 µF or larger) within 10 mm. This provides for large, slow currents. In some cases, but not all, this bulk capacitor can be shared with nearby analog parts.

For split or dual supplies (V_{SS} < 0V < V_{DD}), both the V_{DD} pin and the V_{SS} pin need bypass capacitors as previously described.

4.2.2 PCB SURFACE LEAKAGE

In applications where maintaining low input currents is critical, Printed Circuit Board (PCB) leakage currents must be minimized. These PCB leakage currents are mainly caused by humidity, dust or other contaminants on PCB surfaces.

The following techniques can reduce PCB leakage currents:

- Place critical input traces in inner layers
- Use conformal coating
- Use guard rings where possible (packages with tightly spaced pins can limit this approach)

4.2.3 LOW OFFSETS

4.2.3.1 Input Offset Voltage Errors

The data sheet parameters that describe DC voltage errors at the operational amplifier's input act as an increase of the voltage at the noninverting input (see Figure 4-4). These parameters are: V_{OS}, TC_1, TC_2, CMRR, PSRR and A_{OL} (see the DC Electrical Specifications table).

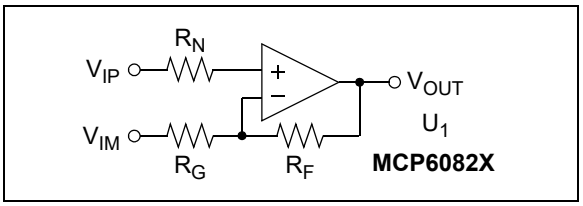


FIGURE 4-4: *Operational Amplifier Feedback Network.*

The combined errors are shows in Equation 4-6.

EQUATION 4-6:

$$V_{OST} = V_{OS} + TC_1(T_A - 5°C) + TC_2(T_A - 5°C)(T_A - 105°C) + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{OUT}}{A_{OL}} + \frac{\Delta(V_{DD} - V_{SS})}{PSRR}$$

Where:

V_{OST}	=	Total Input Offset Voltage (error) (V)
V_{OS}	=	Input Offset Voltage (V)
TC_1	=	Input Offset Drift with Temperature Coefficient (µV/°C)
TC_2	=	Input Offset Quadratic Temperature Coefficient (µV/°C)
T_A	=	Ambient Temperature (°C)
ΔV_{CM}	=	Common Mode Input Voltage Drift (V)
$CMRR$	=	Common Mode Rejection Ratio (dB)
ΔV_{OUT}	=	Output Voltage Drift (V)
A_{OL}	=	DC Open-Loop Gain (µV/V)
V_{DD}	=	Positive Supply Voltage (V)
V_{SS}	=	Negative Supply Voltage (V)
$PSRR$	=	Power Supply Rejection Ratio (dB)

$\frac{1}{CMRR}$, $\frac{1}{A_{OL}}$ and $\frac{1}{PSRR}$ are measured in µV/V (for example, a value of ±100 µV/V corresponds to 80 dB).

The error referred to operational amplifier's output voltage, V_{OERR}, is shown in Equation 4-7.

EQUATION 4-7:

$$V_{OERR} = G_N \cdot V_{OST}$$

$$G_N = 1 + \frac{R_F}{R_G}$$

Where:

V_{OERR} = Total Output Offset Voltage (error) (V)
G_N = Noise Gain (V/V)
V_{OST} = Total Input Offset Voltage (error) (V)
R_F = Feedback Resistance (kΩ)
R_G = Gain Resistance (kΩ)

Mechanical stresses affecting the operational amplifier change the input offset voltage. Standard techniques to minimize stresses on the PCB also minimize this issue.

4.2.3.2 Input Bias Current Errors

The Input Bias Current (I_B) and the Input Offset Current (I_{OS}) cause voltage drops across resistors in the circuit, resulting in increased voltage errors. Considering these currents are positive when they enter the operational amplifier, the voltage errors present in the circuit shown in Figure 4-4 are determined using Equation 4-8.

EQUATION 4-8:

$$V_{TIBE} = R_F \| R_G \cdot \left(I_B - \frac{I_{OS}}{2}\right) - R_N \cdot \left(I_B + \frac{I_{OS}}{2}\right)$$

$$V_{TOBE} = G_N \cdot V_{TIBE}$$

Where:

V_{TIBE} = Total Input Bias Current Error
R_F = Feedback Resistance (kΩ)
R_G = Gain Resistance (kΩ)
I_B = Input Bias Current (pA)
I_{OS} = Input Offset Current (pA)
R_N = Noise Resistance (kΩ)
V_{TOBE} = Total Output Bias Current Error
G_N = Noise Gain (V/V)

Note that the PCB leakage currents discussed in Section 4.2.2, PCB Surface Leakage add additional DC errors to the circuit. These errors depend on where these currents are injected into the circuit. Standard circuit analysis techniques give the output error.

4.2.4 STABILIZING AMPLIFIER CIRCUITS

4.2.4.1 Parasitic Capacitances

The op amp's parasitic capacitances of interest are the input common mode capacitance (C_{CM} in Table 1-1) at the noninverting and inverting inputs.

The PCB's parasitic capacitance (C_{PCB}) varies, depending on the dielectric and physical dimensions. We used 2 layer, FR4 boards for our measurements; we saw between 2 pF to 10 pF for our designs.

Resistor parasitic capacitances can be significant for large values. Usually, surface mount resistors have parallel capacitances less than 1 pF.

The resistors in Figure 4-5 need to be low enough so the resulting poles and zeros from all of these capacitances are fast enough to have little effect on gain or stability.

Use narrow and short PCB traces to connect signals to the op amp. Design the ground system and select components for low parasitic capacitance.

4.2.4.2 Stability Design

Driving large capacitive loads can result in stability problems for operational amplifiers. As the load capacitance (C_L) increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the signal's frequency response and overshoot and ringing in the step response. A unity-gain buffer (G = +1 V/V) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads (e.g., C_L > 30 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. In this situation, the bandwidth is generally lower than the bandwidth with no capacitive load.

R_F and R_G set the DC gain; they are kept at reasonably low values for better stability. C_N and C_G are the sum of parasitic capacitances from the op amp (C_{CM}) and PCB (C_{PCB}). C_F compensates for C_G at low frequencies. R_D improves stability at low gains. R_N helps reduce DC errors caused by U_1's input currents.

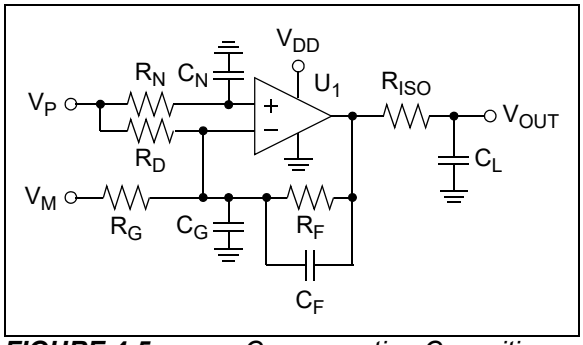


FIGURE 4-5: *Compensating Capacitive Loads (C_L) and Low Gains.*

Figure 2-43 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's Noise Gain. For noninverting gains, the Noise Gain and the Signal Gain are equal. For inverting gains, $G_N = 1 + |\text{Signal Gain}|$. For example, a Signal Gain of -1 V/V gives G_N = +2 V/V.

These additional recommendations will help initialize your stability design (Figure 2-43 is based on them):

R_D = open

$R_G = (2\ k\Omega)/G_N$

$R_F = 2\ k\Omega - R_G$

$C_F = C_G/(G_N - 1)$

When G_N would be less than 1.76 V/V when R_D is open, set:

$R_D = 1 / (1.76/R_F - 1/R_G)$

Double-check the resulting frequency response peaking and step response overshoot using simulations and bench measurements. Modify R_{ISO}, C_F and R_D as needed.

4.2.5 ESTIMATING THE BANDWIDTH

The three most common operational amplifier circuits are represented by Figure 4-6:

- Noninverting Gain (R_{PF} = open and V_{IM} grounded)
- Inverting Gain (R_{PF} = open and V_{IP} grounded)
- Differential Gain

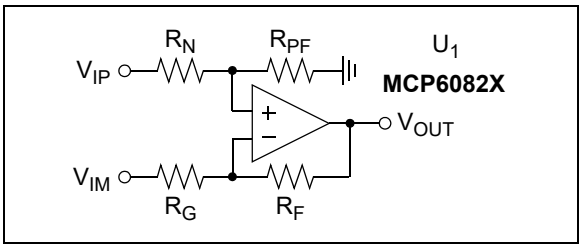


FIGURE 4-6: *Common Operational Amplifier Configurations.*

The Noise Gain and the Small Signal Bandwidth are determined using Equation 4-9.

EQUATION 4-9:

$$G_N = 1 + \frac{R_F}{R_G}$$

$$BW \approx \frac{GBWP}{G_N}, (G_N > 2)$$

Where:

G_N = Noise Gain (V/V)
R_F = Feedback Resistance (kΩ)
R_G = Gain Resistance (kΩ)
BW = Bandwidth (Hz)
$GBWP$ = Gain-bandwidth product (Hz)

The Full Power Bandwidth (FPBW) is the frequency where a large output sine wave's maximum slope equals the Slew Rate (SR), as shown in Equation 4-10.

EQUATION 4-10:

$$FPBW \approx \frac{|SR|}{\pi V_{OPP}}$$

Where:

$FPBW$ = Full Power Bandwidth (Hz)
SR = Slew Rate (V/µs)
V_{OPP} = Peak-to-Peak Output Voltage (V_{P-P})

For accurate AC gains, set the bandwidth higher than the input signal's bandwidth (for example, a 10:1 ratio). For low harmonic distortion, set FPBW higher than the bandwidth (for example, a 3:1 ratio).

4.2.6 POWER UP/DOWN

The **Power Up/Down** section of the AC Electrical Specifications table defines how I_Q and V_{OUT} behave when power pin (V_{DD}) turns MCP6082X on and off, using the internal POR circuit.

When powered up, MCP6082X quickly becomes operational (t_{PONIQ} and t_{PON}). It uses extra current (I_{Q_TR}) for a short time (t_{PON_TR}) to complete the internal trims. During this time, V_{OS} and I_Q settle to their final values.

When powered down, MCP6082X quickly shuts down. (t_{POFFIQ} and t_{POFF}). Once off, I_Q = 0, since $V_{DD} = V_{SS}$.

When powering up and down, make sure that V_{DD} ramps up and down smoothly and quickly between 0V and 2.2V. This assists the internal digital circuitry to operate as specified.

4.2.7 SHUTDOWN PIN

The **Shutdown** section of the AC Electrical Specifications table defines how I_Q and V_{OUT} behave when the Shutdown Pin (SHDN) is brought up (off, with low I_Q) and down (on, with normal operation).

At initial power up, MCP6082X is kept in the enabled state (for t_{PON_TR} – see Figure 1-3) to load all of the internal trim registers from the nonvolatile memory. Once this completes, control is passed to the SHDN pin. At power down, the shutdown function is disabled and the internal trim registers lose their values.

When SHDN turns MCP6082X off, the quiescent current reaches a very low level (I_{SS_SD}), that saves power.

When SHDN turns MCP6082X on, the operational amplifier quickly reaches normal operation (all trims are complete) without needing extra current (I_{Q_TR}) or time (t_{PON_TR}) to complete the internal trims. For these reasons, using the SHDN pin may be preferred in some applications.

While in shutdown, the operational amplifier no longer controls V_{OUT}. The resistors and other voltage sources present in the circuit set V_{DM} ($V_{DM} = V_{IN+} - V_{IN-}$). To support low input offset voltage (V_{OS}) aging, ensure V_{DM} is near 0 mV while in shutdown.

4.2.8 NOISE

Figure 2-31 shows the Input Noise Voltage Density across frequency, $e_{ni}(f)$. The corresponding Integrated Output Noise Voltage (E_{no}) is the Root Mean Square (RMS) noise seen at the output due to $e_{ni}(f)$ and the Noise Gain across frequency, $G_N(f)$. $G_N(f)$ is the gain from the operational amplifier's noninverting input to its output. E_{no} is calculated using Equation 4-11.

EQUATION 4-11:

$$E_{ni}^2(f_L, f_H) = \int_{f_L}^{f_H} e_{ni}^2(f) \cdot G_N^2(f) df$$

Where:

E_{ni} = Input Noise Voltage (μV_{P-P})
f_L = Low Frequency Limit (Hz)
f_H = High Frequency Limit (Hz)
e_{ni} = Input Noise Voltage Density (nV/√Hz)
G_N = Noise Gain (V/V)

$e_{ni}(f)$ is measured in nV/√Hz. E_{ni} has two common units: μV_{RMS} (RMS value) and μV_{P-P} (Peak-to-Peak value). The E_{ni} specification (in AC Electrical Specifications) shows units of μV_{P-P} and a value 6.6 times larger than the RMS value.

4.3 Typical Applications

4.3.1 LOW-PASS FILTER

Figure 4-7 is a low-pass active filter using Sallen-Key topology. It has a bandwidth of 250 kHz that takes advantage of the MCP6082X's speed. It also has low sensitivity to component variations. This and other active filters can be easily designed using Microchip's FilterLab® design tool.

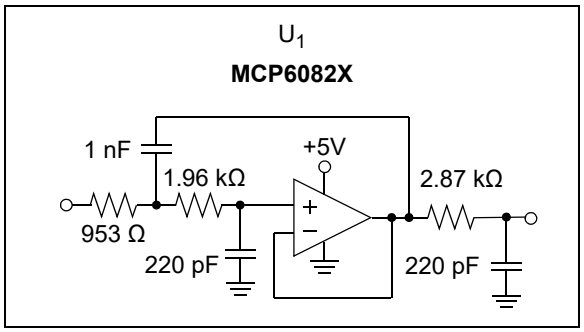


FIGURE 4-7: *Sallen-Key Low-Pass Filter, 250 kHz Bandwidth.*

4.3.2 EDGE DETECTOR

Figure 4-8 shows an edge detector based on a high-pass Sallen-Key filter and a low-pass R-C filter. At low frequencies, the high-pass filter produces a gain proportional to f^2 (or the second time derivative of V_{IN}) that emphasizes the time points when there are large changes in the slope of V_{IN}. The low-pass filter limits the impact of random noise and interference.

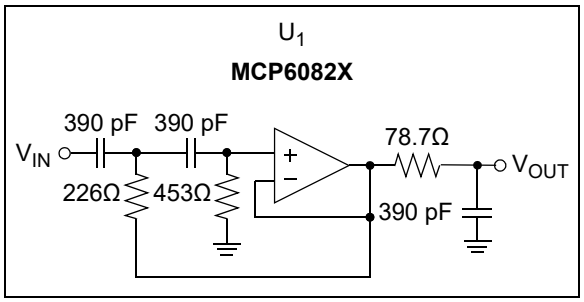


FIGURE 4-8: *Edge Detector Circuit.*

The high-pass filter has a second order Butterworth response, with low step response overshoot. Its cutoff frequency is 1.3 MHz and supports the detection of rise and fall times of 0.3 µs and longer.

The low-pass filter has a cutoff frequency of 5 MHz and supports detection of rise and fall times of 0.3 µs and longer.

4.3.3 PHOTODIODE DETECTOR

The circuit in Figure 4-9 has a photodiode detector (D) that has parasitic capacitance, C_D and produces an output current, I_D. V_{DB} biases the photodiode detector so that it is either in photovoltaic mode (at 0V, like U_1's noninverting input) or photoconductive mode (less than 0V). Photovoltaic mode has a linear response to light, while photoconductive mode is faster.

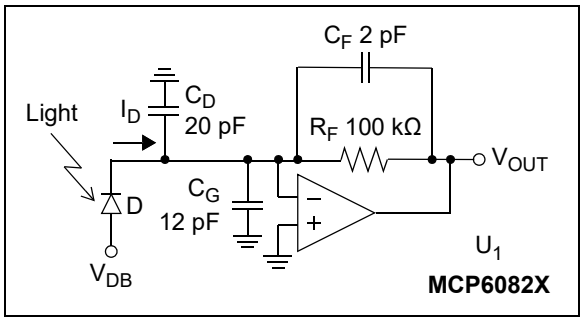


FIGURE 4-9: *Photodiode Detector Circuit.*

The operational amplifier (U_1) provides gain. The capacitance C_G represents parasitic PCB capacitance and U_1's input capacitance (C_{CM}).

The gain resistor (R_F) converts I_D to a voltage at pin V_{OUT}. The combination of R_F, C_D and C_G create a noise gain zero at 22.7 kHz that destabilizes the feedback loop if C_F is not of appropriate value. C_F and the parasitic capacitance of R_F (for example, 0.15 pF) both stabilize the feedback loop by adding a noise gain pole at 0.74 MHz and set the high frequency noise gain to 15.9 V/V.

The feedback loop's crossover frequency is the operational amplifier's gain-bandwidth product divided by the high frequency noise gain, or 1.6 MHz. Since this is roughly 2.5 times larger than the noise gain pole, the feedback loop is robustly stable.

The signal gain has one pole at 0.74 MHz that is set by R_F and C_F (the same as the noise gain pole).

Use simulations and bench testing to obtain the design goals. Check step response overshoot for stability and random output noise for accuracy.

Other photovoltaic detector circuits come with different trade-offs. The circuit in Figure 4-9 is faster than a circuit that does not require C_F, but needs a much faster operational amplifier. Other implementation details can vary as well.

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP60821/1U/3 operational amplifiers.

5.1 Analog Demonstration Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to aid customers achieve faster time to market.

For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchipdirect.com.

5.2 Application Notes

The following Microchip Analog Design Notes and Application Notes are available on the Microchip website at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **AN003** – *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **AN722** – *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723** – *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884** – *"Driving Capacitive Loads With Operational Amplifiers"*, DS00884
- **AN990** – *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1177** – *"Operational Amplifier Precision Design: DC Errors"*, DS01177
- **AN1228** – *"Operational Amplifier Precision Design: Random Noise"*, DS01228
- **AN1297** – *"Microchip's Operational Amplifier SPICE Macro Models"*, DS01297
- **AN1332** – *"Current Sensing Circuit Concepts and Fundamentals"*, DS01332
- **AN1494** – *"Using MCP6491 Operational Amplifiers for Photodetection Applications"*, DS01494

These applications notes and others are listed in the design guide:

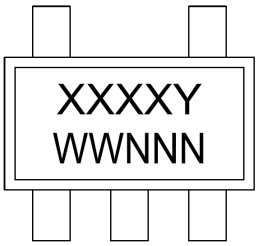
- *"Signal Chain Design Guide"*, DS21825

NOTES:

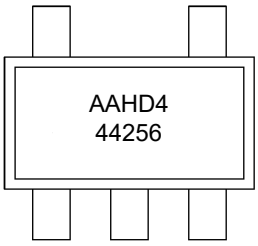
6.0 PACKAGING INFORMATION

6.1 Package Markings

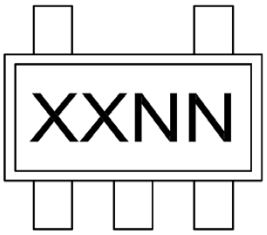
5 Lead SOT-23 (MCP60821)



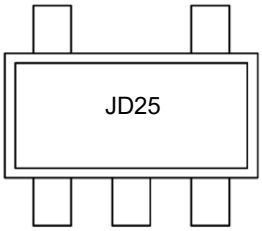
Example:



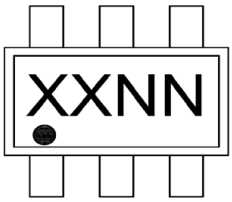
5 Lead SC70 (MCP60821U)



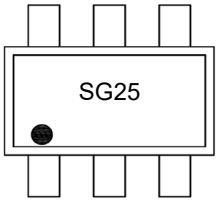
Example:



6 Lead SOT-23 (MCP60823)



Example:



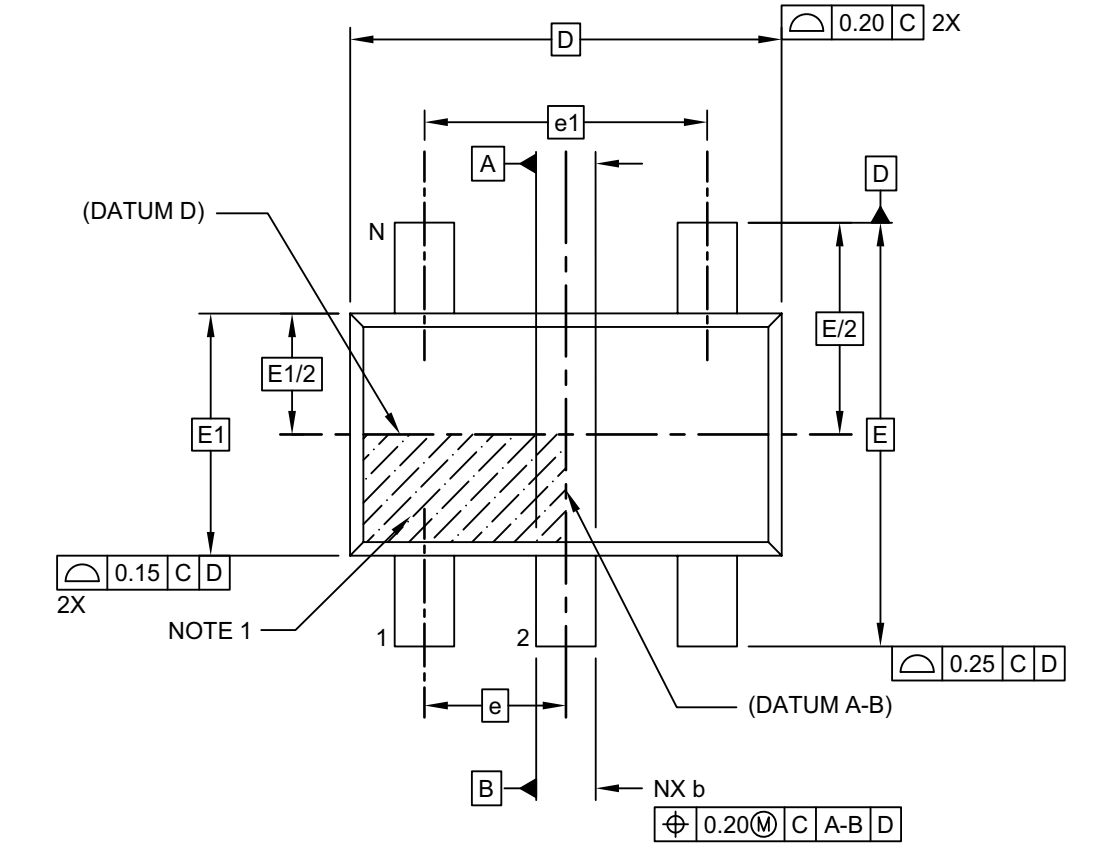
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

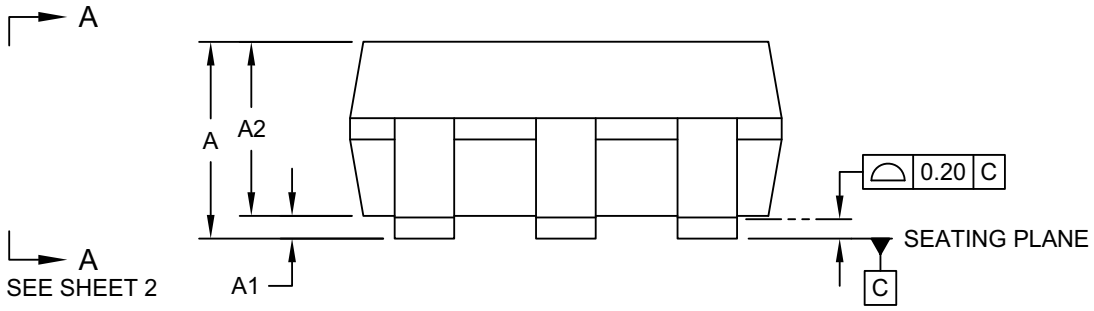
6.2 Package Drawings

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

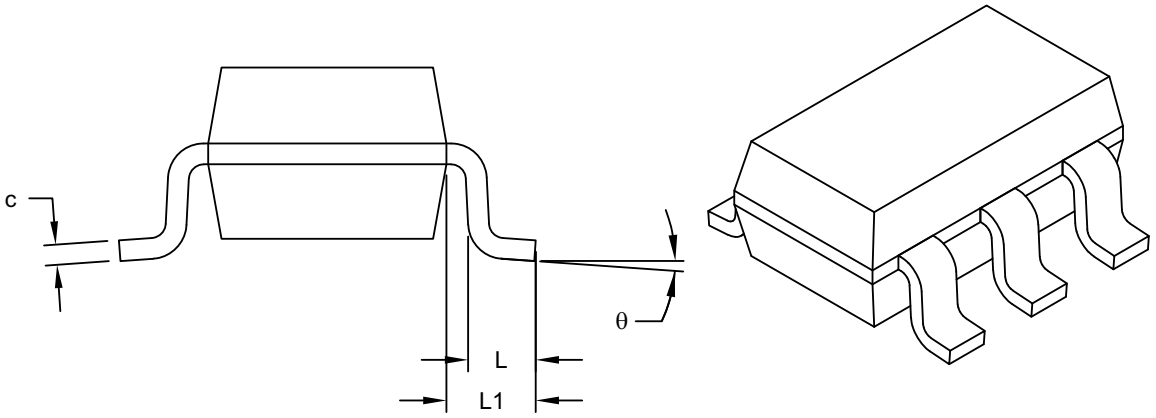


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

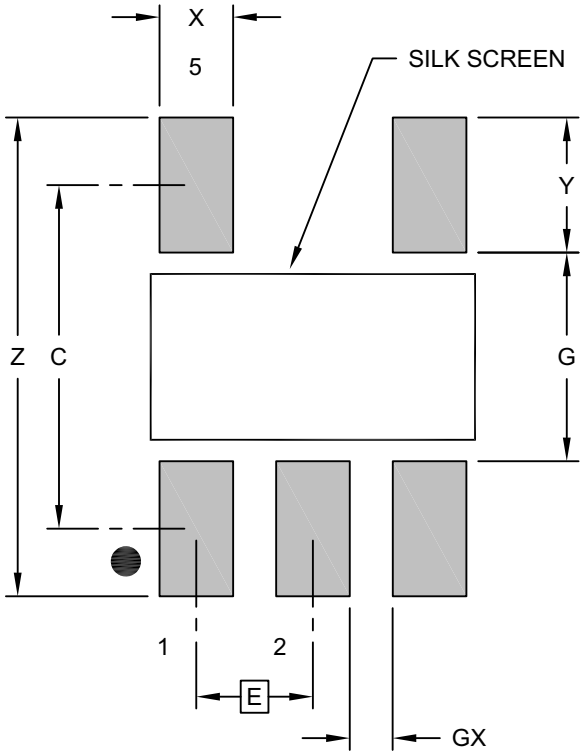
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

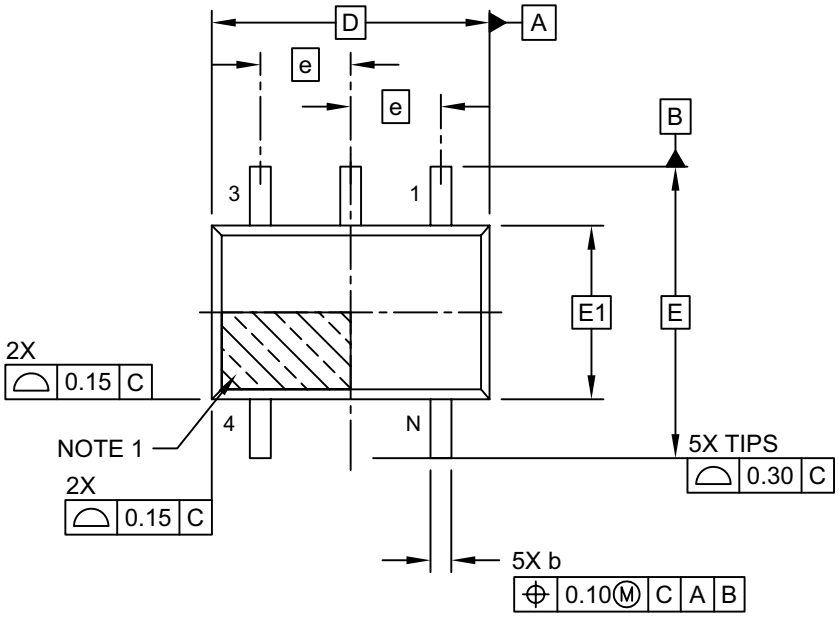
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

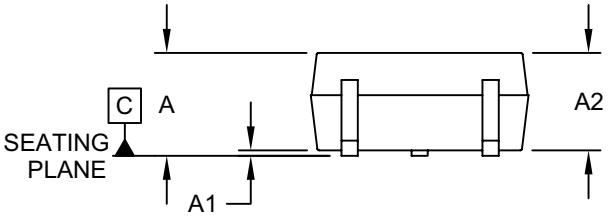
Microchip Technology Drawing No. C04-2091-OT Rev H

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

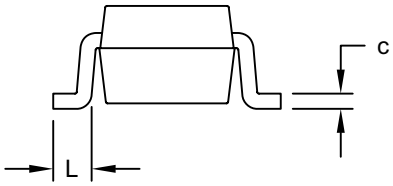
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

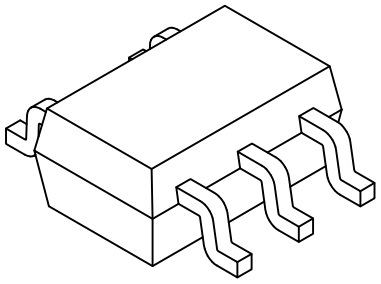


END VIEW

Microchip Technology Drawing C04-061-LTY Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

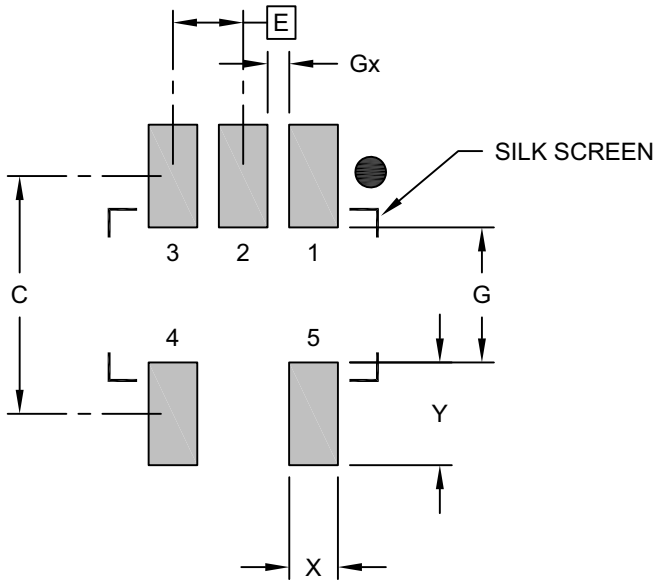
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LTY Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

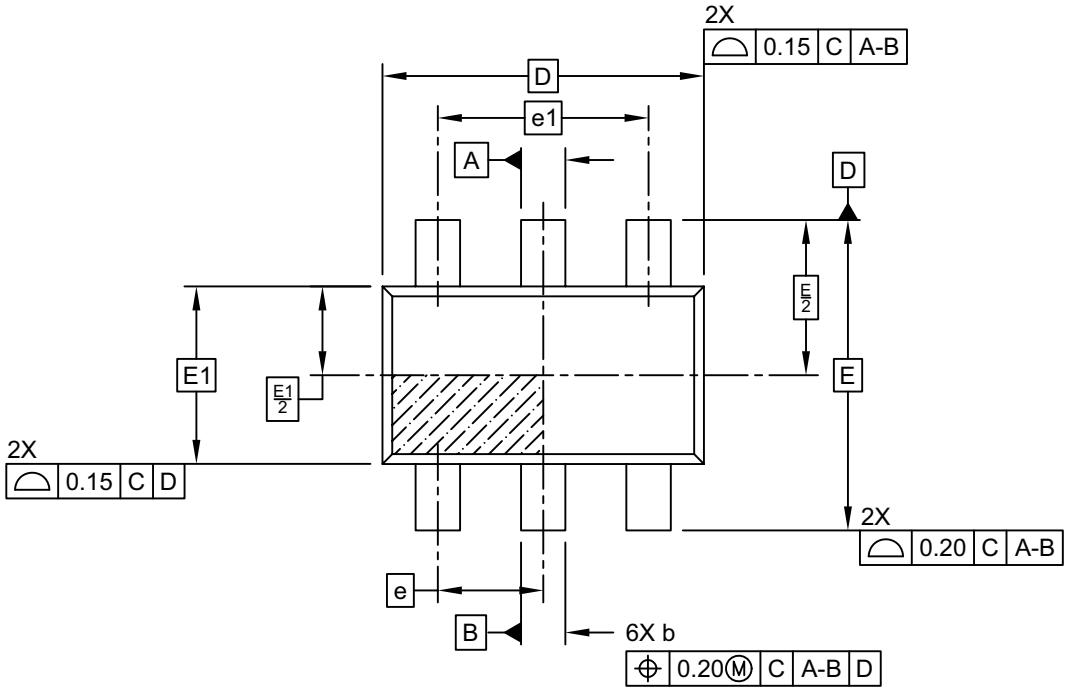
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

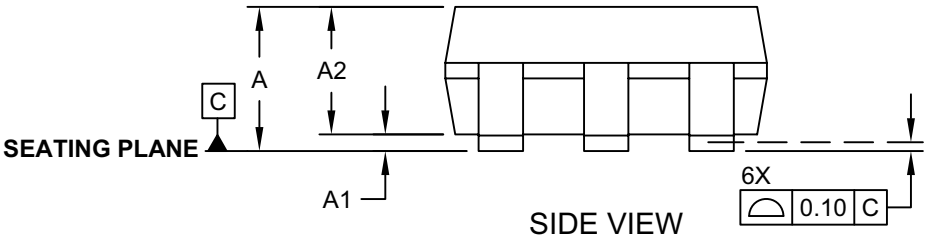
Microchip Technology Drawing No. C04-2061-LTY Rev E

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

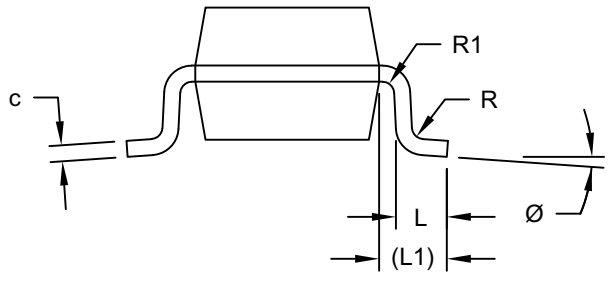
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

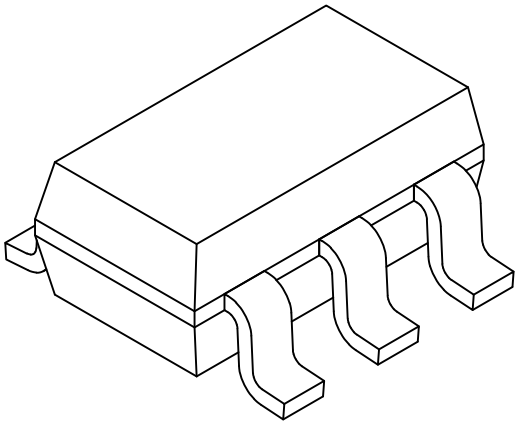


END VIEW

Microchip Technology Drawing C04-028-CH Rev. F Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	Ø	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

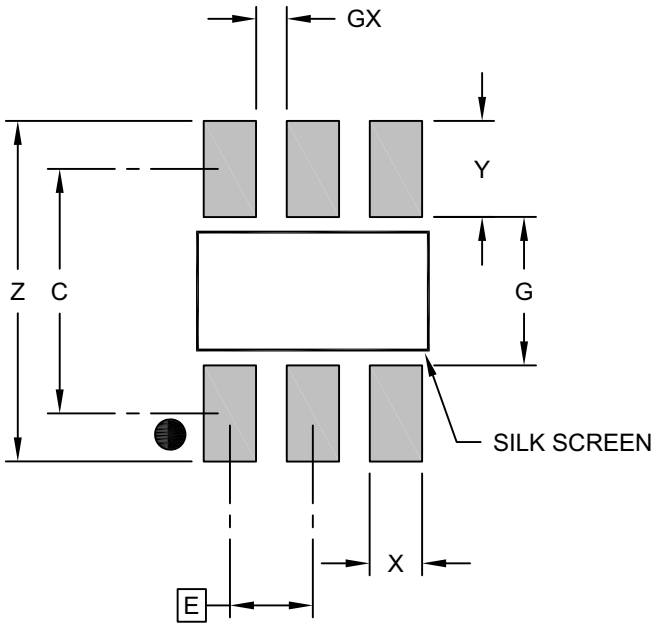
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028-CH Rev.F Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028-CH Rev.F

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2024)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP60821:	25 MHz Single Operational Amplifier
	MCP60821U:	25 MHz Single Operational Amplifier
	MCP60823:	25 MHz Single Operational Amplifier
Temperature Range:	E =	-40 °C to +125 °C
Package:	LTY =	5-Lead Plastic Small Outline Transistor (SC70) *
	OT =	5-Lead Plastic Small Outline Transistor (SOT-23)
	CH =	6-Lead Plastic Small Outline Transistor (SOT-23)
	* Y =	Nickel-Palladium-Gold Manufacturing Designator.

Examples:

a) MCP60821T-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23

b) MCP60821UT-E/LTY: Tape and Reel, Extended Temperature, 5-Lead SC70

c) MCP60823T-E/CH: Tape and Reel, Extended Temperature, 6-Lead SOT-23

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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