CoolSET™ ICE5BRxxxxBZx-1 high-voltage buck converter design guide

About this document

Scope and purpose

This document is a design guide for a Fixed-Frequency high-voltage (HV) buck converter using Infineon's latest CoolSET™ 5th Generation Fixed Frequency Plus ICE5BRxxxxBZx-1, which offers high-efficiency, low-standby power with selectable entry and exit standby power options, wider VCC operating range with fast start-up, and various protection modes for a highly reliable system.

Intended audience

This document is intended for power supply design/application engineers, students, etc. who wish to design power supplies with Infineon's CoolSET™ 5th Generation Fixed Frequency Plus ICE5BRxxxxBZx-1.

CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed-frequency switching scheme offers increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Home appliances
- Server
- Telecom

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1 Abstract

This design guide is for a Fixed Frequency HV buck converter using Infineon's latest CoolSET™ 5th Generation Fixed Frequency Plus ICE5BRxxxxBZx-1.

The IC is optimized for offline SMPS applications including home appliances/white goods, e-metering, and low-power auxiliary power supply. The frequency reduction with soft gate driving and frequency-jitter operation offers lower EMI and better efficiency between light and medium loads. The selectable entry/exit standby power active burst mode (ABM) feature enables flexibility and low-power consumption in standby mode with small and controllable output voltage ripple. The product has a wide operating range (10~30.5 V) of IC power supply and lower power consumption. The numerous protection functions give full protection to the power supply system in failure situations. All of these features make CoolSET™ ICE5BRxxxxBZx-1 an excellent choice for Fixed Frequency HV buck converters.

2 Description

2.1 List of features

- Integrated 800 V/950 V avalanche rugged CoolMOS™
- Enhanced ABM with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast start-up, achieved with cascode configuration
- Discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation with slope compensation
- Frequency jitter and soft gate driving for low EMI
- Built-in digital soft-start
- Cycle-to-cycle peak-current limitation (PCL)
- Integrated error amplifier to support direct feedback (FB) in a HV buck and non-isolated flyback converter
- Comprehensive protection with VCCovervoltage (OV), VCC undervoltage (UV), overload/open-loop, and overtemperature protection
- All protections are in auto-restart mode
- Limited charging current for VCC short-to-GND
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

2.2 Pin configuration and functionality

The pin configuration is shown in Figure 1 and the functions are described in Table 1.

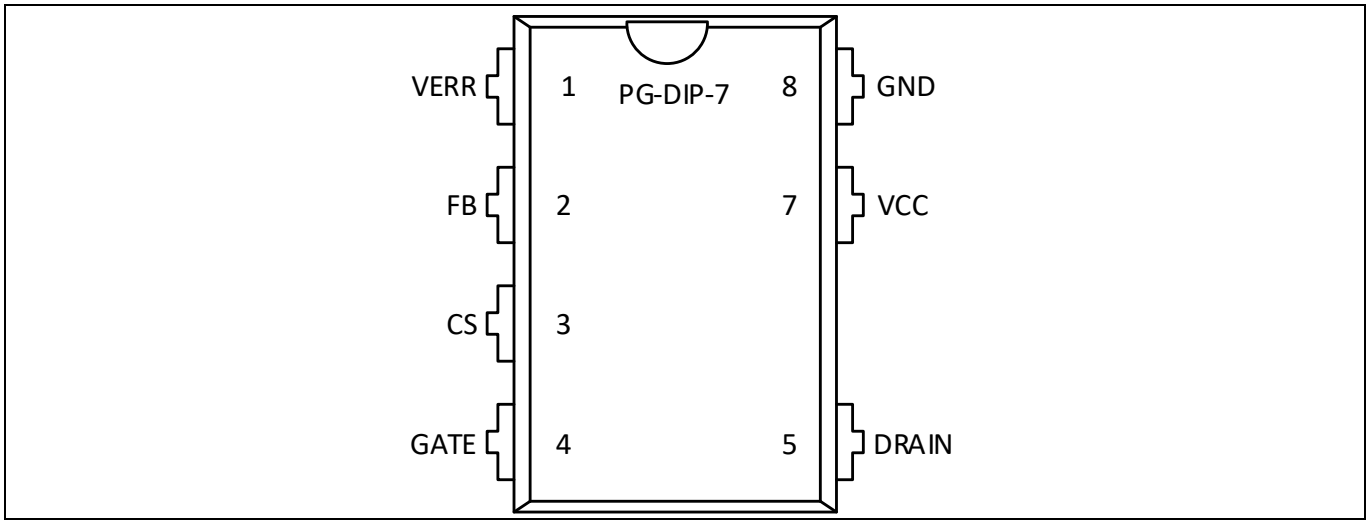

Figure 1 Pin configuration

Description

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	VERR	Error amplifier The VERR pin is internally connected to the transconductance error amplifier for HV buck and non-isolated flyback applications. Connect this pin to GND for an isolated flyback application.
2	FB	FB and ABM entry/exit control The FB pin combines the functions of FB control, selectable burst entry/exit control and overload/open-loop protection.
3	CS	CS The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the FB voltage) internally.
4	GATE	Gate driver output The GATE pin is connected to the gate of the CoolMOS™ power MOSFET, and a pull-up resistor is connected from the bus voltage to turn on the power MOSFET for charging up the VCC capacitor during start-up.
5	DRAIN	Drain (drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™ power MOSFET.
7	VCC	VCC (positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between VV_{CC_OFF} and VV_{CC_OVP}.
8	GND	Ground The GND pin is the common ground of the controller.

3 Overview of fixed-frequency high-voltage buck converter

Figure 2 shows the typical application of ICE5BRxxxxBZx-1 in a HV buck converter.

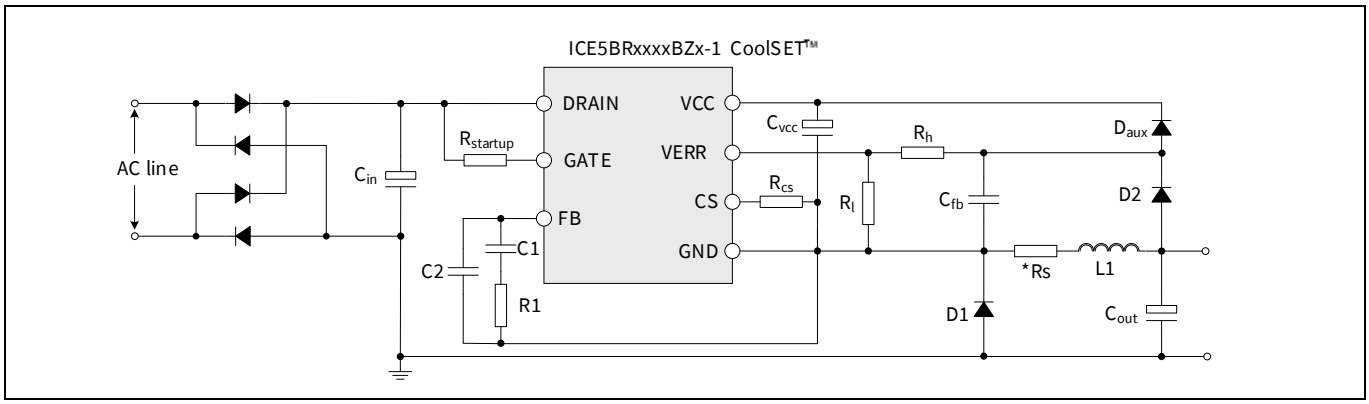

Figure 2 Typical application in a Fixed Frequency HV buck converter

Table 2 Key component quick selection guide for different V_{OUT} and I_{OUT} under universal input range of 85~265 V AC and D1 t_{rr} of ≤35 ns (see Figure 18 for other component values)

V_{OUT} (V)	$I_{OUT(MAX)}$ (mA)	Suggested CoolSET™ device	L1		R_{CS}[1] (Ω)	R_h (kΩ)	R_l (kΩ)
			L_{typ} (µH)	I_{RMS} (mA)			
12	≤250	ICE5BR4780BZ-1	330	308	1.38	270	47
	350		220	427	0.97		
	450		180	520	0.80		
	550	ICE5BR3995BZ-1	150	632	0.66		
	625	ICE5BR2280BZ-1	120	774	0.54		
	700		120	796	0.53		
15	≤250	ICE5BR4780BZ-1	390	303	1.38	270	36
	350		270	419	0.99		
	450		220	517	0.81		
	550	ICE5BR3995BZ-1	150	727	0.57		
	625	ICE5BR2280BZ-1	150	722	0.57		
	700		150	789	0.54		
18	≤250	ICE5BR4780BZ-1	470	311	1.38	270	30
	350		330	402	1.04		
	450		270	508	0.84		
	550	ICE5BR3995BZ-1	220	620	0.67		
	625	ICE5BR2280BZ-1	180	708	0.60		
	700		150	808	0.51		

[1] Select the nearest lower standard or a combination of standard values.

4 Functional description and component design

4.1 VCC pre-charging and typical VCC voltage during start-up

When the AC-line input voltage is applied, a rectified voltage appears across the capacitor C_{IN} (see Figure 2). The pull-up resistor $R_{StartUp}$ provides the current to charge the C_{iss} (input capacitance) of the integrated HV power MOSFET. Once the voltage across C_{iss} is sufficiently high, the power MOSFET will turn on and the VCC capacitor will be charged through the power MOSFET, internal diode, buck inductor, and the output with two steps of constant current source $I_{VCC\_Charge1}$[2] and $I_{VCC\_Charge3}$[1].

A very small current source ($I_{VCC\_Charge1}$) charges the VCC capacitor until VCC reaches V_{VCC_SCP} to protect the controller from a VCC pin short-to-GND during start-up. After this, the second-step constant current source ($I_{VCC\_Charge3}$) is provided to further charge the VCC capacitor, until VCC exceeds the turn-on threshold V_{VCC_ON}. As shown in Phase I in Figure 3, the VCC voltage increases almost linearly, with two steps.

Note: The recommended typical value for $R_{StartUp}$ is 50 MΩ (20 MΩ~100 MΩ). $R_{StartUp}$ value is directly proportional to $t_{StartUp}$ and inversely proportional to no-load standby power.

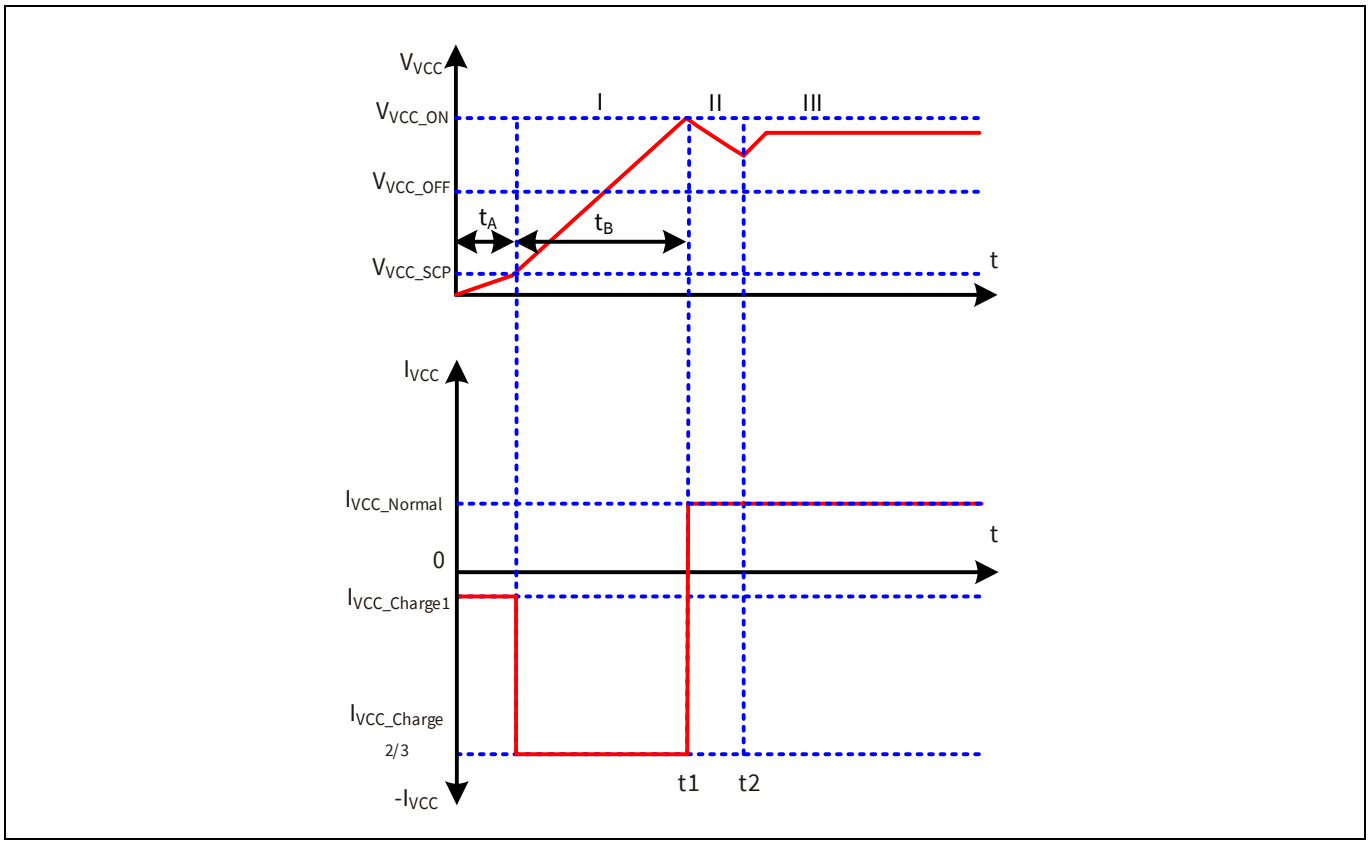

Figure 3 VCC voltage and current at start-up

[2] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to the VCC capacitor during start-up.

The time taken for the VCC pre-charging can then be approximated as:

$$t_{\mathrm{StartUp}} = t_{\mathrm{A}} + t_{\mathrm{B}} = \frac{V_{VCC_{SCP}} \cdot C_{VCC}}{I_{VCC_{Charge1}}} + \frac{(V_{VCC_{ON}} - V_{VCC_{SCP}}) \cdot C_{VCC}}{I_{VCC_{Charge3}}}$$

Equation 1 VCC pre-charging time

Where,

V_{VCC_SCP} = VCC short-circuit protection voltage

C_{VCC} =VCC capacitor

V_{VCC_ON} =VCC turn-on threshold voltage

$I_{VCC\_Charge1}$ = VCC charge current 1

$I_{VCC\_Charge3}$ = VCC charge current 3

When the VCC voltage exceeds the V_{VCC_ON} at time t_1, the IC begins to operate with a soft-start. Because of power consumption of the IC and the fact that the output voltage is still lower than the VCC voltage, the VCC voltage drops during phase II. Once the output voltage exceeds the VCC voltage, the output charges the VCC capacitor from the time t_2 onward, delivering power to the IC. The VCC will then reach a constant value of two diode voltage drops lower than the output voltage.

4.1.1 VCC capacitor

As there is a VCC UV protection, the VCC capacitor should be selected to be large enough to ensure enough energy is stored in the VCC capacitor so that the VCC voltage will not drop below the VCC UV protection threshold V_{VCC_OFF}. Therefore, the minimum capacitance should meet the following requirement:

$$C_{VCC} > \frac{I_{VCC_{normal2}} \times t_{ss}}{V_{VCC_{ON}} - V_{VCC_{OFF}}}$$

Equation 2 Condition for minimum capacitance

Where,

C_{VCC} = VCC capacitor

$I_{VCC\_normal2}$ = VCC supply current with active gate

t_{ss} = Soft-start time

During ABM condition, the VCC voltage may drop below the V_{VCC_OFF} because of the burst switching. Therefore, a higher capacitance is required than the calculated condition.

4.2 Soft-start

After the supply voltage of the IC exceeds V_{VCC_ON} (16 V typical), which corresponds to t_1 of Figure 3, the IC begins to switchwith a soft-start. The soft-start implemented here is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with four steps (see Figure 4). If not limited by other functions, the peak voltage on the

CS pin will increase incrementally from 0.3 V to V_{CS_N} (0.8 V). When the output voltage reaches its regulated value, the normal FB loop will take over the control.

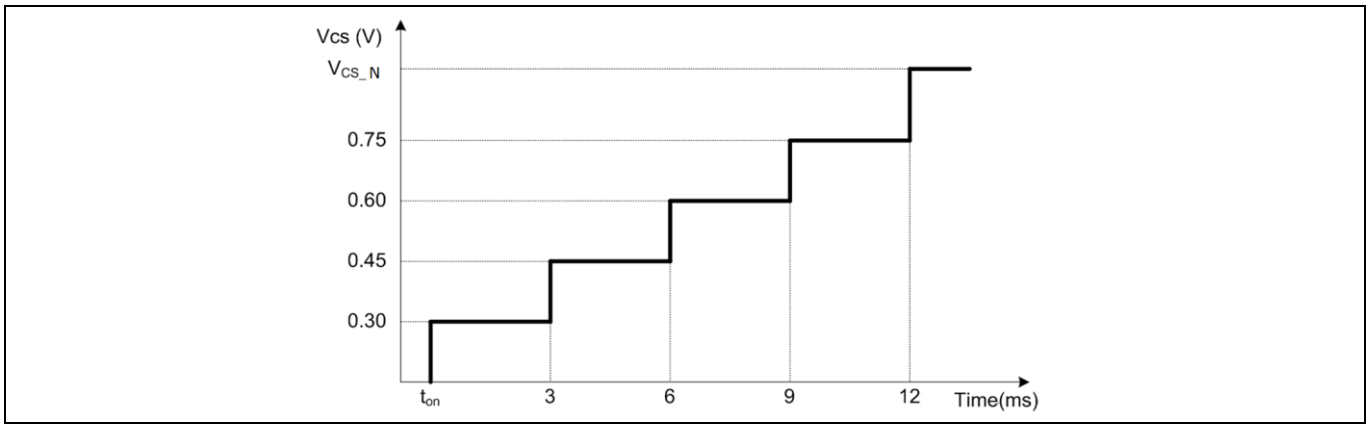

Figure 4 Maximum CS voltage during soft-start

4.3 Normal operation

During normal operation the pulse-width modulation (PWM) controller consists of: digital signal processing regulation control, analog circuit, current measurement unit, and a comparator. Details of normal operation are given in the following sections.

4.3.1 PWM operation and peak-current mode control

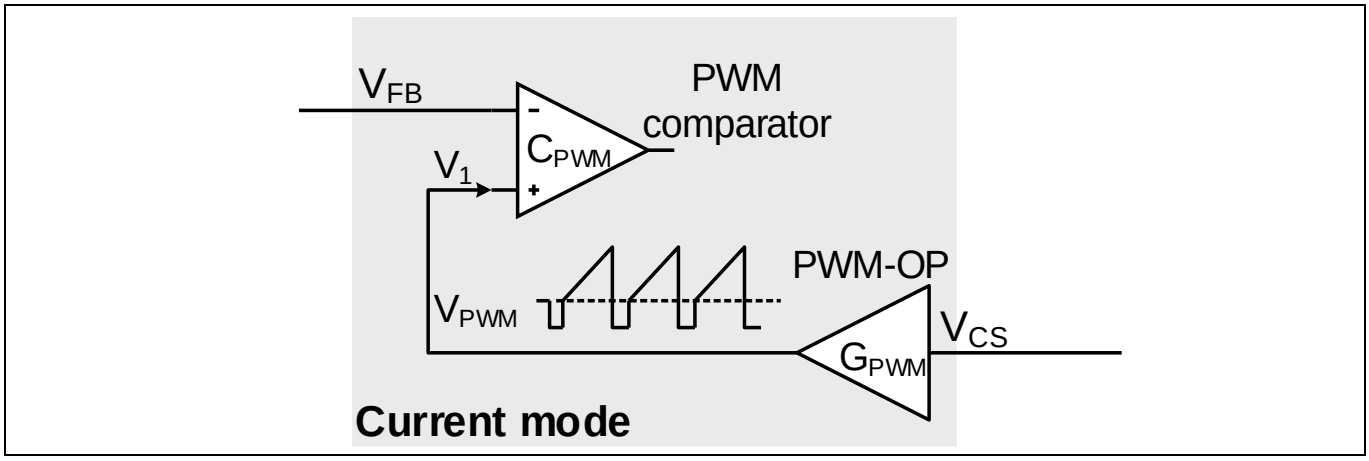

Figure 5 Pulse width modulation (PWM) block

4.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator, with a switching frequency F_{SW} that corresponds to the voltage level V_{FB} (see Figure 7).

4.3.1.2 Switch-off determination

In PCM control, the PWM comparator monitors the instantaneous voltage V_1 of the power MOSFET (see Figure 5). When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the MOSFETs gate. Therefore, the peak current of the power MOSFET is controlled by the FB voltage V_{FB} (see Figure 6).

During the switch-on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch-off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn-on time of the power MOSFET is t_{CS_LEB}.

If the voltage level at V_1 takes a long time to exceed V_{FB}, the IC will implement a maximum duty-cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75.

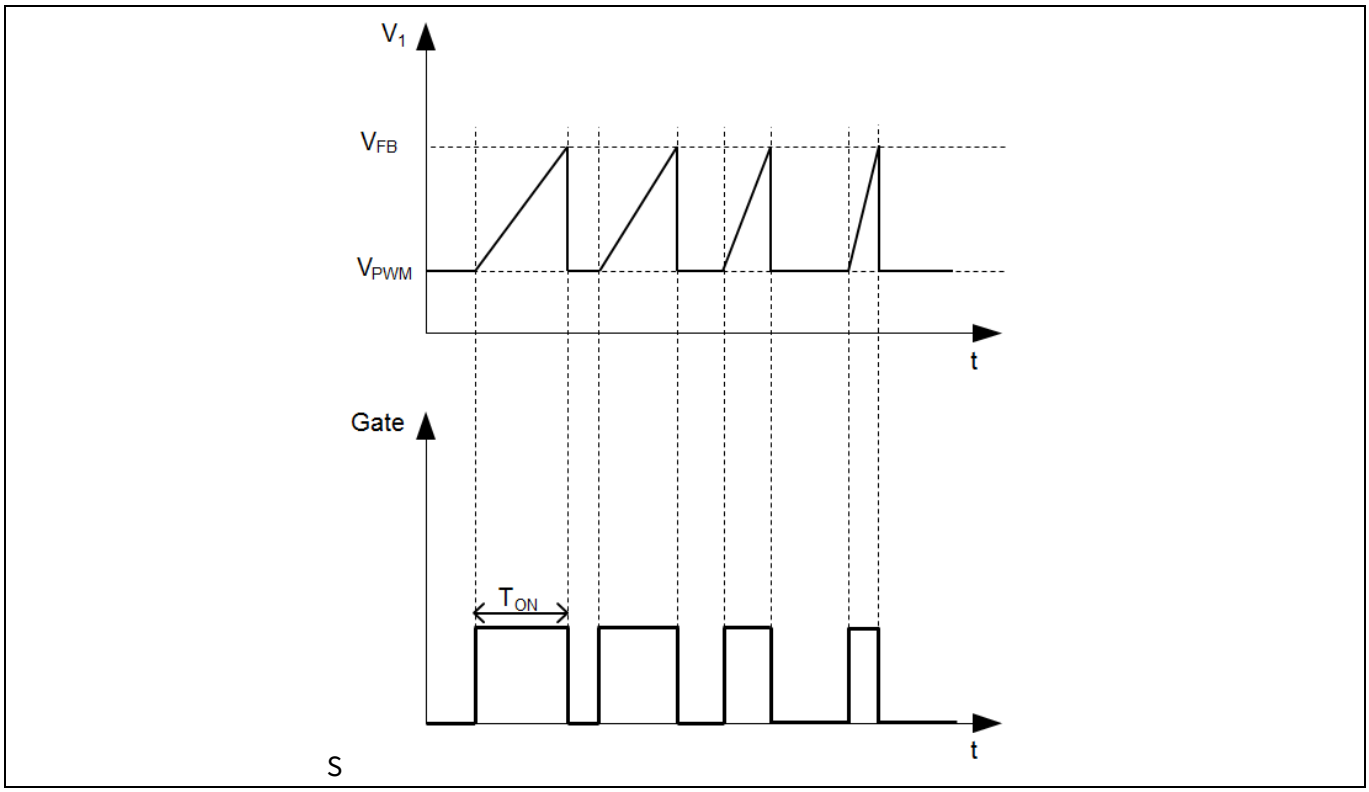

Figure 6 PWM signal

4.3.2 Current sensing

The power MOSFET current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then added with an offset V_{PWM} to become V_1, as described in the following equation.

$$V_{CS} = I_D \times R_{CS}$$

Equation 3 Current sensing voltage

Where,

V_{CS} = CS pin voltage

I_D = Power MOSFET current

R_{CS} = Resistance of the CS resistor

$$V_1 = V_{CS} * G_{PWM} + V_{PWM}$$

Equation 4 Voltage level

Where,

V_1 = Voltage level compared to V_{FB} as described in section 4.3.1.2

G_{PWM} = PWM-OP gain

V_{PWM} = Offset for voltage ramp

4.3.3 Frequency reduction

Frequency reduction is implemented to achieve better efficiency at light load conditions. This is achieved by reducing switching frequency F_{SW} , which improves efficiency by reducing the switching losses.

When the load decreases, V_{FB} decreases as well. F_{SW} is dependent on the V_{FB} as shown in Figure 7. Therefore, F_{SW} decreases as the load decreases.

Typically, F_{SW} at high load is 65 kHz and starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reaches the f_{OSCx_MIN}, even if the load is further reduced.

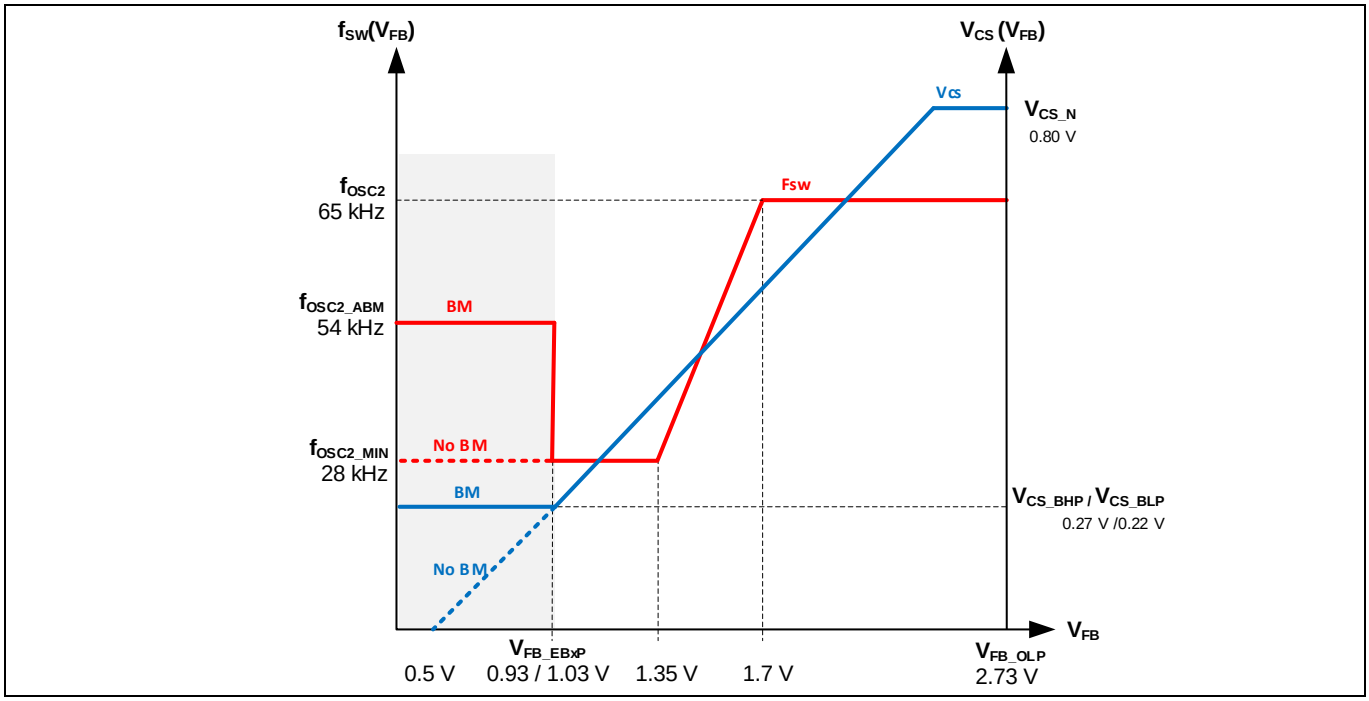

Figure 7 Frequency reduction curve

4.3.4 Slope compensation

In CCM operation, a duty cycle greater than 50 percent may generate a sub-harmonic oscillation. A small perturbation on the transformer flux φ can result in loop instability where the system cannot auto-correct itself, as can be seen in the figure below right, where $\Delta\varphi_2$ is greater than $\Delta\varphi_1$. For a stable system, $\Delta\varphi_2$ should be less than $\Delta\varphi_1$ (figure below, left). DCM operation is more stable as the transformer flux always goes to zero.

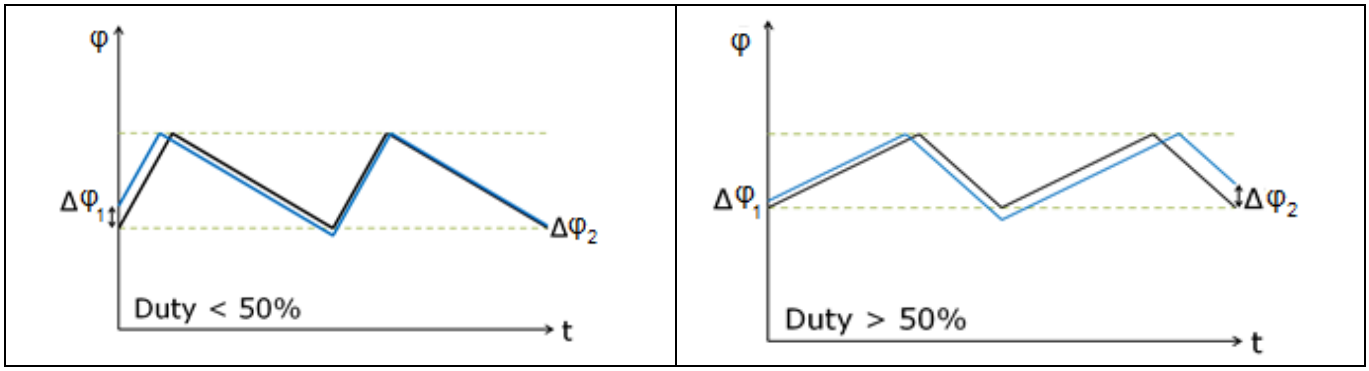

Figure 8 Perturbed transformer charging and discharging flux (black line is the stabilized transformer flux)

ICE5BRxxxxBZx-1 can operate in CCM. To avoid sub-harmonic oscillation, slope compensation is added to V_{CS} when the power MOSFETs gate is turned on for more than 40 percent of the switching cycle period. The relationship between V_{FB} and the V_{CS} for CCM operation is described in the equation below:

$$V_{\mathrm{FB}} = V_{\mathrm{CS}} * G_{\mathrm{PWM}} + V_{\mathrm{PWM}} + M_{\mathrm{COMP}} * (T_{\mathrm{ON}} - 40\% * T_{\mathrm{PERIOD}})$$

Equation 5 CCM operation

where ,

T_{ON} = Gate turn-on time of the power MOSFET

M_{COMP} = Slope compensation rate

T_{PERIOD} = Switching cycle period

As a result of slope compensation, $\Delta\phi_2$ is reduced to smaller values than $\Delta\phi_1$.Therefore, the system is able to stabilize itself as shown in the figure below.

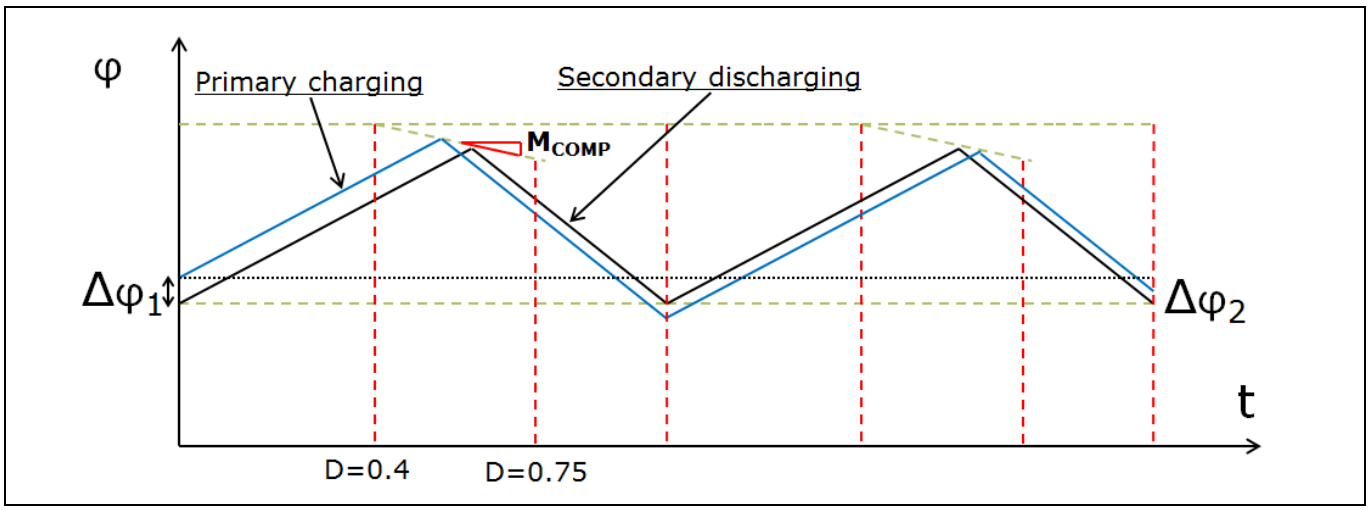

Figure 9 Perturbed transformer flux with slope compensation

The slope compensation circuit is disabled and no slope compensation is added to the V_{CS} pin during ABM to save on power consumption.

4.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 65 kHz with frequency jittering of ±4 percent for a jittering period of T_{JITTER} (4 ms). The frequency jittering primarily helps to reduce conducted EMI.

A capacitor, current source, and current sink that determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor is internally trimmed to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

4.3.6 Modulated gate drive

The drive stage is optimized for EMI consideration. The switch-on speed is slowed down before it reaches the power MOSFET turn-on threshold. There is a slope control on the rising edge at the output of the driver (see Figure 10). In this way the leading switch spike during turn-on is minimized.

The gate drive is 10 V (V_{GATE_HIGH}). For a 1 nF load capacitance, the typical values of rise and fall time are 117 ns and 27 ns respectively.

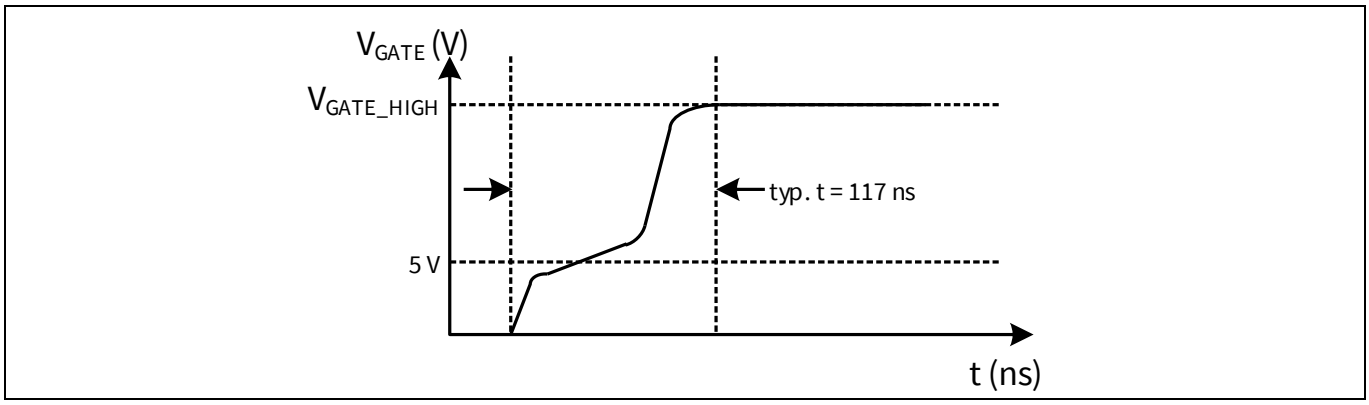

Figure 10 Gate – rising waveform

Note: Do not add a gate discharge resistor on the gate of the power MOSFET or the GATE pin. The discharge resistor together with the RStartUp forms a voltage divider. If the resistance ratio between $R_{StartUp}$ and the discharge resistor is high, then the gate voltage of the power MOSFET may not be enough to turn it on and charge the VCC to exceed V_{VCC_ON}. Similarly, connecting a voltage probe on the GATE pin may result in a non-start-up or a longer start-up time, depending on the probe resistance.

4.4 Peak-current limitation

There is a cycle-by-cycle PCL realized by the current limit comparator to provide primary overcurrent protection (OCP). The primary current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{PEAK\_PRI} = V_{CS\_N}/R_{CS}$$

Equation 6 Primary peak current

Where,

I_{PEAK_PRI} = Maximum peak current in the primary

V_{CS_N} = Threshold voltage for the PCL

R_{CS} = Resistance of the CS resistor

To avoid mis-triggering caused by MOSFET switch-on transient voltage spikes, a leading-edge blanking (LEB) time (t_{CS_LEB}) is integrated into the CS path.

Note: In case of high switch-on noise at the CS pin, the IC may switch off immediately after the LEB time, especially at light-load high-line conditions. To avoid this, a noise-filtering ceramic capacitor, for example, 100 pF~100 nF, can be added across CS pin and GND pin.

4.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching off the power MOSFET. An overshoot on the peak current I_{peak} caused by the delay depends on the ratio of dI/dt of the primary current (see Figure 11).

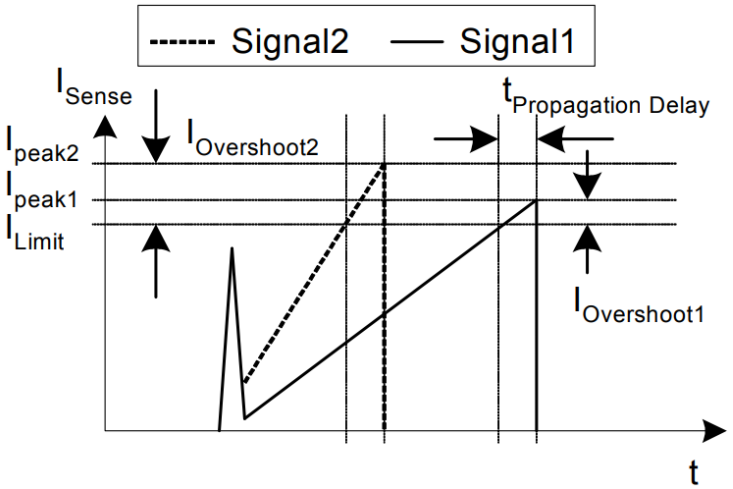

Figure 11 Current limit behavior

The overshoot of Signal2 is larger than Signal1 due to its steeper waveform. The change in the slope of the waveform depends on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Therefore, the propagation delay time between the exceeding CS threshold V_{CS_N} and the switching off of the power MOSFET is compensated over a wide bus voltage range. The current limiting becomes more accurate resulting in a minimum difference of overload protection triggering power between low and high AC-line input voltage.

Under CCM operation, the same V_{CS} does not result in the same power. To achieve a close overload triggering level for CCM, ICE5BRxxxxBZx-1 has implemented a two-curve compensation, as shown in Figure 12. One of the curves is used for T_{ON} greater than 0.40 duty cycle and the other is for T_{ON} lower than 0.40 duty cycle.

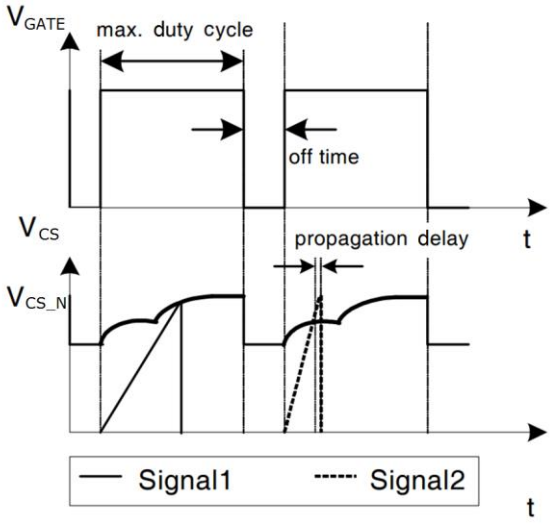

Figure 12 Dynamic voltage threshold V_{CS_N}

Similarly, the same concept of propagation delay compensation is implemented in ABM at a reduced level. With this implementation, the entry and exit burst mode power can remain close between low and high AC-line input voltage.

4.5 ABM with selectable power level

At light load, the IC enters ABM operation to minimize power consumption. Details of ABM operation are explained in the following sections.

4.5.1 Entering ABM operation

The system will enter ABM operation when two conditions are met:

- The FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP} depending on burst configuration option setup
- A certain blanking time t_{FB_BEB}.

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output current is very low.

The threshold output current to enter burst mode can be determined using the following equation.

$$I_{OUT\_enter\_burst} = \frac{L_P \cdot V_{DCIN} \cdot f_{OSC2_{MIN}}}{2 \cdot V_{OUT} \cdot (V_{DCIN} - V_{OUT})} \left(\frac{V_{FB_{EBxP}} - V_{PWM}}{R_{CS} \cdot G_{PWM}} \right)^2$$

Equation 7 Threshold output current

Where,

L_P = Buck inductance

V_{DCIN} = DC input voltage

f_{OSC2_MIN}= Minimum switching frequency

V_{OUT} = Output voltage

V_{FB_EBxP} = V_{FB} entering ABM

4.5.2 During ABM operation

After entering ABM, the PWM section will be inactive, making the V_{OUT} to decrease. As the V_{OUT} starts decreases, V_{FB} begins to rise. Once V_{FB} exceeds V_{FB_BOn}, the internal circuit is again activated by the internal bias to start the switching.

If the PWM is still operating and the output current is still low, V_{OUT} increases and the V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again.The PWM section is disabled, with no switching until V_{FB} increases and once again exceeds the V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn}, as shown in Figure 13.

During ABM, the switching frequency f_{OSC2_ABM} is 54 kHz. The peak current I_{PEAK_ABM} of the power MOSFET is defined as follows:

$$I_{\mathrm{PEAK\_ABM}} = V_{\mathrm{CS\_BxP}}/R_{\mathrm{CS}}$$

Equation 8 Peak current of the power MOSFET

Where,

V_{CS_BxP} = PCL in ABM

4.5.3 Leaving ABM operation

The FB voltage rapidly increases if there is a sudden increase in the output current. When V_{FB} exceeds V_{FB_LB}, it will leave ABM and the PCL threshold voltage will return to V_{CS_N} immediately.

The output current on leaving ABM can be determined using the following equation.

$$I_{OUT\_leave\_burst} = \frac{L_P \cdot V_{DCIN} \cdot f_{OSC2_{ABM}}}{2 \cdot V_{OUT} \cdot (V_{DCIN} - V_{OUT})} \left(\frac{V_{CS_{BxP}}}{R_{CS}}\right)^2$$

Equation 9 Current on leaving ABM

Where,

f_{OSC2_ABM} = ABM switching frequency

V_{CS_BxP} = PCL in ABM

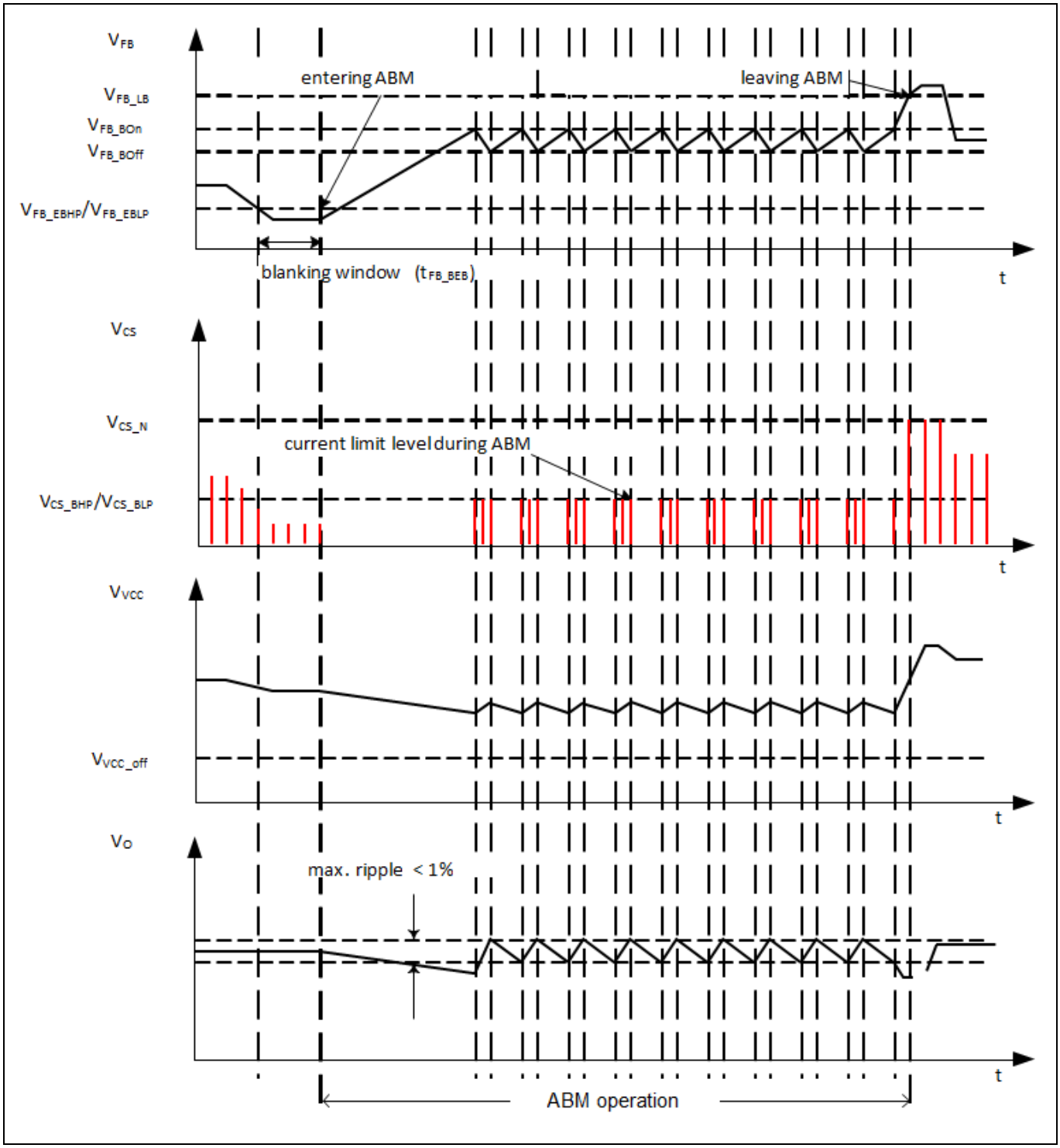

Figure 13 Signals in ABM

4.5.4 ABM configuration

The burst mode entry level can be selected by changing the resistance R_{Sel} at the FB pin. There are three configuration options depending on R_{Sel}, which correspond to the options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit levels with the FB voltage.

Table 3 ABM configuration options set-up

Option	R_{Sel}	V_{FB}	V_{CS_BxP}	Entry level	Exit level
				V_{FB_EBxP}	V_{FB_LB}
1	400 - 470 kΩ	V_{FB} less than $V_{FB\_P\_BIAS1}$	–	–	–
2	720~790 kΩ	$V_{FB\_P\_BIAS1}$ less than V_{FB} less than $V_{FB\_P\_BIAS2}$	0.22 V	0.93 V	2.73 V
3 (default)	Greater than 1210 kΩ	V_{FB} greater than $V_{FB\_P\_BIAS2}$	0.27 V	1.03 V	2.73 V

During start-up of the IC, the controller presets the ABM selection to Option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see Figure 14) and a current source I_{Sel} is turned on instead. From VCC = 4.4 V to the VCC on-threshold, the FB pin will source current I_{Sel} through R_{Sel} and external FB network. When VCC reaches the VCC on-threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option, and the current source (I_{Sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit.

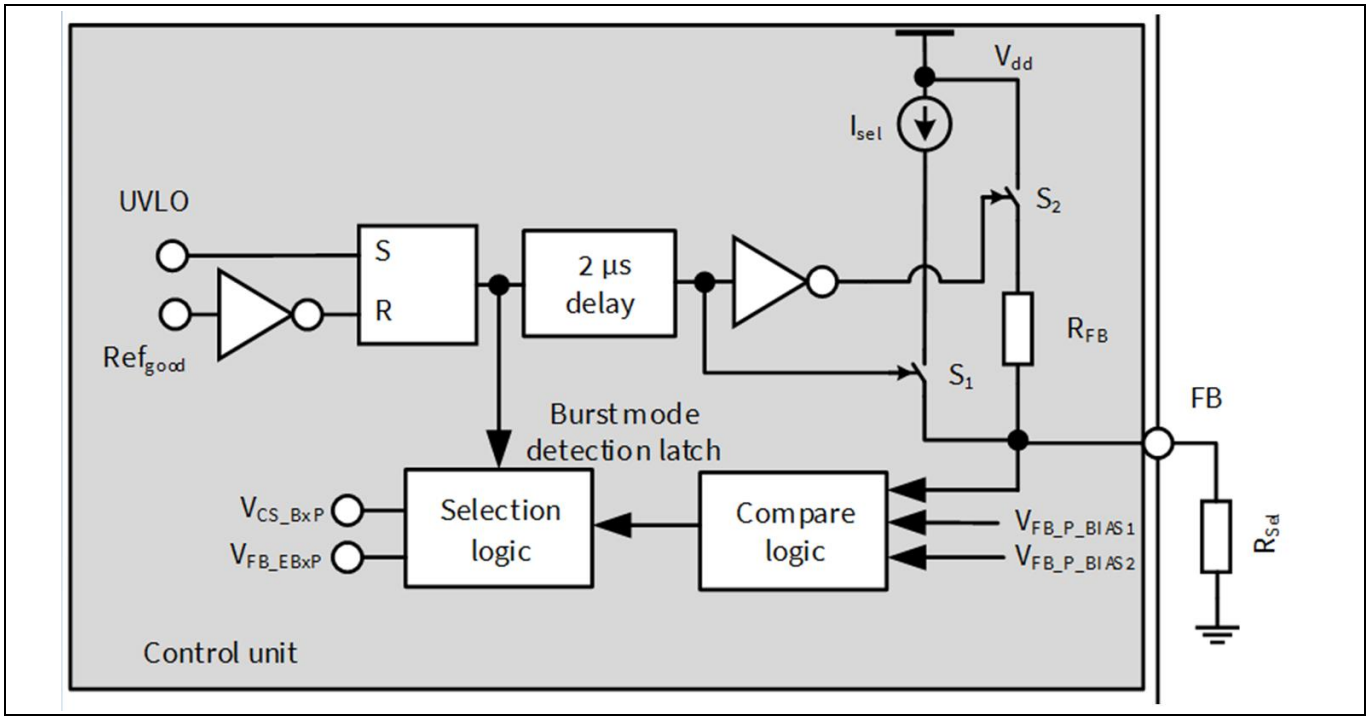

Figure 14 ABM detection and configuration

4.6 Output regulation

The VERR pin, which is connected to the input of an integrated error amplifier, is used for output regulation. The voltage divider R_h and R_l (see Figure 2) is used to sense the output voltage and compare it with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation. To properly enable the integrated error amplifier, the minimum resistance for the parallel combination of resistors R_h and R_l is calculated using the following equation:

$$R_{h//l} \geq V_{ERR\_P\_BIAS\_max} / I_{ERR\_P\_BIAS\_min} = 0.24\,V / 9.5\mu A = 25.3\,k\Omega$$

Equation 10 Minimum resistance for the parallel combination

Where,

$R_{h//l}$ = Parallel combination resistance of R_h and R_l

$V_{ERR\_P\_BIAS\_max}$ = Maximum voltage for error amplifier mode

$I_{ERR\_P\_BIAS\_min}$ = Minimum bias current for error amplifier mode

The output voltage V_{OUT} is set by R_h and R_l using the following equation :

$$R_h = R_l \cdot \left(\frac{V_{OUT}}{V_{ERR_{REF}}} - 1 \right)$$

Equation 11 Output voltage divider resistor

Where,

R_h and R_l = Voltage divider resistors

V_{ERR_REF} = Error amplifier reference voltage

Note: A dummy load resistor is necessary to prevent the output voltage from going out of regulation at no-load condition. A 10 kΩ resistor is recommended but it can be adjusted depending on the acceptable voltage regulation and no-load input power requirement.

4.6.1 V_{OUT} minimum

With reference to the typical application circuit in Figure 2, the output voltage is limited to a minimum value to prevent the ICE5BRxxxxBZx-1 from mis-triggering the VCC UVP. The recommended minimum output voltage V_{OUT_MIN1} can be determined using the following formula.

$$V_{OUT\_MIN1} = V_{VCC\_OFF\_max} + V_{f\_D2} + V_{f\_Daux}$$

Equation 12 Minimum output voltage V_{OUT_MIN1}

Where,

$V_{VCC\_OFF\_max}$ = Maximum value of VCC turn-off threshold voltage

V_{f_D2} = Forward voltage of diode D2

V_{f_Daux} = Forward voltage of diode D_{aux}

Apart from VCC UVP limitation, the minimum output voltage is also limited by the minimum on-time of the power MOSFET. The controller can only limit the peak current if the on-time is more than the LEB time. The on-time reduces as the input voltage increase. To properly control the peak current, the minimum voltage V_{OUT_MIN2} can be determined using the following formula.

$$V_{OUT\_MIN2} = V_{DCIN\_PK} \cdot t_{CS\_LEB\_max} \cdot f_{OSC2\_max}$$

Equation 13 Minimum output voltage V_{OUT_MIN2}

Where,

V_{DCIN_PK} = Peak input voltage

$t_{CS\_LEB\_max}$ = Maximum LEB time

f_{OSC2_max} = Maximum fixed oscillator frequency

The minimum output voltage should be chosen as the higher of V_{OUT_MIN1} or V_{OUT_MIN2}.

4.6.2 V_{OUT} maximum

With reference to the typical application circuit in Figure 2, the maximum output voltage is limited by the VCC OVP and can be determined from the following formula.

$$V_{OUT\_MAX} = V_{VCC\_OVP\_min} + V_{f\_D2} + V_{f\_Daux}$$

Equation 14 Maximum output voltage

Where,

$V_{VCC\_OVP\_min}$ = Minimum value of VCC OV threshold

V_{f_D2} = Forward voltage of diode D2

V_{f_Daux} = Forward voltage of diode D_{aux}

4.7 Protection functions

The ICE5BRxxxxBZx-1 provides numerous protection functions that considerably improve the power supply system robustness, safety, and reliability. The following table summarizes these protection functions and the corresponding protection modes, whether non-switch auto-restart, auto-restart , or odd-skip auto-restart. See Figure 15, Figure 16, and Figure 17 for the waveform illustration of the protection modes.

Table 4 Protection functions

Protection functions	Normal mode	Burst mode		Protection mode
		Burst on	Burst off	
VCC OV	√	√	NA[3]	Extended cycle-skip auto-restart
VCC UV	√	√	√	Auto-restart
Open-loop, overload	√	NA[1]	NA[1]	Extended cycle-skip auto-restart
Overtemperature	√	√	√	Non-switch auto-restart

[3] Not applicable

Protection functions	Normal mode	Burst mode		Protection mode
		Burst on	Burst off	
VCC short-to-GND	√	√	√	No start-up

4.7.1 VCC OV/UV

During operation, the VCC voltage is continuously monitored. If VCC is either below V_{VCC_OFF} for 50 µs ($t_{VCC\_OFF\_B}$) or above V_{VCC_OVP} for 55 µs ($t_{VCC\_OVP\_B}$), the power MOSFET is kept switched off. After the VCC voltage falls below the threshold V_{VCCoff}, the new start-up sequence is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft-start.

4.7.2 Open-loop, overload

In case of open control-loop, output overload or output short, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters odd-skip auto-restart mode. The blanking time enables the converter to provide peak power in case the increase in V_{FB} is due to a sudden load increase.

During output short, the system enters deep CCM. The MOSFET on-time is equal to CS LEB time (t_{CS_LEB}). Because the controller is unable to control the current during t_{CS_LEB}, the MOSFET current can exceed the current rating specifically at maximum input voltage. Also, the MOSFET can enter the linear region. As such, the MOSFET losses will be very high and may exceed the maximum junction temperature. One way to reduce the MOSFET current is to add a resistor R_s in series with the buck inductor. A higher resistor value can reduce the current significantly, but it is an additional loss in the system. Therefore, the resistor value should be adjusted as low as possible, just enough to meet the safe operating range of the MOSFET. To reduce the CoolSET™ temperature, increasing VCC capacitor value can help by making the auto-restart time longer.

4.7.3 Overtemperature

If the junction temperature of the controller exceeds T_{Jcon_OTP} (140 °C typical.), the IC enters an overtemperature protection (OTP) in auto-restart mode. The IC is also implemented with a 40 °C (typical.) hysteresis. That means, the IC can be recovered from OTP only when the controller junction temperature drops 40°C lower than the overtemperature trigger point.

4.7.4 VCC short-to-GND

To limit the power dissipation of the start-up circuit at VCC short-to-GND, the VCC charging current is limited to a minimum level of $I_{VCC\_Charge1}$ when the VCC voltage is below V_{VCC_SCP} (1.1 V typical.). With such low current, the power loss of the IC is limited to prevent overheating.

4.7.5 Protection modes

All the protections are in auto-restart mode with a new soft-start sequence. The three auto-restart modes are illustrated in the following figures.

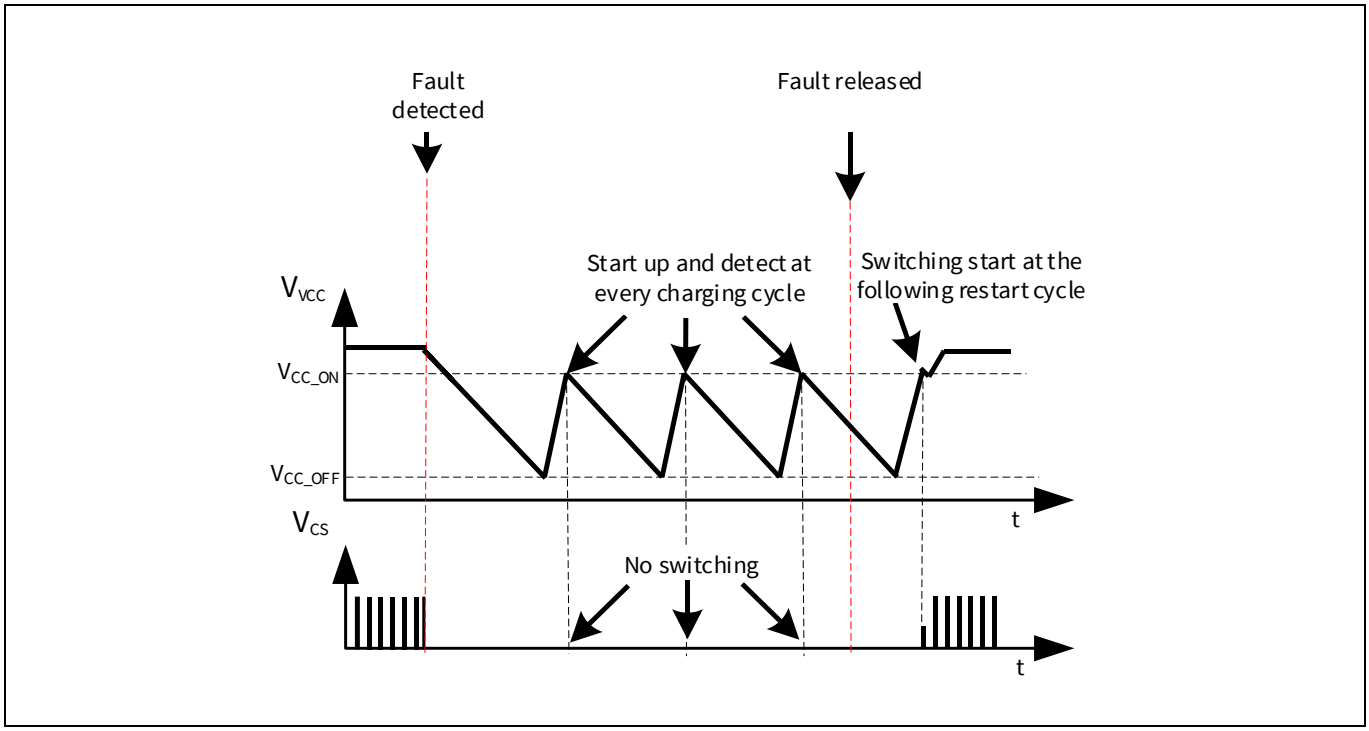

Figure 15 Non-switch auto-restart mode

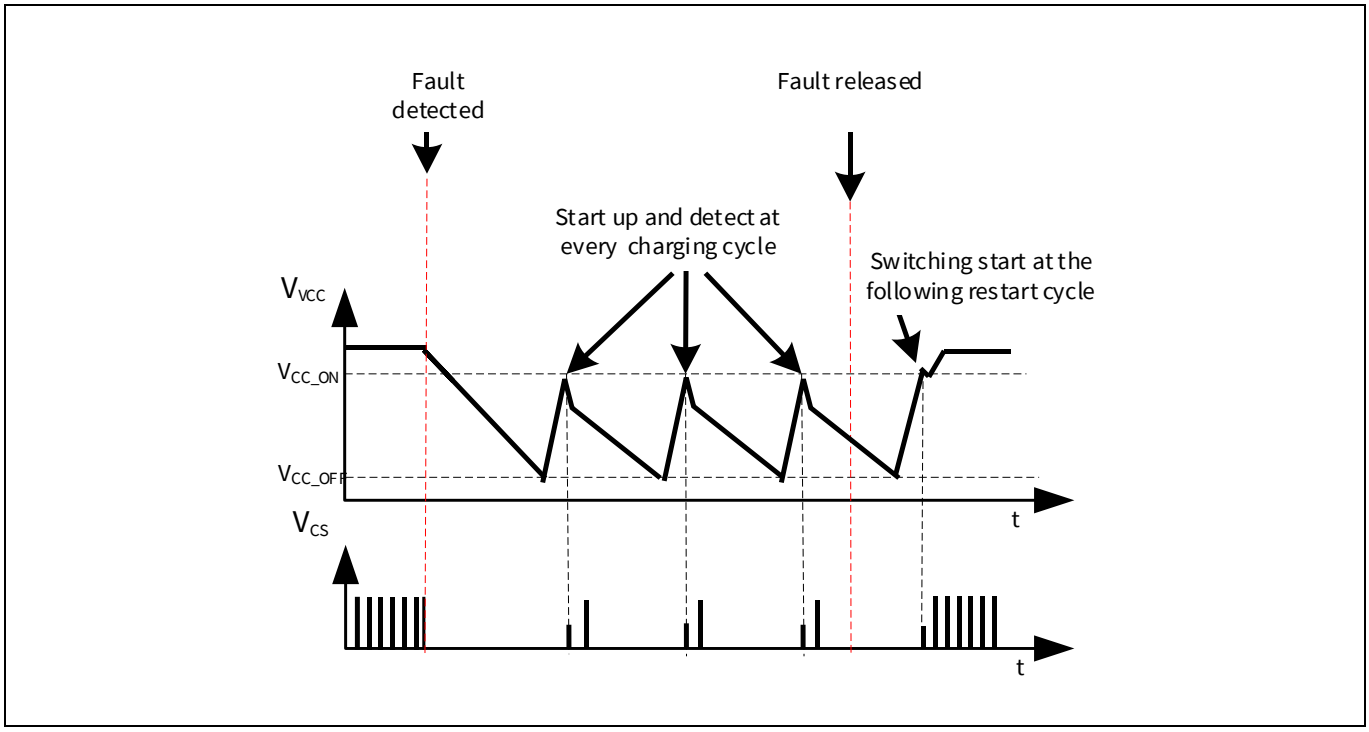

Figure 16 Auto-restart mode

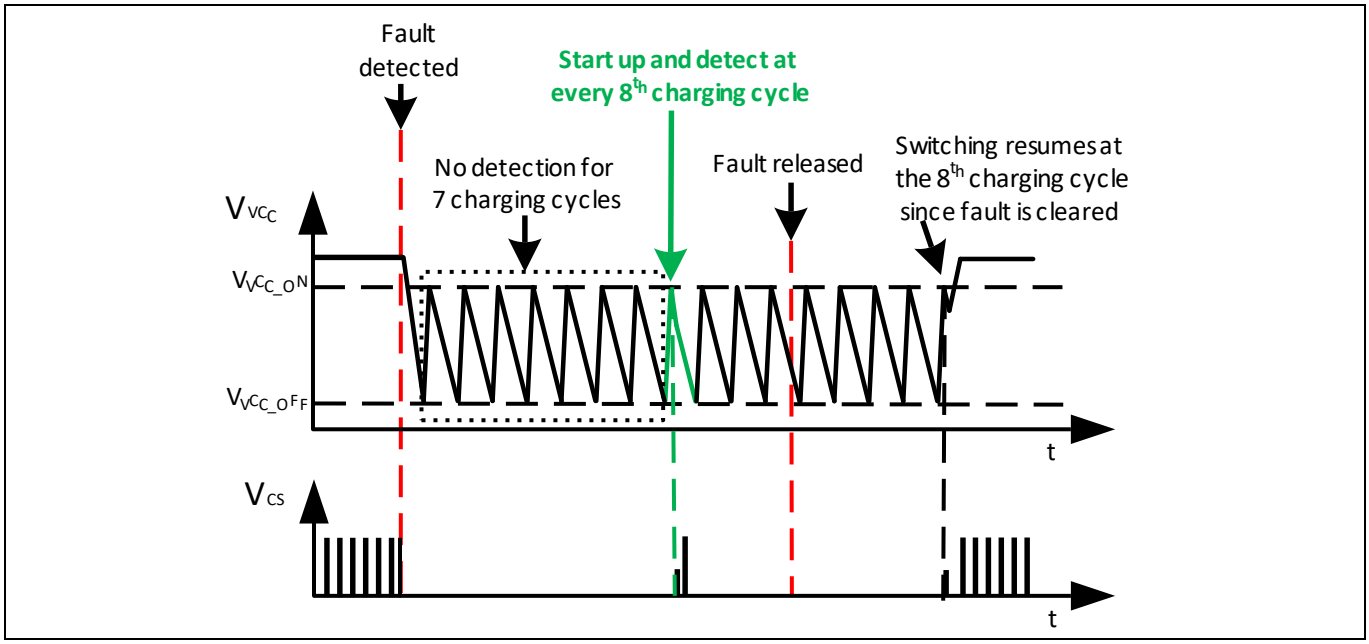

Figure 17 Extended cycle skip auto-restart

5 Schematic

A 700 mA demo board schematic circuit with ICE5BR2280BZ-1 is shown in the following figure.

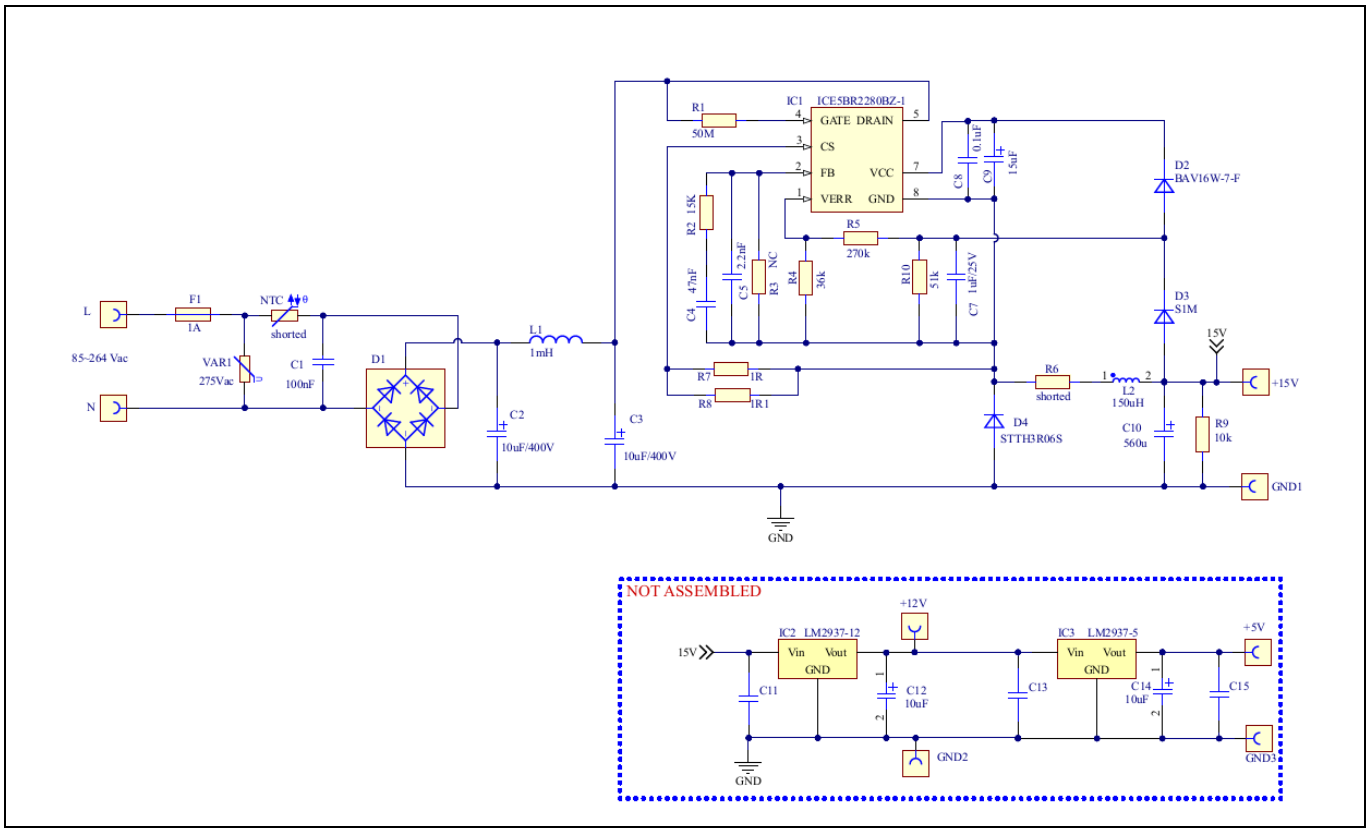

Figure 18 Schematic of EVAL_5BR2280BZ-1_700mA1

6 PCB layout and design recommendations

In an SMPS, the PCB layout is crucial for a successful design. The following are the recommendations for PCB layout .

1. Minimize the HV and high-current switching loop formed by the bulk capacitor, main power switch (power switch CoolMOS™ inside the CoolSET™), CS resistor, buck inductor, output capacitor, and buck diode.
2. Place the filter capacitor close to the controller ground: Filter capacitors (C4, C5, and C8 in Figure 18) should be placed closer to the controller ground and the controller pin to reduce the switching noise coupled into the controller.
3. As the CoolSET™ is configured in high-side switch buck configuration, maintain sufficient PCB trace clearance between the CoolSET™ components,bus voltage and primary ground.
4. It is recommended to increase the copper area at the DRAIN pin on the PCB for better thermal performance of the CoolSET™.

To reduce the switching losses during CCM operation, an ultra-fast freewheeling diode (D4 in Figure 18) with a reverse recovery time (t_{rr}) of 35 ns or less is recommended.

7 Output current of CoolSET™ 5th Generation Fixed Frequency Plus ICs

Table 5 Output current of CoolSET™ 5th Generation Fixed Frequency Plus controllers

Type	Package	Marking	V_{DS}	F_{SW}	$R_{DS(on)}$[4]	85~265 V AC at DCM[5]	Typical output voltage
ICE5BR4780BZ-1	PG-DIP-7	5BR4780BZ-1	800 V	65 kHz	4.13 Ω	450 mA	15 V
ICE5BR3995BZ-1	PG-DIP-7	5BR3995BZ-1	950 V	65 kHz	3.46 Ω	550 mA	
ICE5BR2280BZ-1	PG-DIP-7	5BR2280BZ-1	800 V	65 kHz	2.13 Ω	700 mA	

Figure 19 shows typical output current vs. ambient temperature.The curves are derived based on an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET for CoolSET™), using the minimum 100 mm² drain pin copper area in a 2 oz. copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The following figures are for selection purposes only. The actual current can vary depending on the specific design.

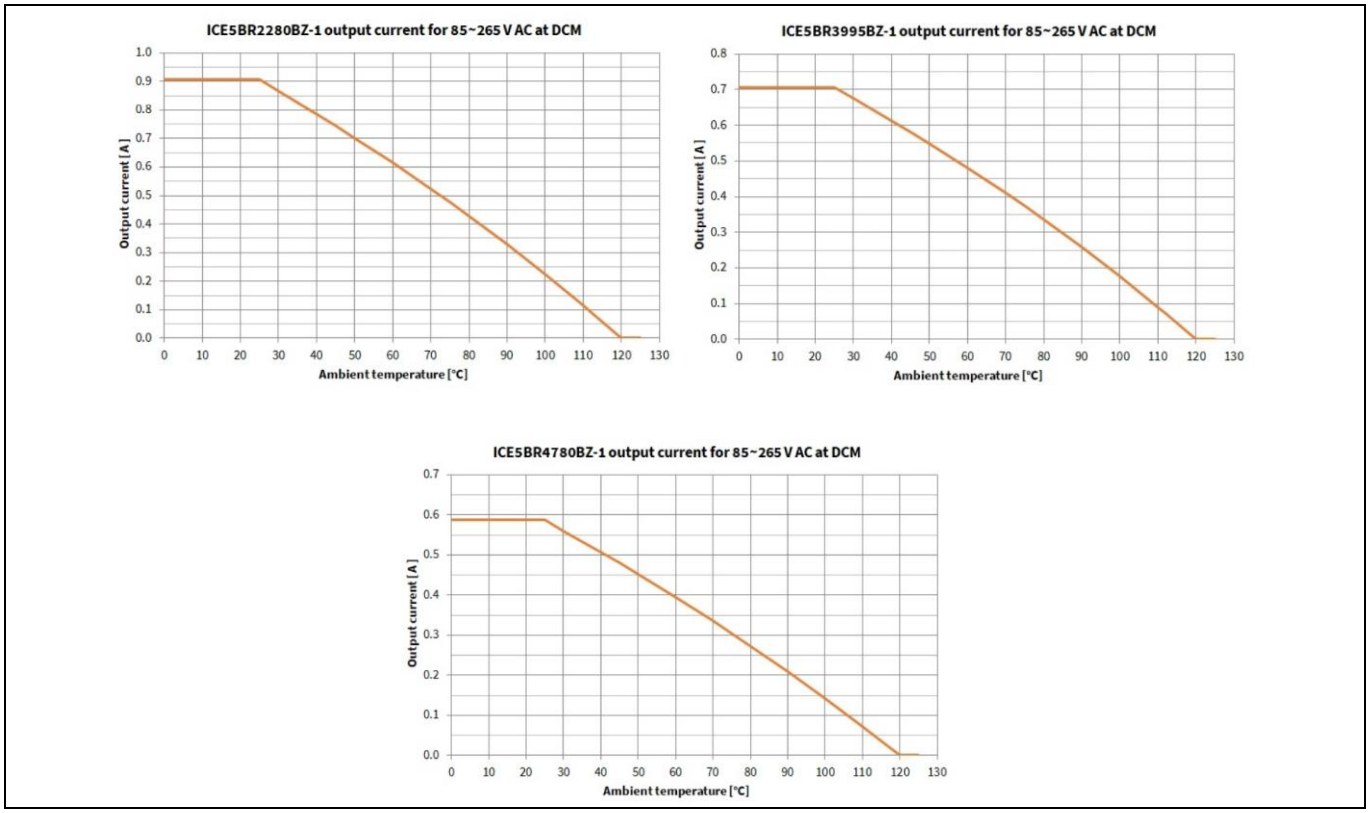

Figure 19 Output current curve of ICE5BRxxxxBZx-1

[4] Typically at T_j = 25°C (inclusive of low-side MOSFET).

[5] Calculated maximum output currrent rating in an open frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET) and using minimum 100 mm² drain pin copper area in a 2 oz. copper single-sided PCB. The output current figure is for selection purposes only. The actual power can vary depending on the design. Contact Technical support from Infineon for more information.

8 5th Generation Fixed Frequency Plus buck design example

A design example of a 700 mA 15 V FF HV buck converter with ICE5BR2280BZ-1 is shown below.

Table 6 Parameters

Define input parameters	Symbol	Value
Minimum AC input voltage	V_{ACMin}	85 V AC
Maximum AC input voltage	V_{ACMax}	264 V AC
Line frequency	f_{AC}	60 Hz
Bulk capacitor DC ripple voltage	$V_{DCRipple}$	40 V
Output voltage	V_{OUT}	15 V
Output current	I_{OUT}	0.7 A
Efficiency	η	80 %
CoolSET™ 5th Generation Fixed Frequency Plus	CoolSET™	ICE5BR2280BZ-1
Switching frequency	f_s	65 kHz
Maximum ambient temperature	T_a	50 °C

8.1 Power

Nominal output power :

$$P_{outNom} = V_{out} \cdot I_{out} \quad \Rightarrow \quad P_{outNom} = 15V \cdot 0.7A = 10.5W$$

Equation 15

Maximum input power :

$$P_{InNom} = \frac{P_{OutNom}}{\eta} \quad \Rightarrow \quad P_{InNom} = \frac{10.5W}{0.80} = 13.13W$$

Equation 16

8.2 Diode bridge

Maximum AC input current:

Power factor cosφ 0.6

$$I_{ACRMS} = \frac{P_{InMax}}{V_{ACMin} \cdot cos\,\phi} \quad \Rightarrow \quad I_{ACRMS} = \frac{13.13W}{85V \cdot 0.6} = 0.257A$$

Equation 17

Maximum DC input voltage:

$$V_{DCMaxPk} = V_{ACMax} \cdot \sqrt{2} \quad \Rightarrow \quad V_{DCMaxPk} = 264V \cdot \sqrt{2} = 373.35V$$

Equation 18

8.3 Input capacitor

Peak voltage at minimum AC input:

$$V_{DCMinPk} = V_{ACMin} \cdot \sqrt{2} \quad \Rightarrow \quad V_{DCMinPk} = 85V \cdot \sqrt{2} = 120.21V$$

Equation 19

Minimum DC input voltage setting:

$$V_{DCMinSet} = V_{DCminPk} - V_{DCRipple} \quad \Rightarrow \quad V_{DCMinSet} = 120.21V - 40V = 80.21V$$

Equation 20

Discharging time at each half-line cycle:

$$T_D = \frac{1}{4 \cdot f_{AC}} \cdot \left(1 + \frac{\sin^{-1}\frac{V_{DCMinSet}}{V_{DCMinPk}}}{90}\right) \quad \Rightarrow \quad T_D = \frac{1}{4 \cdot 60Hz} \cdot \left(1 + \frac{\sin^{-1}\frac{80.21V}{120.21V}}{90}\right) = 6.10ms$$

Equation 21

Required energy at discharging time of input capacitor:

$$W_{IN} = P_{InNom} \cdot T_D \quad \Rightarrow \quad W_{IN} = 13.13W \cdot 6.1ms = 0.08Ws$$

Equation 22

Calculated input capacitor:

$$C_{INCal} = \frac{2 \cdot W_{IN}}{V_{DCMinPk}^2 - V_{DCMinSet}^2} \quad \Rightarrow \quad C_{INCal} = \frac{2 \cdot 0.08Ws}{(120.21V)^2 - (80.21V)^2} = 19.99\mu F$$

Equation 23

Alternatively, a rule of thumb for estimating the input capacitor can be applied based on maximum input power, as follows:

Table 7 Input capacitor estimation

Input voltage	Factor
115 V AC	2 µF/W
230 V AC	1 µF/W
85 to 265 V AC	2 to 3 µF/W

Applying the rule of thumb using the 2 µF/W factor:

$$C_{INEst} = P_{INNom} \cdot factor \quad \Rightarrow \quad C_{INEst} = 13.13W \cdot \frac{2\mu F}{W} = 26.26\mu F$$

Equation 24

Choose a capacitance value that is greater than or equal to calculated as per Equation 23 or Table 7. The voltage rating should be greater than or equal to the maximum DC input voltage.

Input capacitor	C_{IN}	20 µF/400 V

Recalculation after input capacitor selection:

$$V_{DCMin} = \sqrt{V_{DCMinPk}^2 - \frac{2 \cdot W_{IN}}{C_{IN}}} \quad \Rightarrow \quad V_{DCMin} = \sqrt{(120.2V)^2 - \frac{2 \cdot 0.08W \cdot s}{20\mu F}} = 80.24V$$

Equation 25

Note: Special requirements for hold-up time, including cycle skip/dropout, or other factors that affect the resulting minimum DC input voltage and capacitor discharging time, are not considered above.

8.4 Buck inductance design

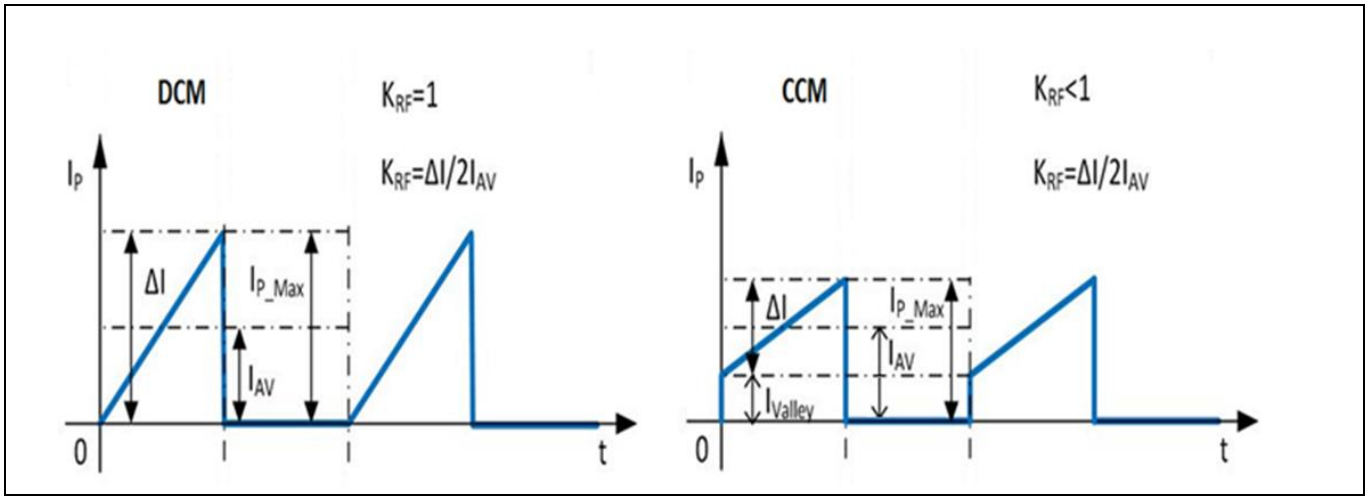

Figure 20 Drain current waveform

Maximum duty cycle:

$$D_{Max} = V_{Out}/V_{DCMin} \quad \Rightarrow \quad D_{Max} = 15V/80.24V = 0.19$$

Equation 26

Primary inductance:

$$L_P = \frac{D_{Max} \cdot (V_{DCMin} - V_{Out})}{2 \cdot I_{Out} \cdot K_{RF} \cdot f_s} \quad \Rightarrow \quad L_P = \frac{0.19 \cdot (80.24V - 15V)}{2 \cdot 0.7A \cdot 0.9 \cdot 65kHz} = 148.91\mu H$$

Equation 27

Input DC voltage for DCM operation:

$$V_{VIN_{DCM}} = \frac{V_{Out}^2}{V_{Out} - 2 \cdot f_S \cdot I_{Out} \cdot L_P} \quad \Rightarrow \quad V_{VIN_{DCM}} = \frac{(15V)^2}{15V - 2 \cdot 65kHz \cdot 0.7A \cdot 148.91\mu H} = 155.27V$$

Equation 28

Average current through inductor:

$$I_{AV} = I_{Out} \quad \Rightarrow \quad I_{AV} = 0.7A$$

Peak-to-peak current:

$$\Delta I = 2 \cdot I_{Out} \cdot K_{RF} \quad \Rightarrow \quad \Delta I = 2 \cdot 0.7A \cdot 0.9 = 1.26A$$

Equation 29

Peak current:

$$I_{PMax} = I_{AV} + \Delta I/2 \quad \Rightarrow \quad I_{PMax} = 0.7A + 1.26A/2 = 1.33A$$

Equation 30

Valley current:

$$I_{Valley} = I_{PMax} - \Delta I \quad \Rightarrow \quad I_{Valley} = 1.33A - 1.26A = 0.07A$$

Equation 31

MOSFET RMS current:

$$I_{PRMS} = \sqrt{\left[3I_{AV}^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{Max}}{3}} \quad \Rightarrow \quad I_{PRMS} = \sqrt{\left[3 \cdot (0.7A)^2 + \left(\frac{1.26A}{2}\right)^2\right]\frac{0.19}{3}} = 0.341A$$

Equation 32

RMS current through buck inductor:

$$I_{BuckRMS} = \sqrt{\left[3I_{AV}^2 + \left(\frac{\Delta I}{2}\right)^2\right]/3} \quad \Rightarrow \quad I_{PRMS} = \sqrt{\left[3 \cdot (0.7A)^2 + \left(\frac{1.26A}{2}\right)^2\right]/3} = 0.789A$$

Equation 33

8.5 Output rectifier

A low forward voltage and a very low reverse recovery time (t_{rr}) of 35 ns or less are recommended for a highly efficient design. The very low t_{rr} helps reduce switching losses, especially during CCM start-up and output short condition.

The output capacitor is necessary to minimize the output ripple and to provide necessary energy during high load jumps. Therefore, the output capacitor should have enough capacitance and low ESR, and meet the ripple current rating.

Diode reverse voltage at maximum AC input:

$V_{RDiode} = V_{DCMaxPk}$	⇒	$V_{RDiode} = 373.35V$

Diode RMS current at minimum AC input:

$I_{DRMS} = \sqrt{\left[3I_{AV}^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{1 - D_{Max}}{3}}$	⇒	$I_{DRMS} = \sqrt{\left[3 \cdot (0.7A)^2 + \left(\frac{1.26A}{2}\right)^2\right]\frac{1 - 0.19}{3}} = 0.71A$

Equation 34

Output capacitor:

Maximum voltage undershoot	ΔV_{Out1}	0.5 V
Number of clock periods	n_{CP}	20
$C_{OutCal} = \frac{I_{Out} \cdot n_{CP}}{\Delta V_{Out} \cdot f_s}$	⇒	$C_{OutCal} = \frac{0.7A \cdot 20}{0.5V \cdot 65kHz} = 431\mu F$
Output capacitor	C_{Out}	560 µF

Equation 35

8.6 CS resistor

The CS resistor value defines the peak current of the power MOSFET and buck inductor during normal operation. As the IC cycle-by-cycle PCL is defined by this resistor, it also defines the maximum output power delivered by the power MOSFET.

Maximum CS resistor:

PCL threshold	$V_{CS\_N\_min}$	0.72 V
$R_{sense} = V_{CS\_N\_min}/I_{PMax}$	⇒	$R_{sense} = 0.72V/1.33A = 0.54\Omega$

Equation 36

8.7 VCC capacitor

Calculate start-up time given VCC capacitor:

$I_{VCC\_Charge1}$ from datasheet	$I_{VCC\_Charge1}$	0.2 mA
$I_{VCC\_Charge3}$ from datasheet	$I_{VCC\_Charge3}$	3 mA
V_{VCC_ON} from datasheet	V_{VCC_ON}	16 V
V_{VCC_SCP} from datasheet	V_{VCC_SCP}	1.1 V
VCC capacitor	C_{VCC}	15 µF

Equation 37

8.8 Calculation of losses

Input diode bridge loss:

Diode bridge forward voltage	V_{FBR}	1 V
$P_{DIN} = V_{FBR} \cdot I_{ACRMS} \cdot 2$	⇒	$P_{DIN} = 1V \cdot 0.257A \cdot 2 = 0.51W$

Equation 38

Inductor copper loss:

DC resistance	R_{LCU}	0.2 Ω
$P_{LCU} = (I_{BuckRMS})^2 \cdot R_{LCU}$	⇒	$P_{LCU} = (0.789A)^2 \cdot 0.2\Omega = 0.12W$

Equation 39

Output rectifier diode loss:

Forward voltage of output diode	V_{FOut}	0.6 V
$P_{diode} = V_{FOut} \cdot I_{DRMS}$	⇒	$P_{diode} = 0.6V \cdot 0.71A = 0.43W$

Equation 40

CS resistor loss:

$$P_{CS} = (I_{PRMS})^2 \cdot R_{sense} \quad \Rightarrow \quad P_{CS} = (0.341A)^2 \cdot 0.54\Omega = 0.06W$$

Equation 41

MOSFET loss:

$R_{DS(on)}$ at T_J = 125°C from datasheet	R_{DSON}	4.31 Ω
$C_{o(er)}$ from datasheet	$C_{o(er)}$	7 pF
External drain-to-source capacitance	C_{DS}	0 pF

$$P_{SONMinAC} = \frac{1}{2} \cdot (C_{o(er)} + C_{DS}) \cdot (V_{DCMin})^2 \cdot f_s \quad \Rightarrow \quad P_{SONMinAC} = \frac{1}{2} \cdot (7pF) \cdot (80.24V)^2 \cdot 65kHz = 1.5mW$$

Equation 42

$$P_{condMinAC} = (I_{PRMS})^2 \cdot R_{DSON} \quad \Rightarrow \quad P_{condMinAC} = (0.341A)^2 \cdot 4.31\Omega = 0.5W$$

Equation 43

$$P_{MOSMinAC} = P_{SONMinAC} + P_{condMinAC} \quad \Rightarrow \quad P_{MOSMinAC} = 1.5mW + 0.5W = 0.5W$$

Equation 44

$$t_{ONMaxAC} = \sqrt{\frac{2 \cdot P_{OutNom} \cdot L_P}{V_{DCMaxPk} \cdot (V_{DCMaxPk} - V_{Out}) \cdot f_s}} \quad \Rightarrow \quad t_{ONMaxAC} = \sqrt{\frac{2 \cdot 10.5W \cdot 149\mu H}{373V \cdot (373V - 15V) \cdot 65kHz}} = 0.6\mu s$$

Equation 45

$$P_{SONMaxAC} = \frac{1}{2} \cdot (C_{o(er)} + C_{DS}) \cdot (V_{DCMaxPk})^2 \cdot f_s \quad \Rightarrow \quad P_{SONMaxAC} = \frac{1}{2} \cdot (7pF) \cdot (373V)^2 \cdot 65kHz = 32mW$$

Equation 46

$$I_{PRMSMaxAC} = \frac{t_{ONMaxAC} \cdot (V_{DCMaxPk} - V_{Out})}{L_P} \sqrt{\frac{t_{ONMaxAC} \cdot f_s}{3}} \quad \Rightarrow \quad I_{PRMSMaxAC} = \frac{0.6\mu s \cdot (373V - 15V)}{149\mu H} \sqrt{\frac{0.6\mu s \cdot 65kHz}{3}} = 0.165A$$

Equation 47

$$P_{condMaxAC} = (I_{PRMSMaxAC})^2 \cdot R_{DSON} \quad \Rightarrow \quad P_{condMaxAC} = (0.165A)^2 \cdot 4.31\Omega = 0.116W$$

Equation 48

$$P_{MOSMaxAC} = P_{SONMaxAC} + P_{condMaxAC} \quad \Rightarrow \quad P_{MOSMaxAC} = 32mW + 0.116W = 0.148W$$

Equation 49

Controller loss:

Controller current consumption IVCC_normal2 0.9 mA

$$P_{Ctrl} = (V_{Out} - 1.4V) \cdot I_{VCC\_normal2} \quad \Rightarrow \quad P_{Ctrl} = (15V - 1.4V) \cdot 0.9mA = 12mW$$

Equation 50

Total power loss:

$$P_{Losses} = P_{DIN} + P_{LCU} + P_{diode} + P_{CS} + P_{MOS} + P_{Ctrl} \quad \Rightarrow \quad P_{Losses} = 0.51W + 0.12W + 0.43W + 0.06W + 0.5W + 12mW = 1.64W$$

Equation 51

Efficiency after losses:

$$\eta_{Post} = P_{OutNom}/(P_{OutNom} + P_{Losses}) \quad \Rightarrow \quad \eta_{Post} = 10.5W/(10.5W + 1.64W) = 86.6\%$$

Equation 52

8.9 CoolSET™ temperature

CoolSET™ temperature:

Assumed junction-to-ambient thermal impedance (include copper pour)	R_{thJA_As}	100 K/W
$\Delta T = R_{thJA_{As}} \cdot P_{MOS}$	⇒	$\Delta T = \frac{100K}{W} \cdot 0.5W = 50.3K$
ΔT 50.3 K	≡	ΔT 50.3°C

Equation 53

$T_{jmax} = \Delta T + T_{amax}$	⇒	$T_{jmax} = 50.3\,°C + 50°C = 100.3°C$

Equation 54

8.10 Output regulation

Setting resistor dividers for output:

Select voltage divider RO1	R_{O1}	36 kΩ
$R_{O2} = \frac{R_{O1} \cdot (V_{Out} - 1.8V)}{1.8V}$	⇒	$R_{O2} = \frac{36k\Omega \cdot (15V - 1.8V)}{1.8V} = 264k\Omega$
R_{O2}	⇒	$270k\Omega$

Equation 55

References

[1] Infineon Technologies AG: *ICE5xRxxxxxBZx-1 datasheet*; Available online

[2] Infineon Technologies AG: *CoolSET™ 5th Generation Fixed Frequency Plus Calculation tool for buck;* Available online

[3] Infineon Technologies AG: *CoolSET™ 5th Generation Fixed Frequency Plus EVAL_5BR2280BZ-1_700mA1* (Contact Infineon Support to obtain this document).

Design support

Developer community

For a wider discussion with peers from industry to trade ideas regarding Infineon products, we welcome you to actively participate on the Infineon Developer Community.

Technical support

Have technical queries? Consult experts from Infineon to get a fast turn-around by raising a request on the Technical Support page or a local sales representative.

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V 1.0	2024-08-23	Initial release

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