



FDPC8014S

PowerTrench® Power Clip

25V Asymmetric Dual N-Channel MOSFET

Features

- Q1: N-Channel
- Max $r_{DS(on)}$ = 3.8 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$
 - Max $r_{DS(on)}$ = 4.7 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 18\text{ A}$
- Q2: N-Channel
- Max $r_{DS(on)}$ = 1.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 41\text{ A}$
 - Max $r_{DS(on)}$ = 1.4 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 37\text{ A}$
 - Low inductance packaging shortens rise/fall times, resulting in lower switching losses
 - MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
 - RoHS Compliant

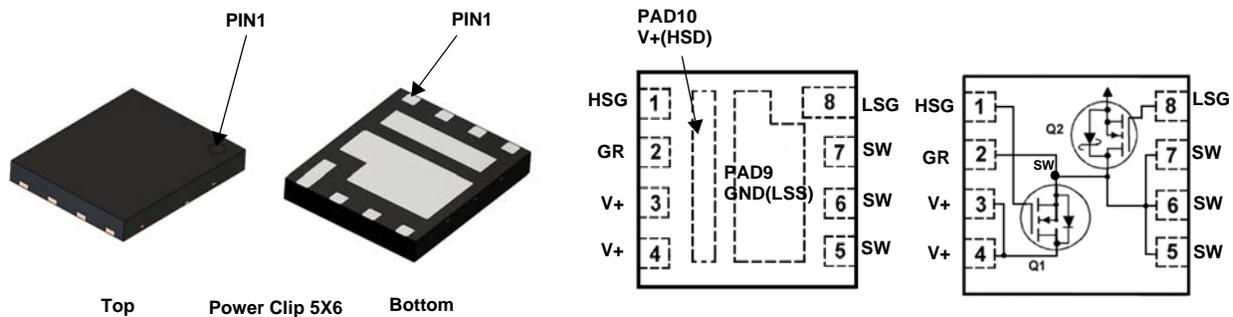


General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	25 ^{Note5}	25	V
V_{GS}	Gate to Source Voltage	±12	±12	V
I_D	Drain Current -Continuous	$T_C = 25\text{ °C}$	60	110
	-Continuous	$T_A = 25\text{ °C}$	20 ^{Note1a}	41 ^{Note1b}
	-Pulsed	$T_A = 25\text{ °C}$ (Note 4)	75	160
E_{AS}	Single Pulse Avalanche Energy (Note 3)	73	253	mJ
P_D	Power Dissipation for Single Operation	$T_C = 25\text{ °C}$	21	42
	Power Dissipation for Single Operation	$T_A = 25\text{ °C}$	2.1 ^{Note1a}	2.3 ^{Note1b}
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.0	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD/16OD	FDPC8014S	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		24 24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 12\text{ V}/-8\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V}/-8\text{ V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	Q1 Q2	0.8 1.1	1.3 1.4	2.5 2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-4 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	Q1		2.8 3.4 3.9	3.8 4.7 5.3	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 41\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 37\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 41\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	Q2		0.9 1.0 1.1	1.2 1.4 1.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 20\text{ A}$ $V_{DS} = 5\text{ V}$, $I_D = 41\text{ A}$	Q1 Q2		182 315		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1: Q2:			1695 6580	2375 9870	pF
C_{oss}	Output Capacitance	$V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		495 1720	710 2580	
C_{rss}	Reverse Transfer Capacitance	Q2: $V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		54 204	100 370	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.4 0.4	1.2 1.2	Ω

Switching Characteristics

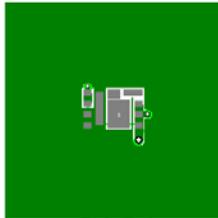
$t_{d(on)}$	Turn-On Delay Time		Q1 Q2		8 16	16 28	ns
t_r	Rise Time	Q1: $V_{DD} = 13\text{ V}$, $I_D = 20\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		2 6	10 11	
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 13\text{ V}$, $I_D = 41\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		24 47	38 75	ns
t_f	Fall Time		Q1 Q2		2 4	10 10	
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V	Q1 Q2		25 93	35 130	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 4.5 V	Q1 Q2		11 43	16 60	
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		3.4 13		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.2 8.5		

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

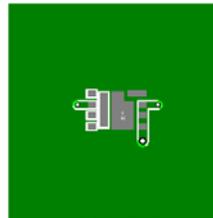
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 41\text{ A}$ (Note 2)	Q2		0.8	1.2	
I_S	Diode continuous forward current	$T_C = 25\text{ }^\circ\text{C}$	Q1		60		A
			Q2		110		
$I_{S,Pulse}$	Diode pulse current		Q1		75		A
			Q2		160		
t_{rr}	Reverse Recovery Time	Q1 $I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		25	40	ns
		Q2	Q2		36	58	
Q_{rr}	Reverse Recovery Charge	$I_F = 41\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		10	20	nC
			Q2		47	75	

Notes:

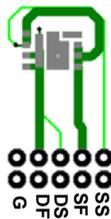
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



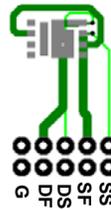
a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 130 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1 : E_{AS} of 73 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 3\text{ mH}, I_{AS} = 7\text{ A}, V_{DD} = 30\text{ V}, V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}, I_{AS} = 24\text{ A}$.

Q2 : E_{AS} of 253 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 3\text{ mH}, I_{AS} = 13\text{ A}, V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}, I_{AS} = 43\text{ A}$.

4. Pulsed I_d limited by junction temperature, $t_d \leq 10\text{ }\mu\text{s}$. Please refer to SOA curve for more details.

5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

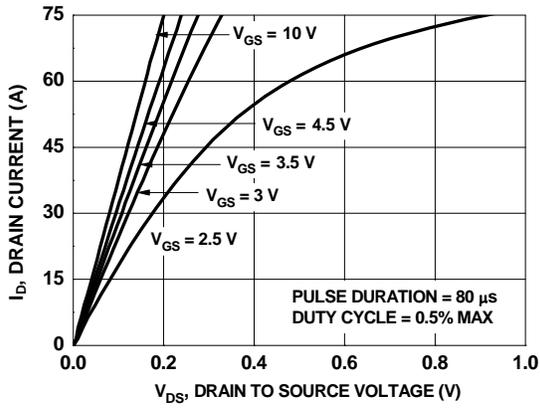


Figure 1. On Region Characteristics

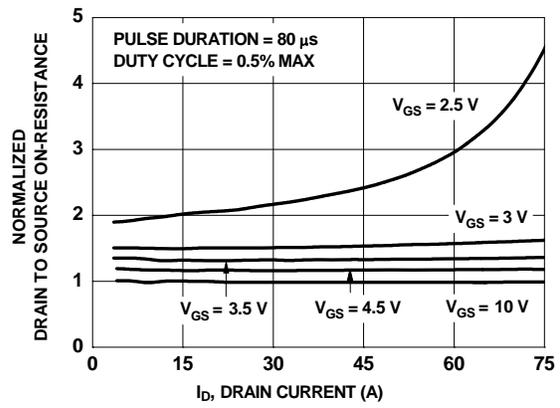


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

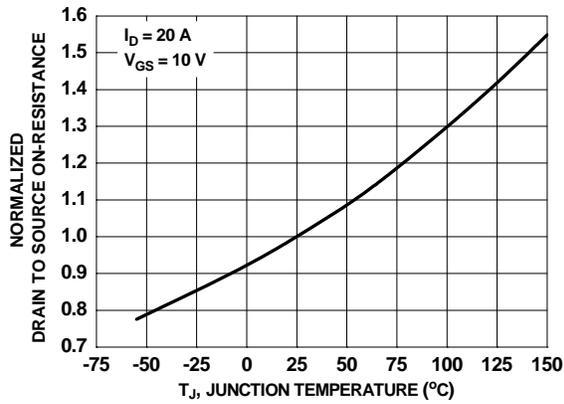


Figure 3. Normalized On Resistance vs. Junction Temperature

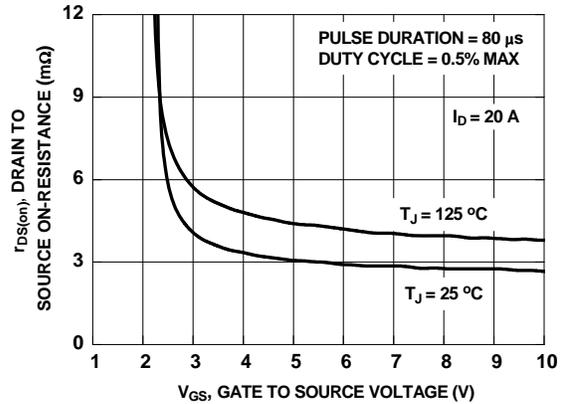


Figure 4. On-Resistance vs. Gate to Source Voltage

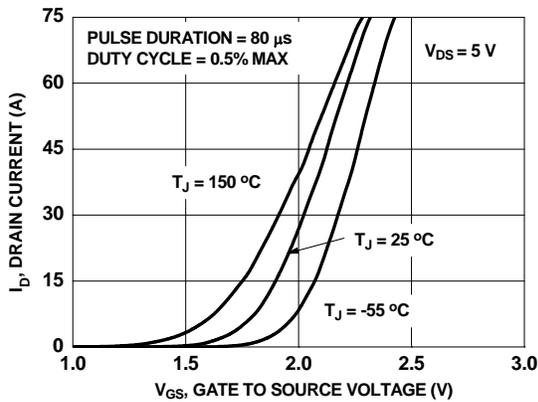


Figure 5. Transfer Characteristics

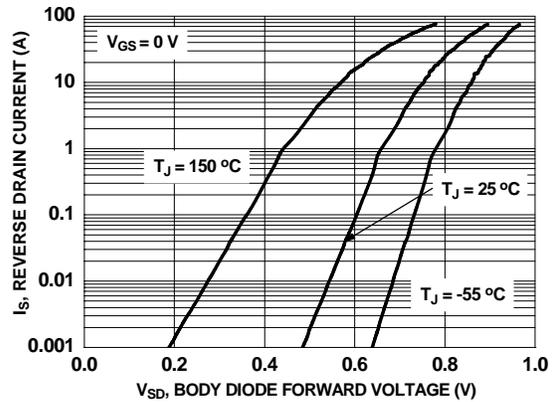


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

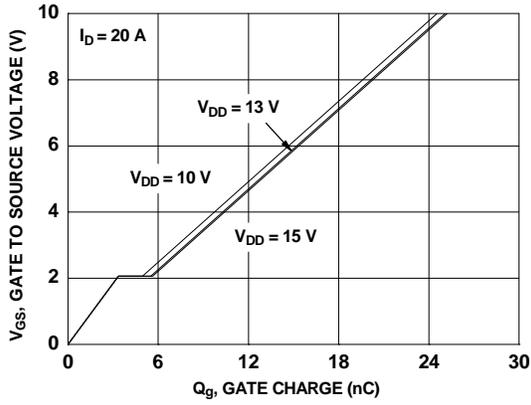


Figure 7. Gate Charge Characteristics

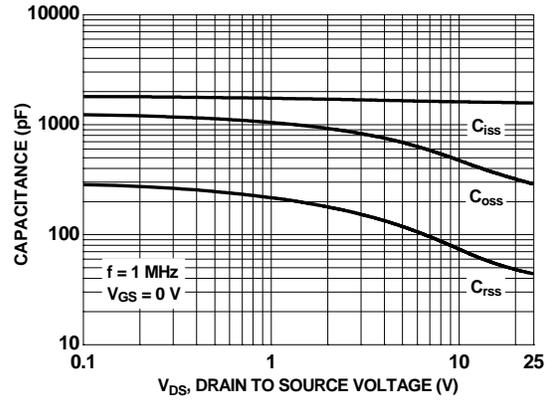


Figure 8. Capacitance vs. Drain to Source Voltage

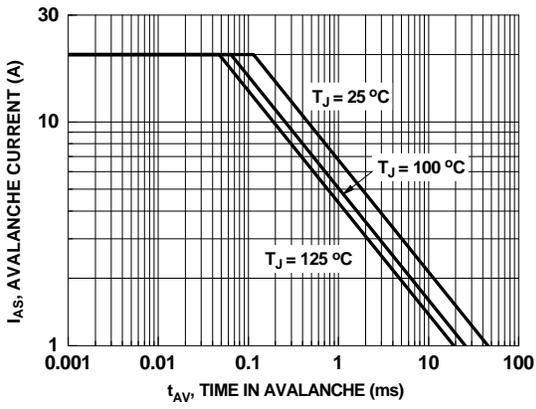


Figure 9. Unclamped Inductive Switching Capability

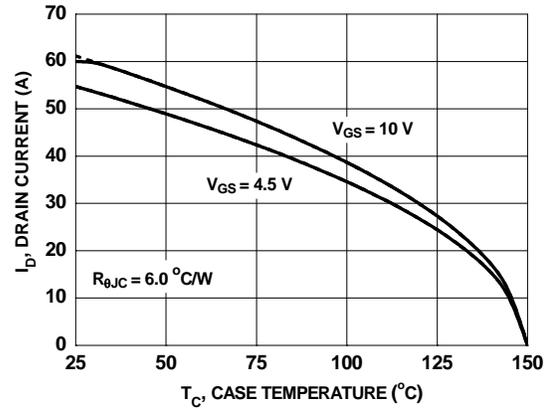


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

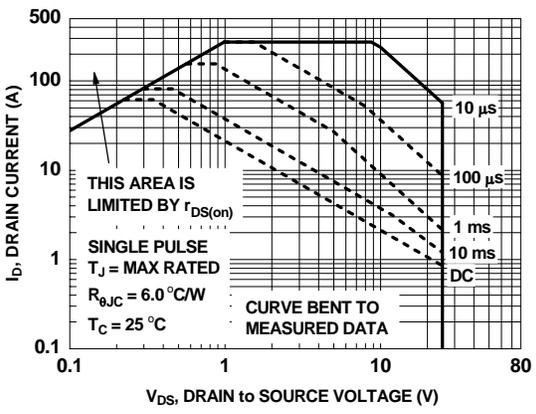


Figure 11. Forward Bias Safe Operating Area

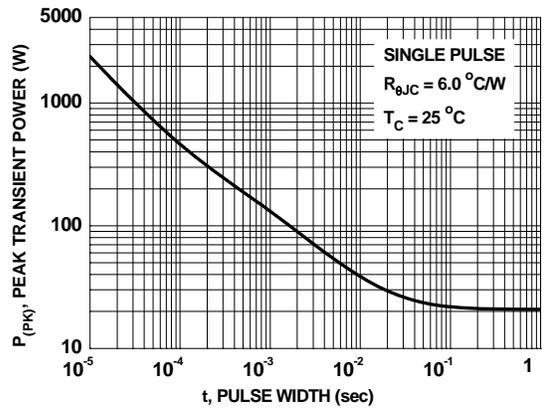


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

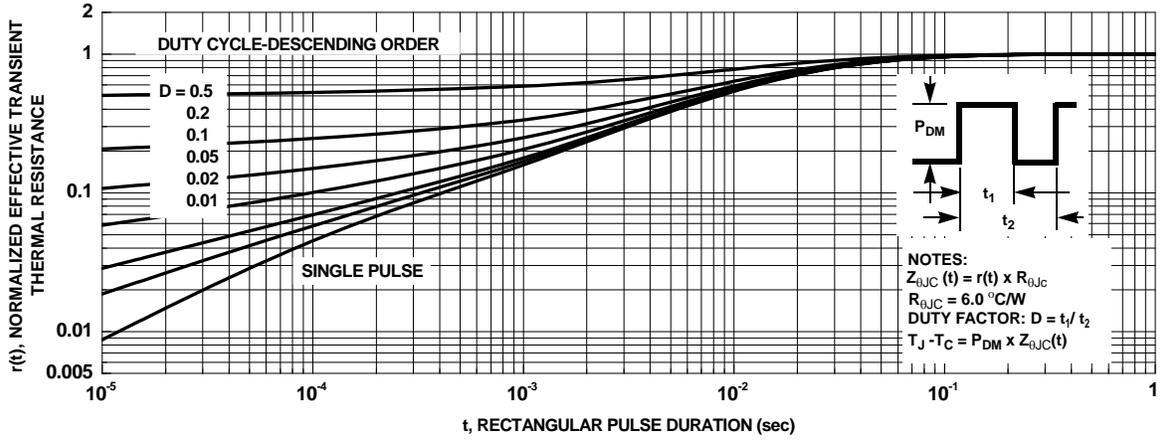


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

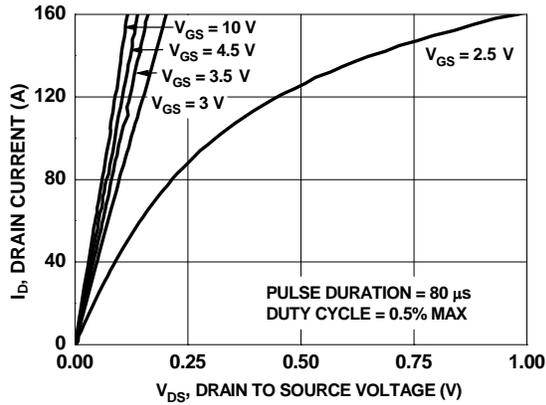


Figure 14. On-Region Characteristics

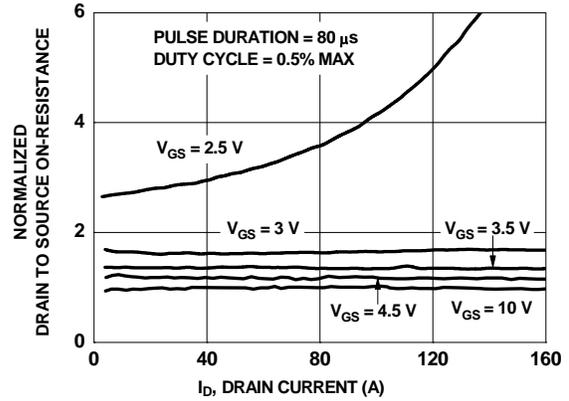


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

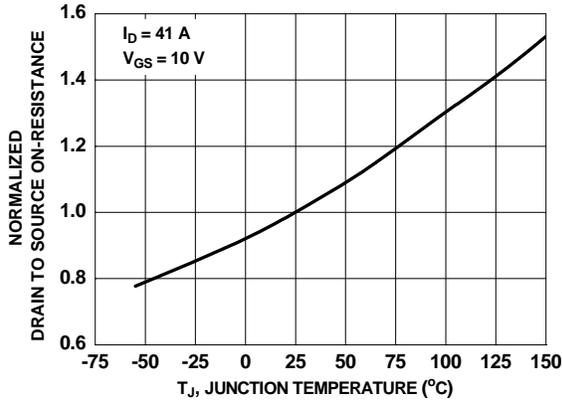


Figure 16. Normalized On-Resistance vs. Junction Temperature

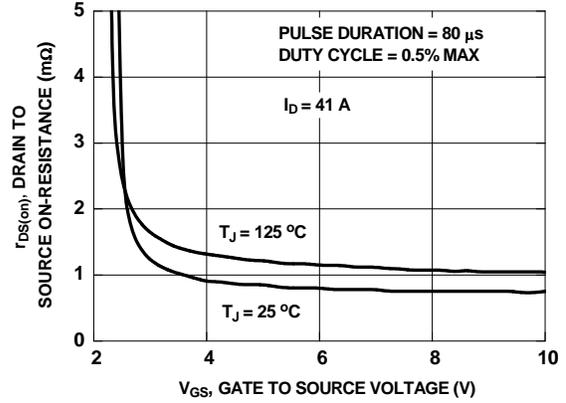


Figure 17. On-Resistance vs. Gate to Source Voltage

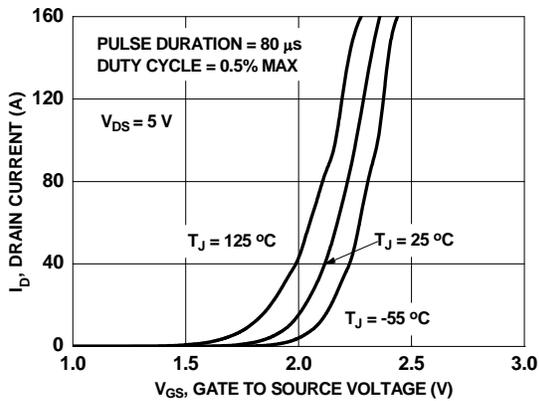


Figure 18. Transfer Characteristics

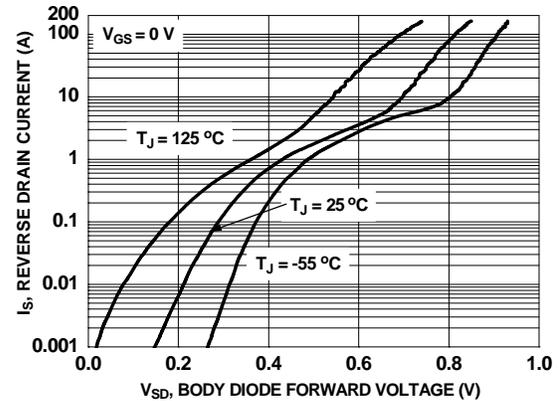


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

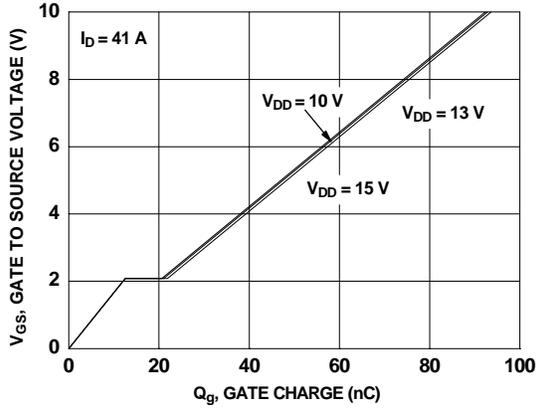


Figure 20. Gate Charge Characteristics

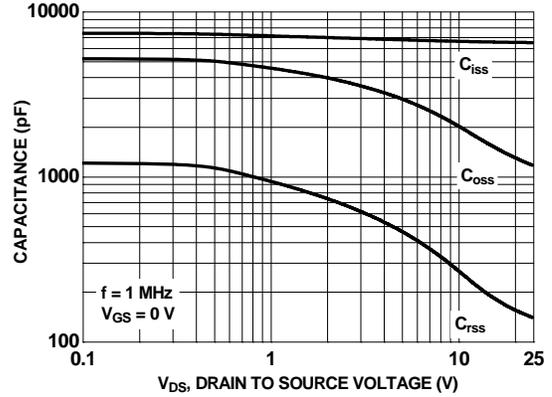


Figure 21. Capacitance vs. Drain to Source Voltage

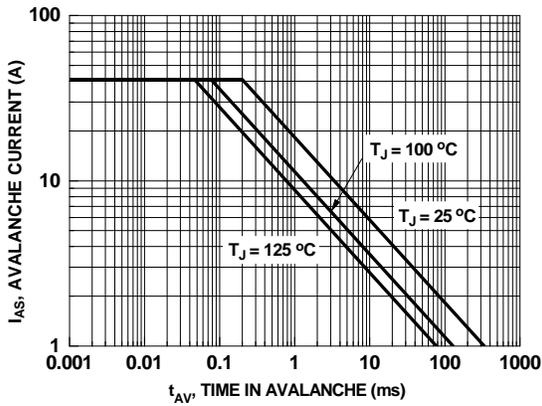


Figure 22. Unclamped Inductive Switching Capability

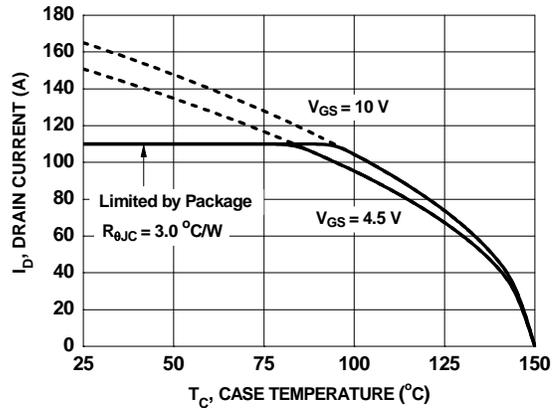


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

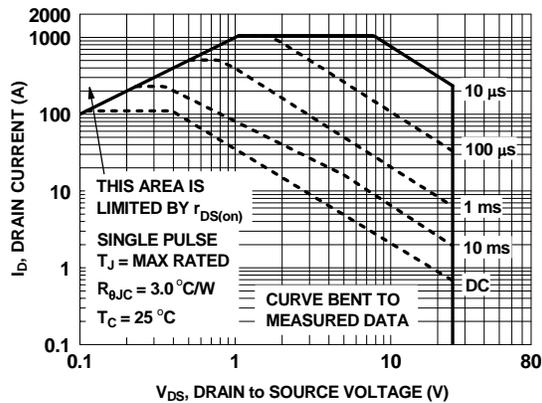


Figure 24. Forward Bias Safe Operating Area

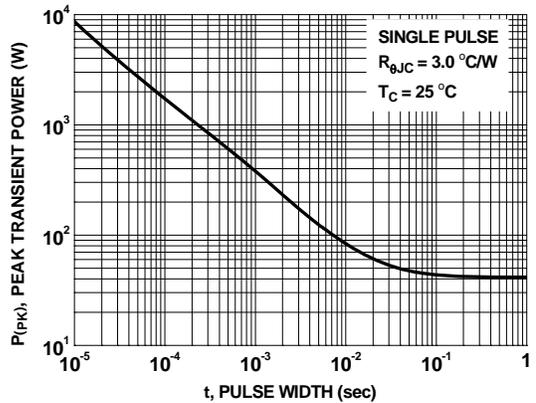


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

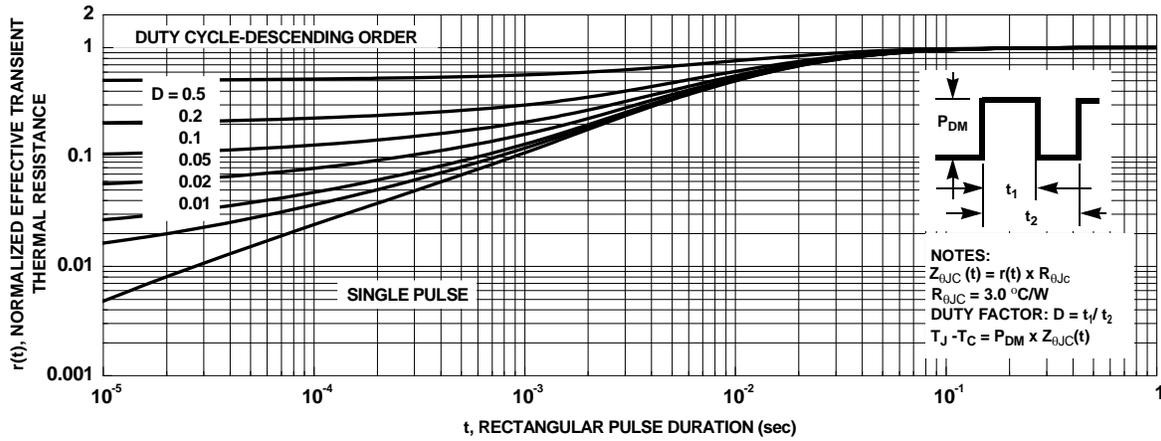


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8014S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

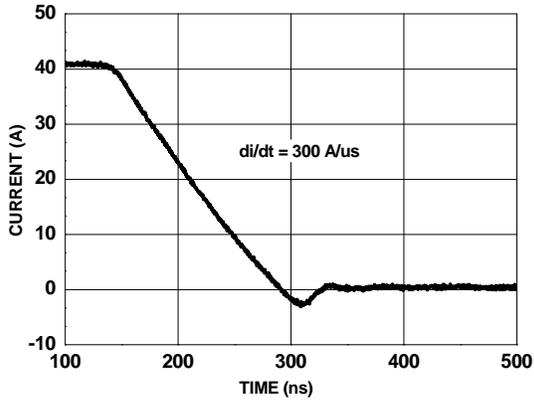


Figure 27. FDPC8014S SyncFET™ Body Diode Reverse Recovery Characteristic

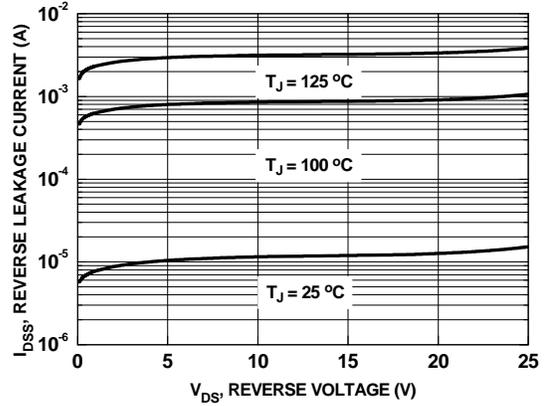
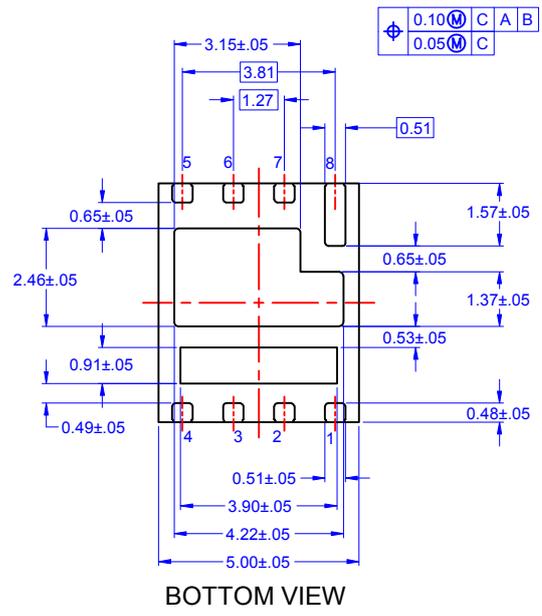
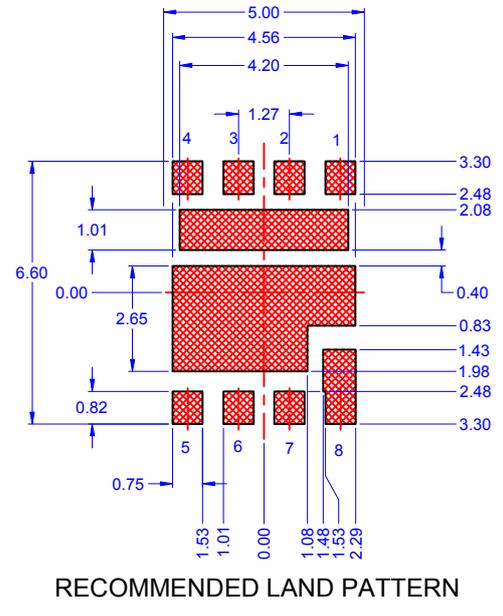
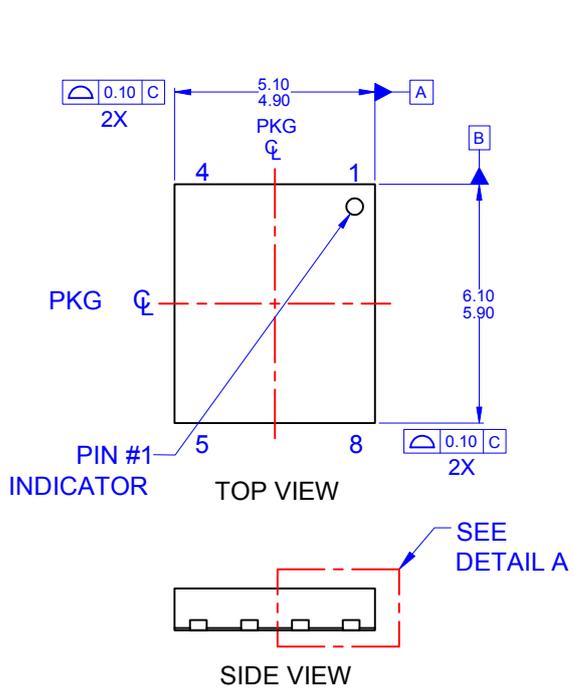
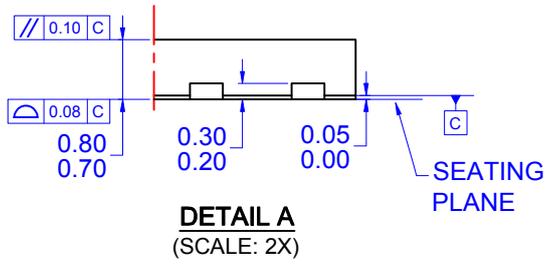


Figure 28. SyncFET™ Body Diode Reverse Leakage vs. Drain-source Voltage



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - E) DRAWING FILE NAME: PQFN08KREV2





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| DEUXPEED® | MegaBuck™ | SignalWise™ | TRUECURRENT®* |
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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