# UCS4003

## USB Type-C Power Delivery Port Protector

### Description

The UCS4003 is a USB Type-C Power Delivery port protector for Configuration Channel (CC), and D+, D- (data lines). The CC, D+, D- and SG_SENS (short-to-GND) are ESD-protected to meet IEC 61000-4-2 and ISO 10605. The UCS4003 provides short-to-battery protection on CC, D+ and D-. It also provides battery short-to-GND protection for the charging port. Additionally, it is configurable to assert FAULT# in case of any fault or in case of any fault except D+/D- or CC overvoltage.

### Features

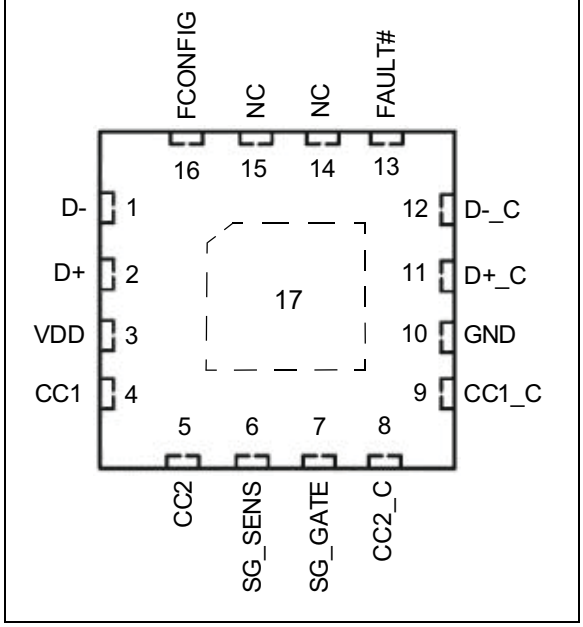
- AEC-Q100 Automotive Qualified, See Product Identification System
- Short-to-Battery Protection on D+, D-, and CC (24V DC)
- Battery Short-to-GND Protection for Charging Port
- FAULT# Assertion Configurability
- IEC 61000-4-2 and ISO 10605 ESD Protection on D+, D-, CC and SG_SENS
- Overtemperature Protection (Thermal Shutdown)
- Temperature Range: -40°C to +125°C
- Supports Power Delivery Protocol

### Applications

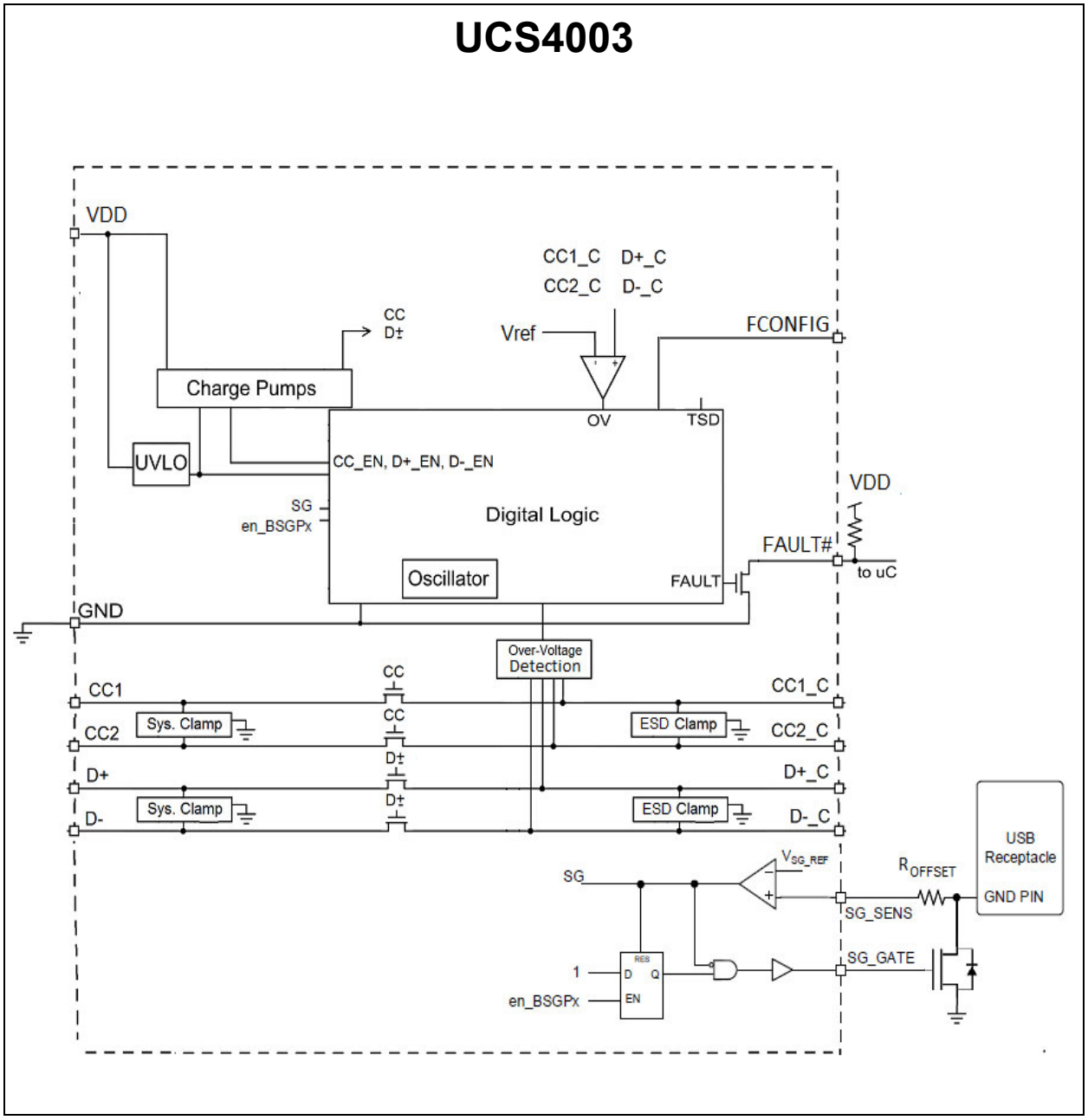
- USB Type-C Power Delivery
- Consumer, Industrial and Automotive Protection

### Package Type

**UCS4003**
3 x 3 mm VQFN
(Top View)



## Block Diagram



## 1.0 DEVICE OVERVIEW

The UCS4003 is a USB Type-C Power Delivery port protector for D+, D- and CC. The D+, D-, CC and SG_-SENS (short-to-GND) are ESD-protected to meet the IEC 61000-4-2 and ISO 10605 standards. The UCS4003 provides short-to-battery protection on D+, D- and CC. The UCS4003 will also provide battery short-to-GND protection for charging ports. Additionally, the UCS4003 is configurable to assert FAULT# in case of any fault or any fault except D+/D- or CC overvoltage as defined in Section 1.4, Fault Configuration (FCONFIG).

The UCS4003 implements VDD undervoltage lockout protection. It also has a thermal shutdown circuit, which will shut the port protection device off when the junction temperature exceeds the limit.

The UCS4003 is a pass-through device that will be transparent to the application and will not affect the signal integrity of the USB data lines or the intended USB application functions, including power delivery.

### 1.1 D+, D- (USB DATA LINES)

The D+_C and D-_C pins are protected against short to battery and VBUS of the USB application. As shown in Figure 1-1, when the voltage on D+_C/D-_C exceeds $V_{OVP\_D\pm}$, the pass FETs for D+, D-, CC1 and CC2 will turn OFF in $t_{OVP\_RT\_D\pm\_C}$ and FAULT# pin asserted in $t_{FAULT\_ASSERT}$. Once the voltage on D+_C/D-_C goes below $V_{OVP\_D\pm}$ minus $V_{OVP\_D\pm\_HYST}$ and $t_{OVP\_REC\_D\pm\_C}$ has elapsed, the UCS4003 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

As shown in Figure 1-2, if the overvoltage condition remains on D+_C/D-_C after $t_{OVP\_REC\_D\pm\_C}$ elapses, all the pass FETs will remain OFF and FAULT# asserted. Once the voltage on D+_C/D-_C goes below $V_{OVP\_D\pm}$ minus $V_{OVP\_D\pm\_HYST}$ and $t_{REC\_D\pm\_C}$ has elapsed, the UCS4003 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Additionally, the UCS4003 implements voltage clamps after the pass FETs on the D+/D- side of the protection circuit. The purpose of these clamps is to limit the voltage on the D+/D- pins for the duration of $t_{OVP\_RT\_D\pm\_C}$ until the pass FETs are turned OFF.

### 1.2 CC (CONFIGURATION CHANNEL)

The CC1_C and CC2_C pins are protected against short to battery and VBUS for USB applications implementing higher than 5V on VBUS.

Figure 1-1 shows the overvoltage timing diagram for D+ and D- when the overvoltage condition is shorter than the recovery time. This also applies to CC1_C and CC2_C by replacing D± with its corresponding CCx timing and voltage parameters. When the voltage on CC1_C/CC2_C exceeds $V_{OVP\_CCx}$, the pass FETs for D+, D-, CC1 and CC2 will turn OFF in $t_{OVP\_RT\_CCx\_C}$ and FAULT# pin asserted in $t_{FAULT\_ASSERT}$. Once the voltage on CC1_C/CC2_C goes below $V_{OVP\_CCx}$ minus $V_{OVP\_CCx\_HYST}$ and $t_{OVP\_REC\_CCx\_C}$ has elapsed, the UCS4003 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Figure 1-2 shows the overvoltage timing diagram for D+ and D- when the overvoltage condition is longer than the recovery time. This also applies to CC1_C and CC2_C by replacing D± with its corresponding CCx timing and voltage parameters. If the overvoltage condition remains on CC1_C/CC2_C after $t_{OVP\_REC\_CCx\_C}$ elapses, all the pass FETs will remain OFF and FAULT# asserted. Once the voltage on CC1_C/CC2_C goes below $V_{OVP\_CCx}$ minus $V_{OVP\_CCx\_HYST}$ and $t_{REC\_CCx\_C}$ has elapsed, the UCS4003 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Additionally, the UCS4003 implements voltage clamps after the pass FETs on the CC1/CC2 side of the protection circuit. The purpose of these clamps is to limit the voltage on the CC1/CC2 pins for the duration of $t_{OVP\_RT\_CCx\_C}$ until the pass FETs are turned OFF.

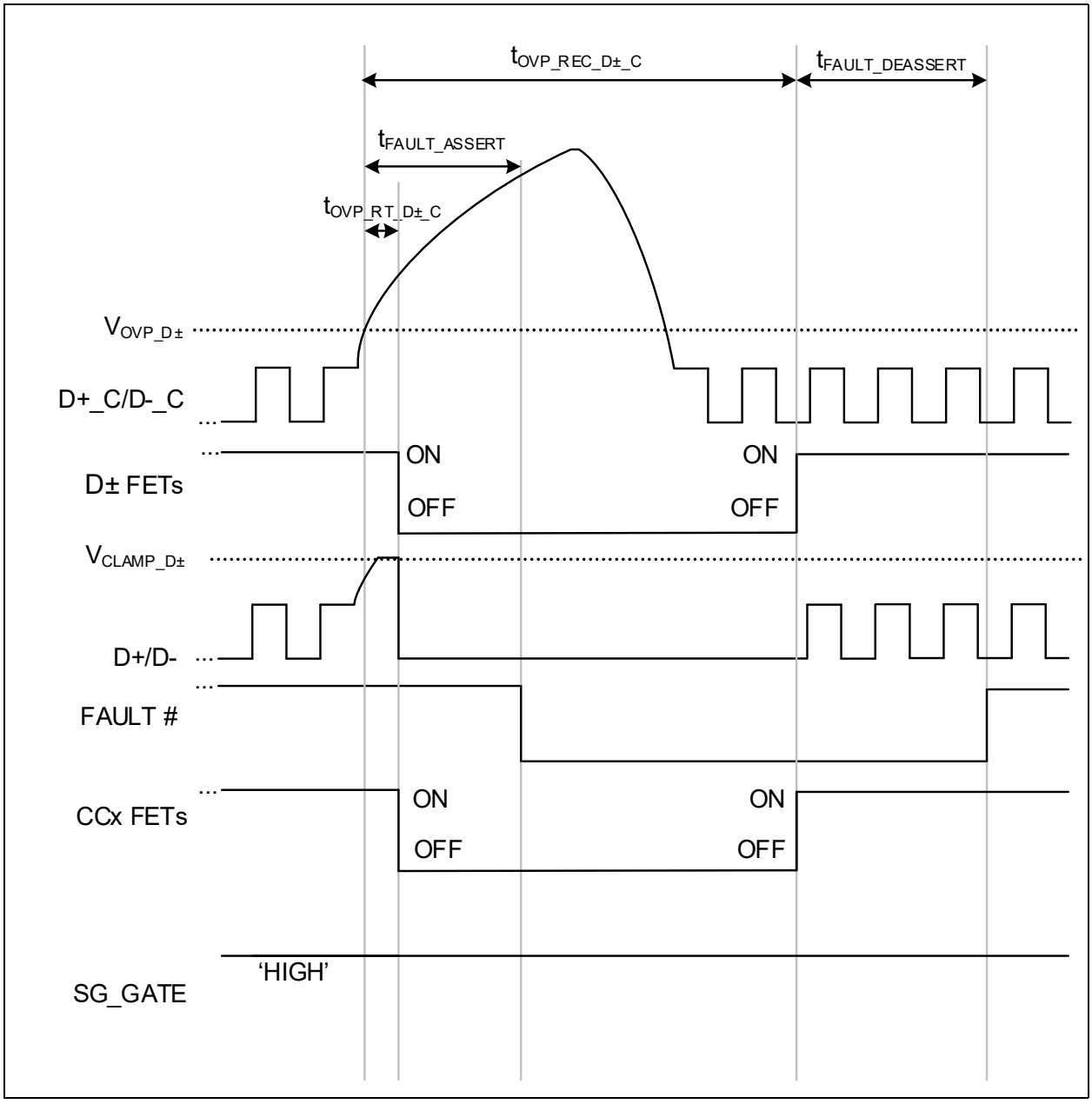



***FIGURE 1-1:*** *D+_C/D-_C Overvoltage Shorter than Recovery Time.*

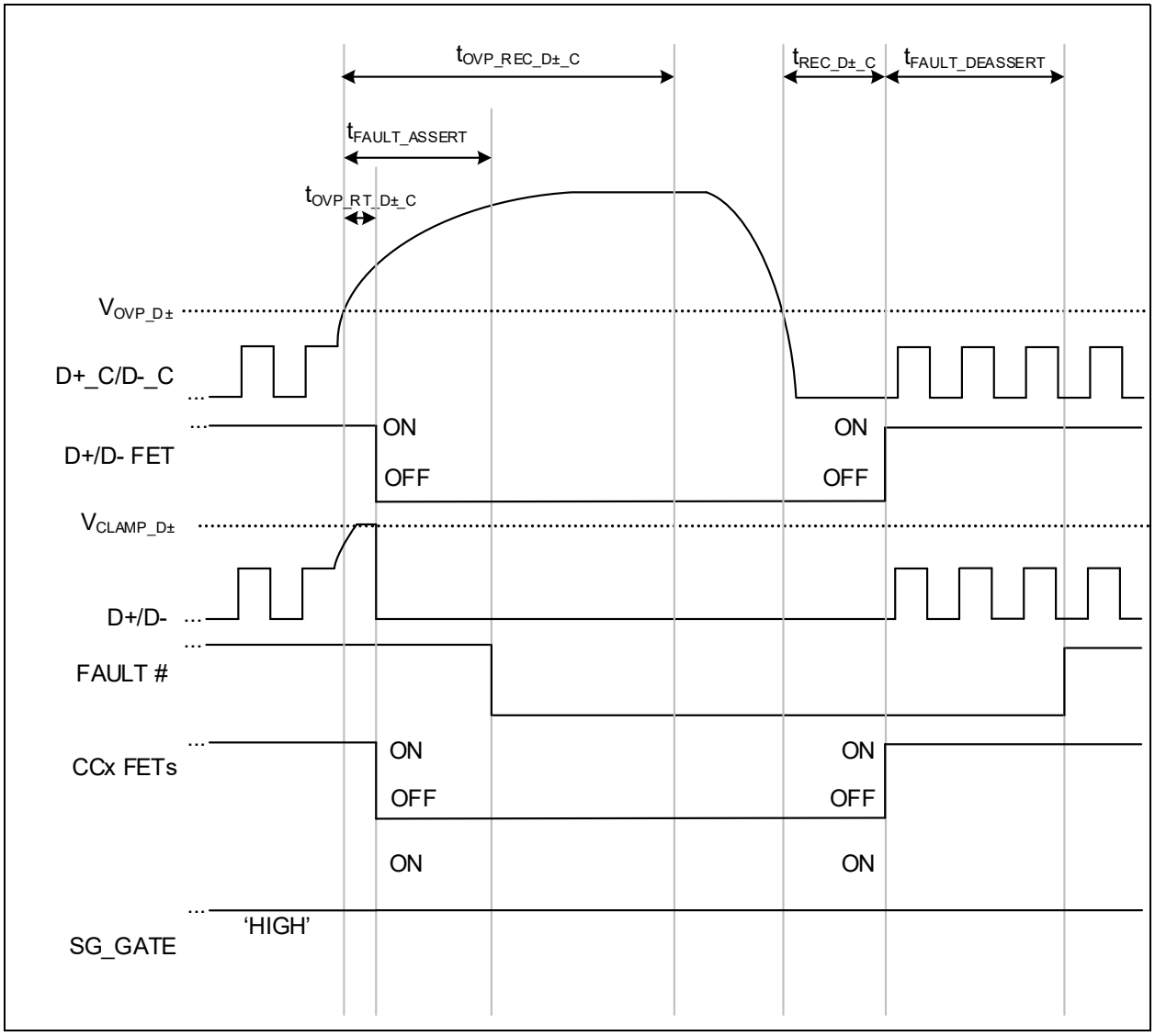



***FIGURE 1-2:*** *D+_C/D-_C Overvoltage Longer than Recovery Time.*

## 1.3 SG_SENS, SG_GATE

The SG_SENS and SG_GATE are dedicated protection pins for short-to-GND conditions on a charging port. If this protection feature is not implemented, SG_SENS must be connected to GND and SG_GATE must be left open.

An external FET and a resistor ($R_{OFFSET}$) may optionally be implemented to protect against battery shorts to GND. The external FET must have an $R_{dsON}$ ranging from 5 mΩ to 30 mΩ ($R_{FET}$) and must be able to sustain $I_{DS}$ for $t_{STG\_RT}$.

The amount of current the external FET must be able to sustain can be computed using Equation 1-1.

**EQUATION 1-1:**

$$I_{DS} = \frac{V_{DS}}{R_{FET}}$$

The drain to source voltage ($V_{DS}$) on the external FET can be computed using Equation 1-2:

**EQUATION 1-2:**

$$V_{DS} = \frac{V_{BAT} \times R_{FET}}{R_{SHORT} + R_{CABLE} + R_{FET}}$$

The minimum voltage shorted to GND must be greater than 6V ($V_{BAT}$) in order to guarantee the short-to-GND detection. In addition to FET RdsON and minimum voltage shorted to GND, cable resistance ($R_{CABLE}$)

must be taken into account, as well as the resistance of the short ($R_{SHORT}$). The following formula can then be used to compute the voltage on the SG_SENS pin:

**EQUATION 1-3:**

$$V_{SG\_SENS} = R_{OFFSET} \times I_{OFFSET} + V_{DS}$$

Please refer to Figure 1-3 for short-to-GND simplified application diagram.

As shown in Figure 1-4, when the SG_SENS pin voltage goes above $V_{SG\_IH}$, the SG signal is asserted. The SG_GATE pin will drive low to turn OFF the external FET and the pass FETs for D+, D-, CC1 and CC2 will turn OFF in $t_{STG\_RT}$ and FAULT# pin asserted in $t_{FAULT\_ASSERT}$. Once the voltage on SG_SENS pin goes below $V_{SG\_IL}$ and $t_{SG\_REC}$ has elapsed, the UCS4003 will automatically turn all internal pass FETs back ON and drive the SG_GATE pin high to turn the external FET back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

As shown in Figure 1-5, if the short-to-GND condition is still present after $t_{SG\_REC}$ elapses, the SG_GATE pin will remain driven low, all pass FETs will remain OFF and the FAULT# asserted. Once the voltage on SG_SENS goes below $V_{SG\_IL}$ and $t_{SG\_REC\_LONG}$ has elapsed, the UCS4003 will automatically turn all internal pass FETs back ON and drive the SG_GATE pin high to turn the external FET back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

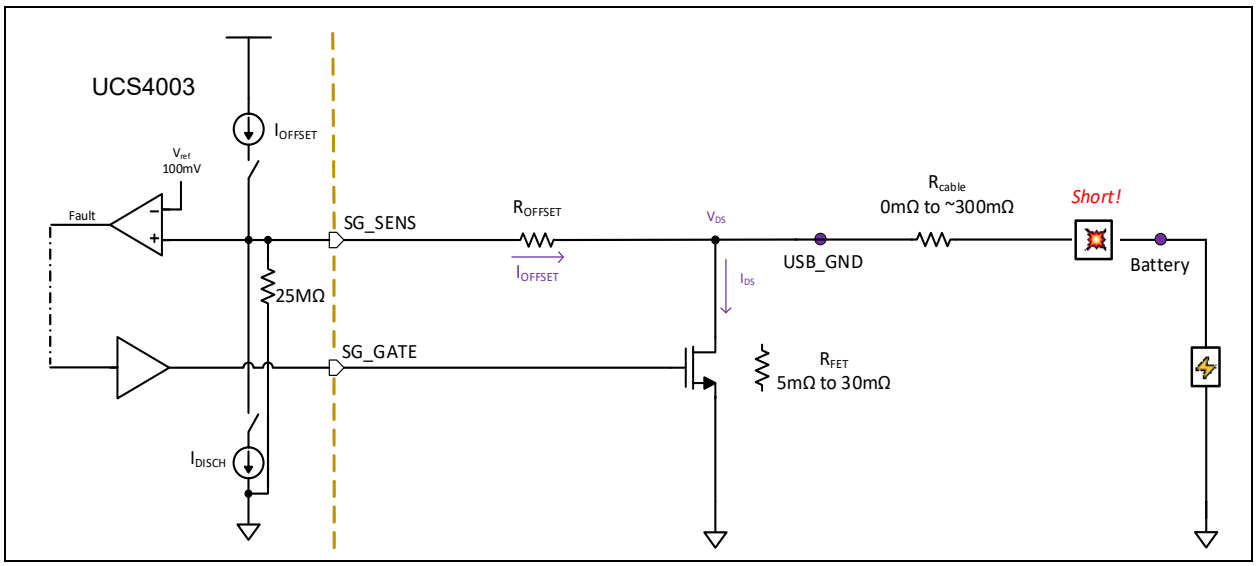



***FIGURE 1-3:*** *Short-to-GND System Protection.*

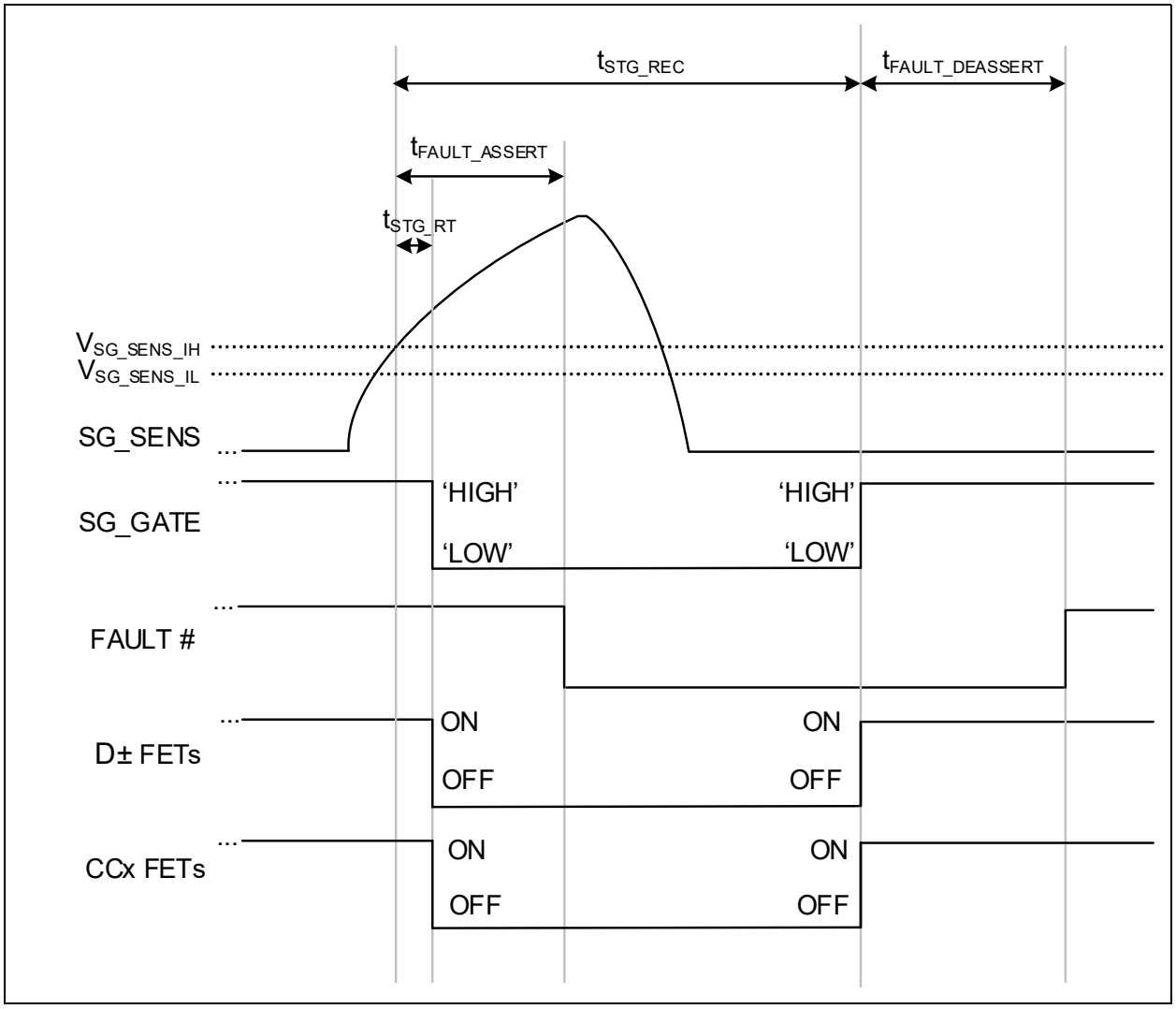



***FIGURE 1-4:*** *Short-to-GND Shorter than Recovery Time.*

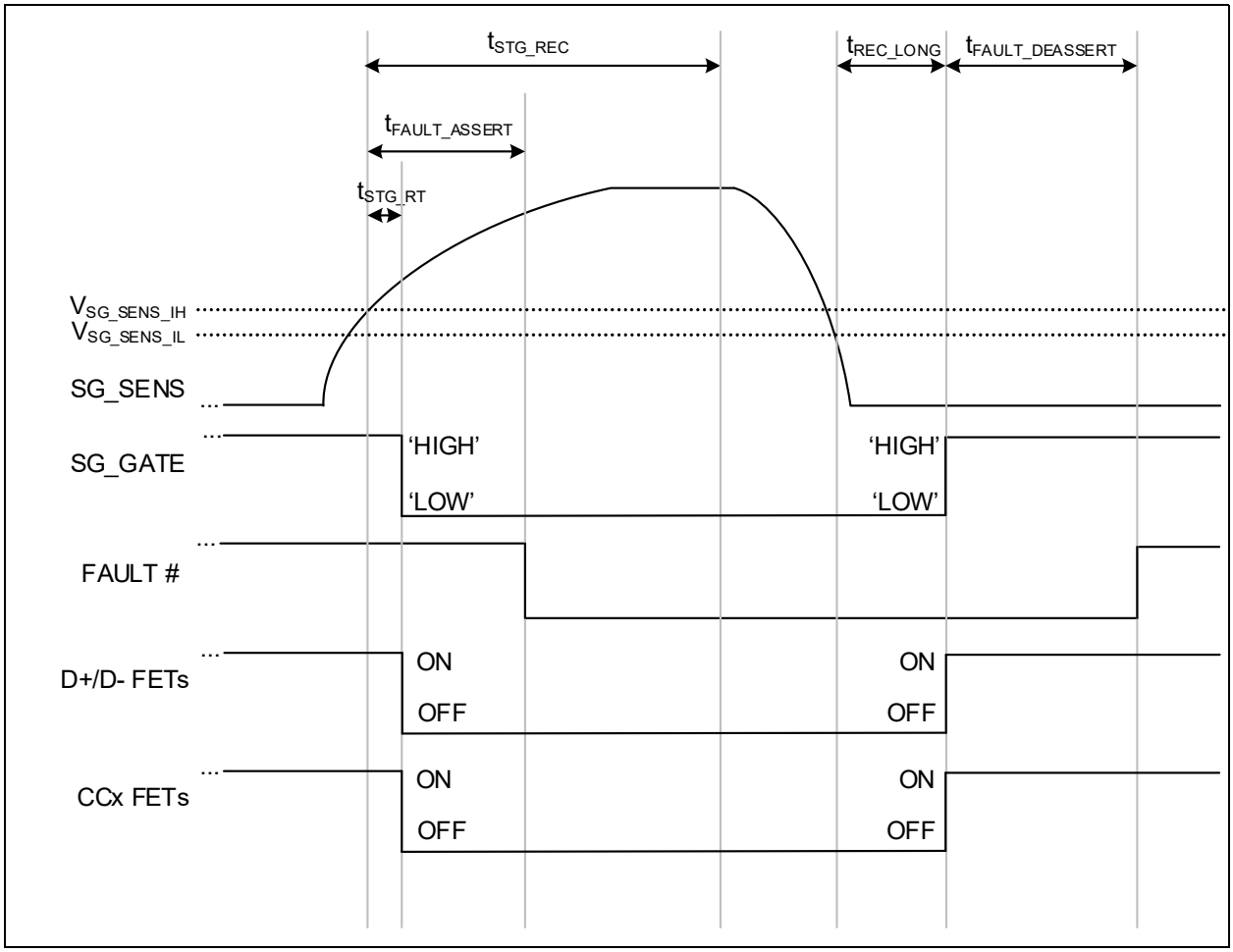



***FIGURE 1-5:*** *Short-to-GND Longer than Recovery Time.*

## 1.4 Fault Configuration (FCONFIG)

The UCS4003 allows the user to configure the FAULT# behavior via the FCONFIG pin as follows:

- **FCONFIG = GND or 'OPEN'**
  Assert FAULT# in case of any fault
- **FCONFIG = 'HIGH'**
  Assert FAULT# in case of any fault except D+/D- or CC overvoltage

Although the FAULT# may not be asserted based upon the specific FCONFIG setting, the pass FETs for D+, D-, CC1 and CC2 will still turn OFF and back ON based upon the Fault condition.

## 1.5 Thermal Shutdown

The thermal shutdown circuit sends the TSD signal to the digital logic when the die temperature exceeds $T_{TSD}$. It has a hysteresis of $T_{TSD\_HYST}$.

## 1.6 Operating Mode

When VDD is below the $V_{DD\_UVLO}$ threshold, the UCS4003 functionality is fully disabled except for the short-to-GND gate driver.

When VDD is higher than the $V_{DD\_UVLO}$ threshold, the D+, D- and CC MOSFETs, the short-to-GND gate driver, and the Fault detection blocks are fully enabled. The UCS4003 will remain in the same power state when a Fault condition has occurred.

### 1.6.1 FAULT HANDLING

A Fault state means that at least one of the following conditions has occurred:

- Overvoltage (see Figure 1-6 for D+, D- example)
- Undervoltage
- Short-to-GND
- Thermal Shutdown

The digital logic continuously monitors the comparators outputs. Any Fault will cause the rest of the protection circuit blocks in the UCS4003 to be enabled. Example: If there is an overvoltage on D+, all the UCS4003 pass FETs will be disabled. The only protection circuit that will remain active, if implemented, is the external FET for battery short-to-GND (keeping GND connected).

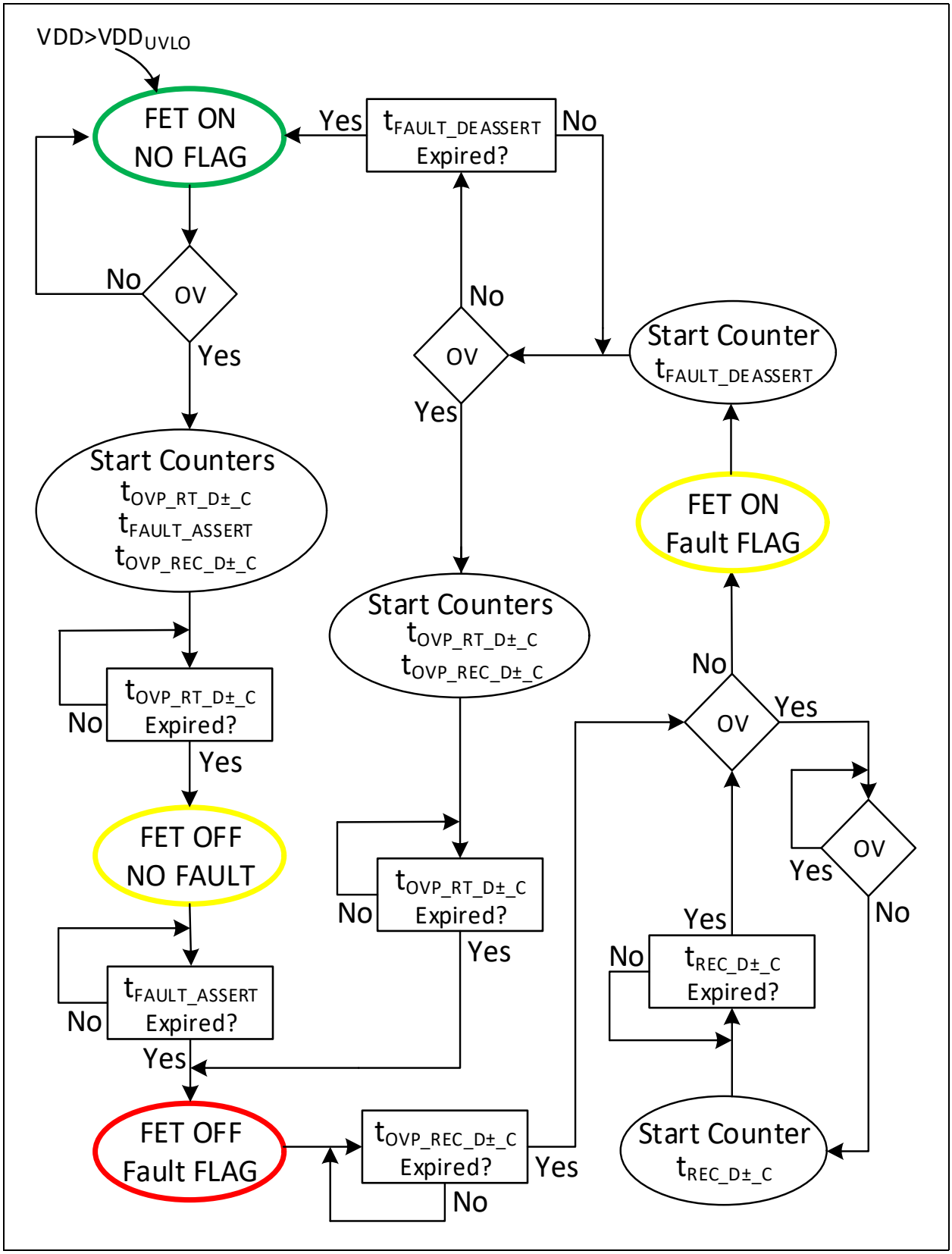



***FIGURE 1-6:*** *D+, D- Fault Flow Chart.*

## 1.7 FUNCTIONAL PIN DESCRIPTIONS

The table below describes the function of each pin.

**TABLE 1-1: PIN DESCRIPTION TABLE**

| Pin | Symbol | Pin Type | Description |
|---|---|---|---|
| 1 | D- | I/O | Module side of the High-Speed USB data line (-). This pin connects to the D- of the USB transceiver. |
| 2 | D+ | I/O | Module side of the High-Speed USB data line (+). This pin connects to the D+ of the USB transceiver. |
| 3 | VDD | Power | Power supply |
| 4 | CC1 | I/O | Module side of the CC1 overvoltage protection FET. This pin is connected to either of the CC pins of the CC/PD Controller. |
| 5 | CC2 | I/O | Module side of the CC2 overvoltage protection FET. This pin is connected to either of the CC pins of the CC/PD Controller. |
| 6 | SG_SENS | I | Short-to-GND protection sense input. This pin must be grounded when the protection feature is not implemented. |
| 7 | SG_GATE | O | Short-to-GND protection gate drive. This pin must be left open when the protection feature is not implemented. |
| 8 | CC2_C | I/O | Connector side of the CC2 overvoltage protection FET. This pin is connected to either of the CC pins of the USB connector. |
| 9 | CC1_C | I/O | Connector side of the CC1 overvoltage protection FET. This pin is connected to either of the CC pins of the USB connector. |
| 10 | GND | Ground | Ground for the power supply |
| 11 | D+_C | I/O | Connector side of the High-Speed USB data line (+). This pin connects to the D+ of the USB connector. |
| 12 | D-_C | I/O | Connector side of the High-Speed USB data line (-). This pin connects to the D- of the USB connector. |
| 13 | FAULT# | Open Drain Output | A logic low state indicates a Fault condition. This pin requires an external pull-up resistor. |
| 14, 15 | NC | Not Connected | Connect to ground |
| 16 | FCONFIG | I | FAULT# assertion configuration pin<br>‘low’ or ‘open’ = FAULT# asserted in case of any Fault<br>‘high’ = FAULT# asserted in case of any Fault except D+/D- or CC overvoltage |
| 17 | EP | Exposed Pad | Exposed pad is NOT electrically connected. It is recommended to connect the exposed pad to ground. |

## 1.8 Typical Applications

Figure 1-7 illustrates an example of a typical application of the UCS4003.

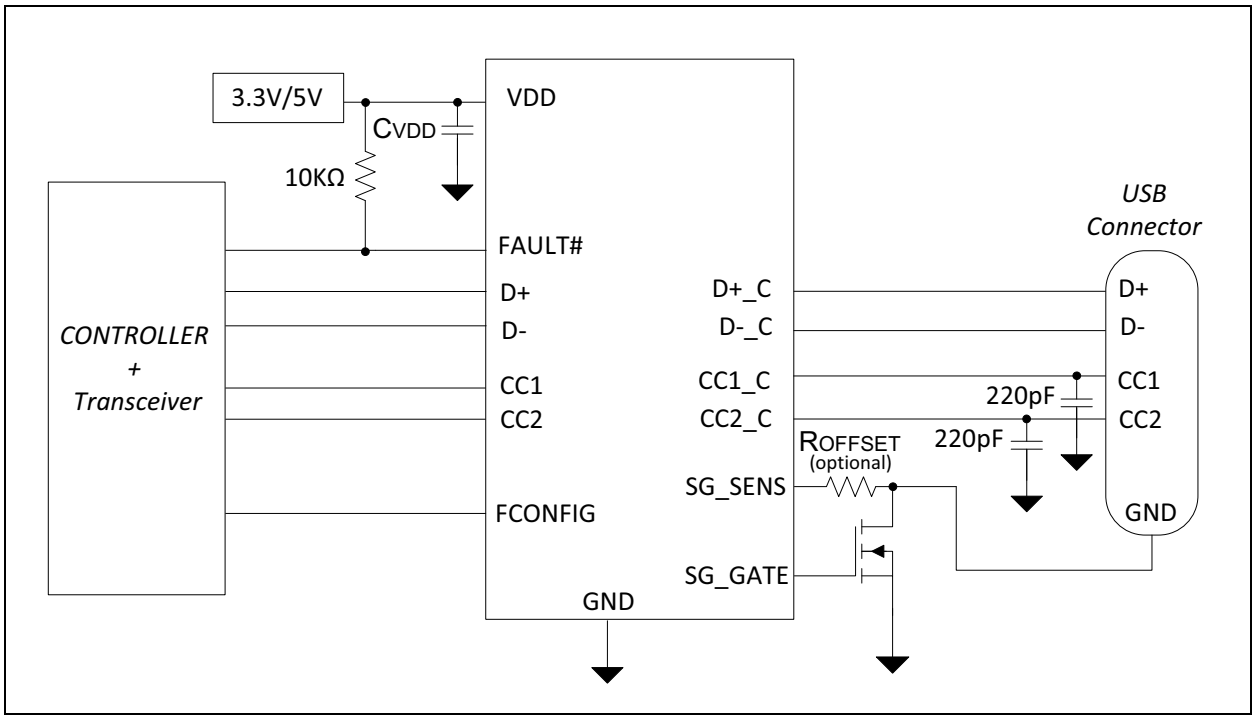



***FIGURE 1-7:*** *Typical Application.*

## 2.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Voltage on D+_C, D-_C, CC1_C, CC2_C, SG_SENS pins ..... -0.3V to 25V

Voltage on any other pin to ground ..... -0.3V to 6V

Current on the FAULT# pin ..... 10 mA

Operating Junction Temperature ..... -40°C to +125°C

Storage Temperature ..... -55°C to +150°C

Junction-to-Ambient Thermal Resistance ..... 62°C/W

ESD protection on D+_C, D-_C, CC1_C, CC2_C, SG_SENS, GND pins

(IEC 61000-4-2: 150pF, 330Ω) ..... ±8 kV Contact, ±15 kV Air

ESD protection on CC1_C, CC2_C, SG_SENS, GND pins (ISO 10605: 330pF, 2kΩ) ..... ±8 kV Contact, ±15 kV Air (1)

ESD protection on D+_C, D-_C pins (ISO 10605: 330pF, 2kΩ) ..... ±7 kV Contact, ±15 kV Air (1)

ESD protection on D+_C, D-_C, CC1_C, CC2_C, SG_SENS, GND pins

(JEDEC JESD22-A114; Human Body Model) ..... ±6 kV

ESD protection on all other pins (JEDEC JESD22-A114; Human Body Model) ..... ±2 kV

ESD protection on all pins (JEDEC JESD22-C101; Charge Device Model) ..... ±500V

† **NOTICE:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** System level ESD testing setup is shown in Figure 1-7.

### TABLE 2-1: RECOMMENDED OPERATING CONDITIONS

| Parameters | Pin/s | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply voltage | VDD | 2.7 | — | 5.5 | V |
| Supply voltage capacitance | | 2.2 | — | 10 | µF |
| USB data lines on module side voltage range | D+, D- | 0 | — | 3.6 | V |
| USB data lines on connector side voltage range | D+_C, D-_C | 0 | — | 3.6 | V |
| CC lines on module and connector side voltage range | CC1, CC2, CC1_C, CC2_C | 0 | — | 5.5 | V |
| FAULT# Pull-up resistor power rail | FAULT# | 2.7 | — | 5.5 | V |

**TABLE 2-2: ELECTRICAL SPECIFICATIONS**

$T_J$ = -40 °C to 125 °C,
All typical values $T_J$ = 25 °C, VDD = 2.7V to 5.5V, unless otherwise noted.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Power** | | | | | | |
| Supply Voltage Capacitance | $C_{VDD}$ | 2.2 | — | — | µF | Minimum capacitance required VDD |
| Operating Current | $I_{DD}$ | — | 1 | 2.5 | mA | VDD = 5.5V<br>All pins = OPEN<br>Measure current into VDD |
| Undervoltage Lockout Threshold | $V_{DD\_UVLO}$ | 2.1 | 2.3 | 2.5 | V | Ramp-up voltage on VDD until switches turn ON. |
| Undervoltage Lockout Hysteresis | $V_{UVLO\_HYS}$ | 100 | 150 | 200 | mV | Ramp-down voltage on VDD until switches turn OFF. Calculate delta between rise and fall voltages. |
| Turn-ON Time | $t_{ON}$ | — | — | 3.5 | ms | Time from $V_{DD\_UVLO}$ until D+, D- and CC overvoltage protection FETs are ON.<br>Note 1 |
| Turn-OFF Slew Rate | $t_{OFF\_SR}$ | — | — | 0.5 | V/µs | Highest slew rate allowed to guarantee D+, D- and CC FETs turn OFF during power OFF.<br>Note 1 |
| **D+, D-, D+_C, D-_C** | | | | | | |
| On Resistance | $R_{DS\_ON\_D\pm}$ | — | 4 | 6.5 | Ω | 0 to 0.4V signal on D±<br>10 mA test current |
| Equivalent ON Capacitance | $C_{ON\_D\pm}$ | — | 5 | — | pF | Capacitance across D±_C with 0V to 0.4V bias voltage when FET is ON. |
| D±_C Overvoltage Protection | $V_{OVP\_D\pm}$ | 3.6 | 4 | 4.5 | V | Ramp-up voltage on D±_C from 3.3V to 4.5V until FAULT# is asserted. |
| D±_C Overvoltage Protection Hysteresis | $V_{OVP\_D\pm\_HYST}$ | — | 50 | — | mV | Ramp-down voltage on D±_C until FAULT# is deasserted. Calculate delta between rise and fall voltages. |
| ON Bandwidth (-3dB) | $BW_{ON}$ | — | 1000 | — | MHz | Measure $S_{21}$ bandwidth from D+ to D+_C or D- to D-_C with voltage swing = 400 mVpp. $V_{CM}$=0.2V |
| ON Bandwidth (-3dB) differential | $BW_{ON\_DIFF}$ | — | 1050 | — | MHz | Measure $S_{DD21}$ bandwidth from D± to D±_C with voltage<br>swing = 800 mVpp. $V_{CM}$ = 0.2V |
| Crosstalk | $X_{TALK}$ | — | -44 | — | dB | Measure $S_{21}$ bandwidth from D+ to D-_C or D- to D+_C with voltage swing = 400 mVpp. Be<br>sure to terminate open sides to 50 ohms. f = 480 MHz. |
| D± Leakage Current (Powered or Unpowered) | $I_{LEAK\_D\pm}$ | — | — | 3 | µA | VDD = 5V, D±_C = 3.5V, D± pins floating, measure leakage into D±_C pins and vice-versa |
| D± Leakage Current (Overvoltage) | $I_{LEAK\_D\pm\_OV}$ | — | — | ±1 | µA | VDD = GND or 5V, D±_C = 24V, D± pins = GND. Measure leakage out of D± pins |
| D±_C Leakage Current (Overvoltage) Powered or Unpowered | $I_{LEAK\_D\pm\_C\_OV}$ | — | — | 80 | µA | VDD = GND or 5V, D±_C = 24V, D± pins = GND. Measure leakage into D±_C pins |
| Overvoltage Response Time | $t_{OVP\_RT\_D\pm\_C}$ | — | 200 | — | ns | Time from Over Voltage detected until OVP FETs turn OFF. |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is guaranteed by design.

**TABLE 2-2: ELECTRICAL SPECIFICATIONS (CONTINUED)**

$T_J$ = -40 °C to 125 °C,
All typical values $T_J$ = 25 °C, VDD = 2.7V to 5.5V, unless otherwise noted.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Overvoltage Recovery Time | $t_{OVP\_REC\_D\pm\_C}$ | 10 | 20 | 30 | ms | Minimum time duration after Overvoltage condition is removed until FETs turn back ON. |
| Overvoltage Recovery Time - Long | $t_{REC\_D\pm\_C}$ | — | 500 | — | µs | Time from removal of Overvoltage condition until OVP FETs turn ON when OVP condition is longer than $t_{OVP\_REC\_D\pm\_C}$. |
| D± Overvoltage Clamp | $V_{CLAMP\_D\pm}$ | — | 8 | — | V | Hot-plug 24V to D±_C with a 30Ω load on D±<br>VDD > $V_{DD\_UVLO}$ |
| **CC1, CC2, CC1_C, CC2_C** | | | | | | |
| On Resistance | $R_{DS\_ON\_CC}$ | — | 4 | 6.5 | Ω | CCx = 3.6V<br>10 mA test current |
| CCx Leakage Current (Powered) | $I_{LEAK\_CC}$ | — | — | 15 | µA | VDD = 5V, CCx_C = 5.65V, CCx pins floating, measure leakage into CCx_C pins and vice-versa |
| CCx Leakage Current (Overvoltage) | $I_{LEAK\_CC\_OV}$ | — | — | ±1 | µA | VDD = GND or 5V, CCx_C = 24V, CCx pins = GND. Measure leakage out of CCx pins |
| CCx_C Leakage Current (Overvoltage) | $I_{LEAK\_CC\_C\_OV}$ | — | — | 30 | µA | VDD = GND or 5V, CCx_C = 24V, CCx pins = GND. Measure leakage into CCx_C pins |
| CCx_C Overvoltage Protection | $V_{OVP\_CCx\_C}$ | 5.75 | 6 | 6.2 | V | Ramp up voltage on CCx_C from 5.5 to 6.2V until FAULT# is asserted. |
| CCx_C Overvoltage Protection Hysteresis | $V_{OVP\_CCx\_HYST}$ | — | 60 | — | mV | Ramp down voltage on CCx_C until FAULT# is deasserted. Calculate delta between rise and fall voltages. |
| ON Bandwidth (-3dB) | $BW_{ON\_CCx}$ | — | 530 | — | MHz | Measure -3dB bandwidth from CCx_C to CCx. Single-ended measurement, 50Ω system.<br>$V_{cm}$ = 0.1V to 1.2V |
| Overvoltage Response Time | $t_{OVP\_RT\_CCx\_C}$ | — | 100 | — | ns | Time from Overvoltage detected until OVP FETs turn OFF. |
| Overvoltage Recovery Time | $t_{OVP\_REC\_CCx\_C}$ | 10 | 20 | 30 | ms | Minimum time duration after Overvoltage condition is removed until FETs turn back ON. |
| Overvoltage Recovery Time - Long | $t_{REC\_CCx\_C}$ | — | 500 | — | µs | Time from removal of Overvoltage condition until OVP FETs turn ON when OVP condition is longer than $t_{OVP\_REC\_CCx\_C}$. |
| CCx Overvoltage Clamp | $V_{CLAMP\_CCx}$ | — | 8 | — | V | Hot-plug 24V to CCx_C with a 30Ω load on CCx.<br>VDD > $V_{DD\_UVLO}$ |
| **FAULT** | | | | | | |
| FAULT# Low level Output Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{SINK\_IO}$ = 8 mA |
| FAULT# Assertion Time | $t_{FAULT\_ASSERT}$ | — | 20 | — | µs | Time from Overvoltage detected to FAULT# assertion. |
| FAULT# Deassertion Time | $t_{FAULT\_DEASSERT}$ | — | 5 | — | ms | Time from FET turn ON after an OVP event to FAULT# deassertion. |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is guaranteed by design.

**TABLE 2-2: ELECTRICAL SPECIFICATIONS (CONTINUED)**

$T_J$ = -40 °C to 125 °C,
All typical values $T_J$ = 25 °C, VDD = 2.7V to 5.5V, unless otherwise noted.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **FCONFIG** | | | | | | |
| Input High Voltage | $V_{IH}$ | VDD – 1 | — | — | V | Note 2 |
| Input Low Voltage | $V_{IL}$ | — | — | 1 | V | Note 2 |
| Leakage Current | $I_{FCONFIG\_LEAK}$ | — | — | ±20 | µA | FCONFIG = 0V<br>FCONFIG = 5.5V |
| **SG_SENS, SG_GATE** | | | | | | |
| Short-to-GND Sense | $V_{SG\_SENS\_IH}$ | 100 | — | — | mV | Ramp up SG_SENS from 10 mV to 150 mV until SG_GATE < $V_{SG\_GATE\_OL}$ . |
| Short-to-GND Release | $V_{SG\_SENS\_IL}$ | — | — | 80 | mV | Ramp down SG_SENS from 120 mV to 0 mV until SG_GATE > $V_{SG\_GATE\_OL}$ . |
| SG_SENS Bias Current | $I_{OFFSET}$ | — | 5 | — | µA | Current coming out of SG_SENS |
| SG_SENS Discharge Current | $I_{DISCH}$ | 0.4 | 6 | 15 | µA | Current coming into SG_SENS |
| SG_GATE Output Low Voltage | $V_{SG\_GATE\_OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA<br>SG_GATE |
| Short-to-GND Response Time | $t_{STG\_RT}$ | — | 500 | — | ns | Time from short-to-GND detected until SG_GATE < $V_{SG\_GATE\_OL}$. |
| Short-to-GND Recovery Time | $t_{SG\_REC}$ | 10 | 20 | 30 | ms | Minimum time duration after short-to-GND removed condition is removed until SG_GATE > $V_{SG\_GATE\_OL}$. |
| Short-to-GND Recovery Time - Long | $t_{REC\_LONG}$ | — | 500 | — | µs | Time from removal of short-to-GND condition until SG_GATE driven ‘high’ when short-to-GND condition is longer than $t_{SG\_REC}$. |
| **Thermal** | | | | | | |
| Thermal Shutdown Threshold | $T_{TSD}$ | — | 145 | — | °C | Die Temperature at which ALL of the UCS4003 switches will turn OFF Note 1. |
| Thermal Shutdown Hysteresis | $T_{TSD\_HYST}$ | — | 40 | — | °C | After shutdown due to $T_{TSD}$ being reached, die temperature drop required before the UCS4003 can be turned ON again Note 1. |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is guaranteed by design.

## 3.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables shown following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

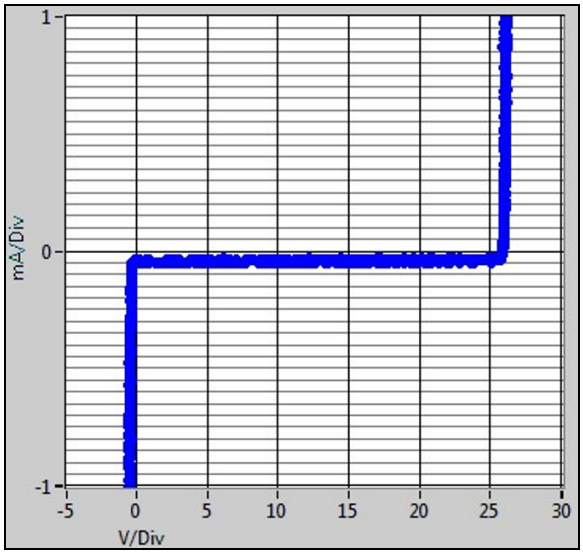



***FIGURE 3-1:*** *D±_C I-V Curve.*

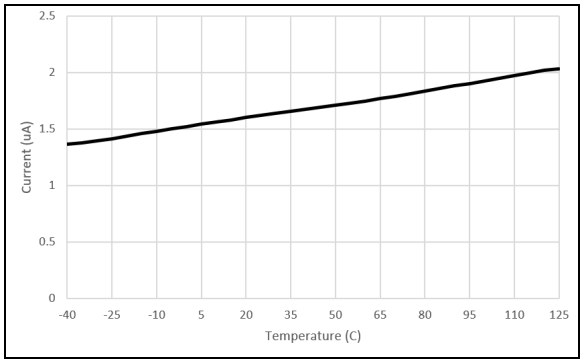



***FIGURE 3-2:*** *D±_C Short-to-5V across Temperature (Powered).*

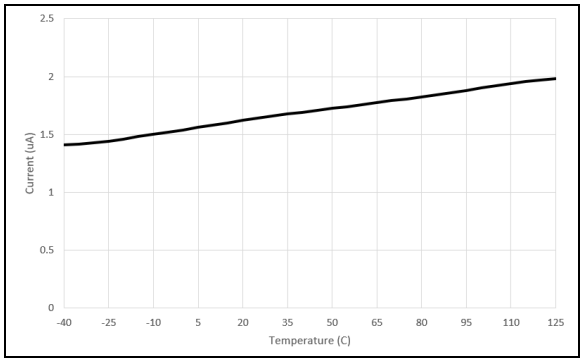



***FIGURE 3-3:*** *D±_C Short-to-5V across Temperature (Unpowered).*

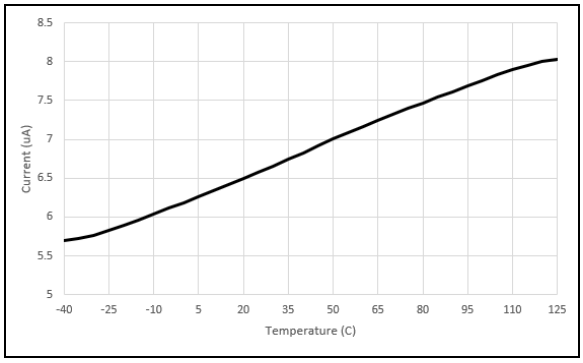



***FIGURE 3-4:*** *D±_C Short-to-20V across Temperature (Powered).*

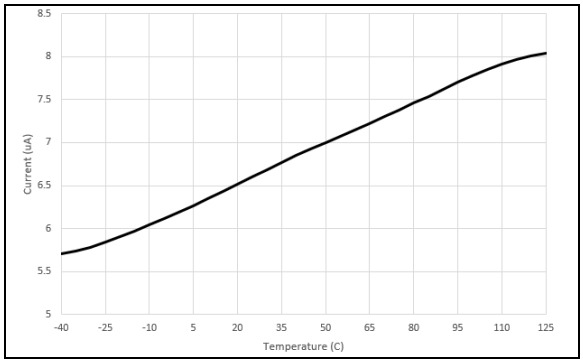



***FIGURE 3-5:*** *D±_C Short-to-20V across Temperature (Unpowered).*

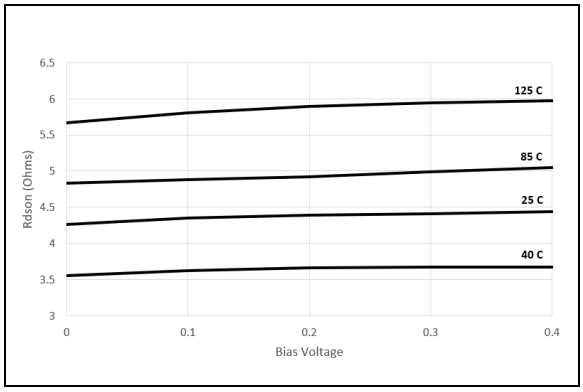



***FIGURE 3-6:*** *D± R_ON vs Bias Voltage.*

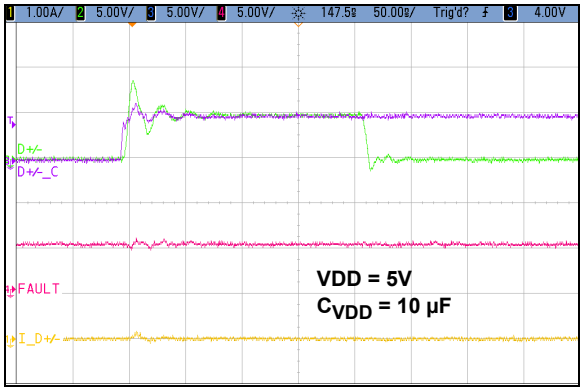



***FIGURE 3-7:*** *D± Short-to-5V Response Waveform.*

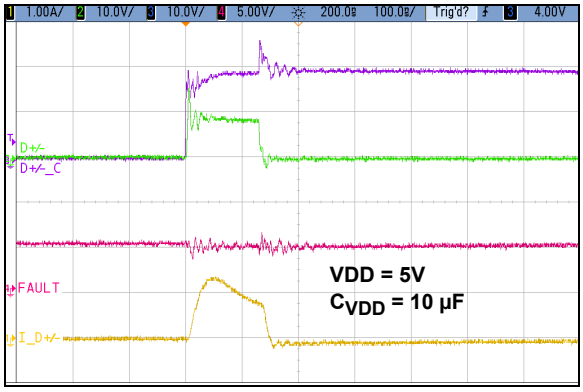



***FIGURE 3-8:*** *D± Short-to-20V Response Waveform.*

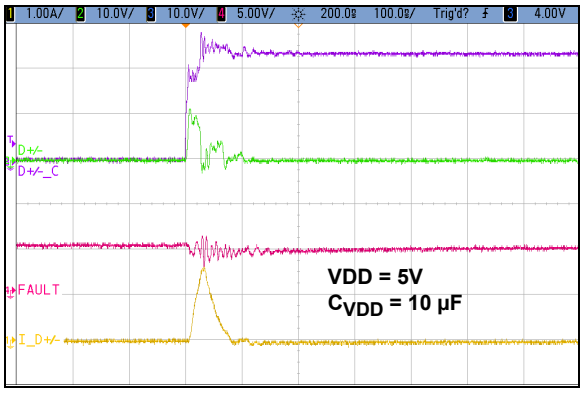



***FIGURE 3-9:*** *D± Short-to-24V Response Waveform.*

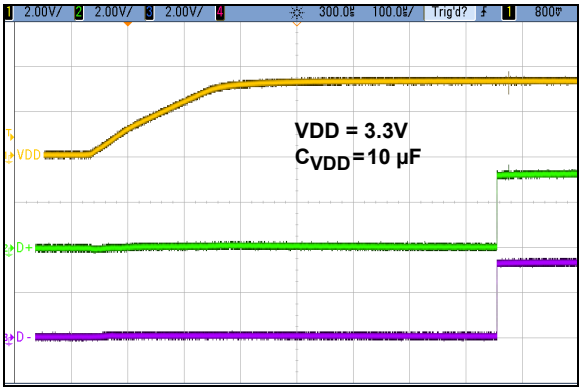



***FIGURE 3-10:*** *Soft Start Turn ON: D+/-.*

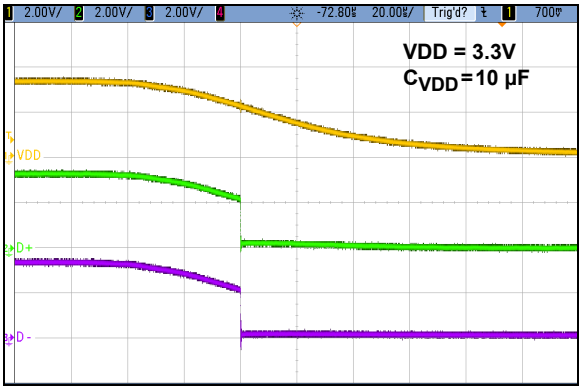



***FIGURE 3-11:*** *Soft Start Turn OFF: D+/-.*

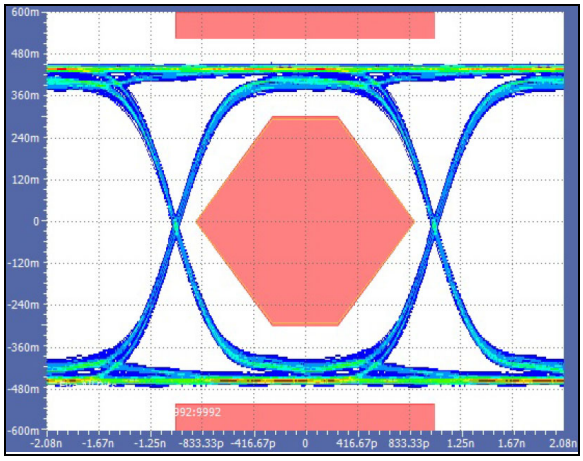



***FIGURE 3-12:*** *USB 2.0 High-Speed Eye Diagram without UCS4003.*

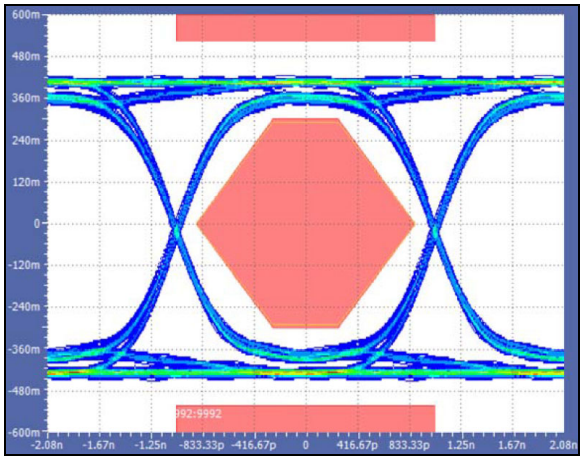



***FIGURE 3-15:*** *USB 2.0 High-Speed Eye Diagram with UCS4003.*

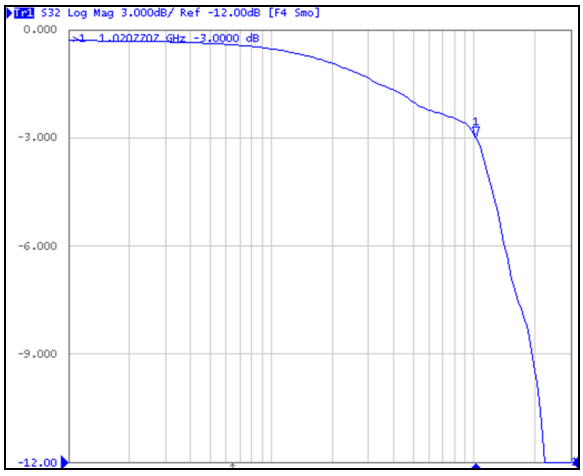



***FIGURE 3-13:*** *D+/- Single-Ended Bandwidth.*

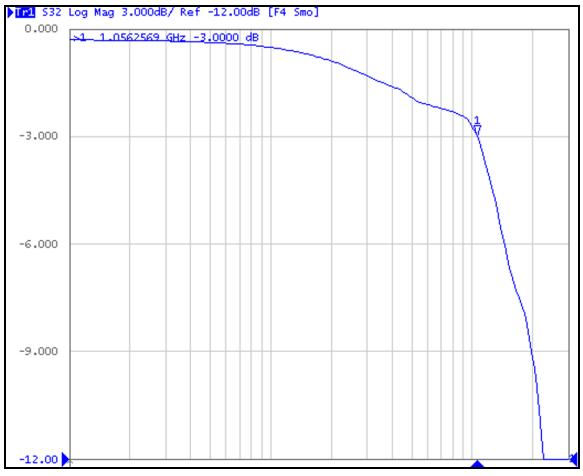



***FIGURE 3-16:*** *D+/- Differential Bandwidth.*

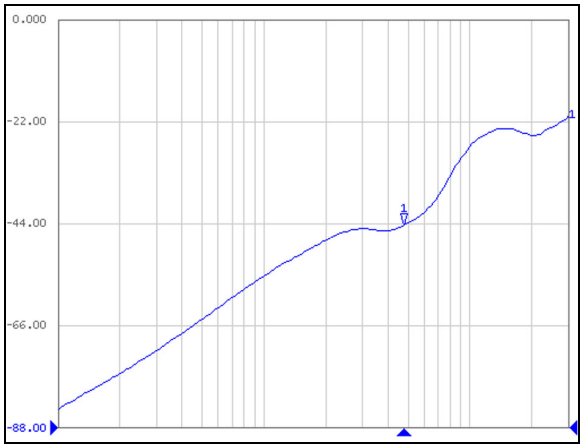



***FIGURE 3-14:*** *D+/- Crosstalk.*

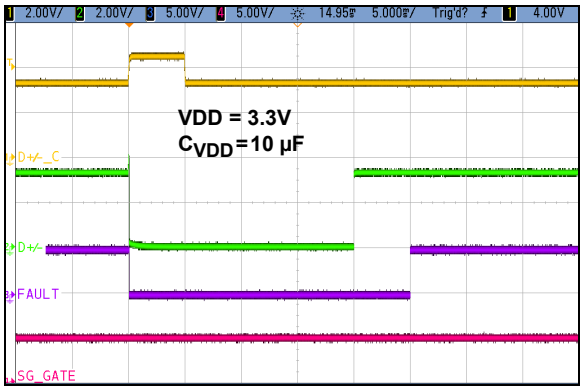



***FIGURE 3-17:*** *D+/-_C Overvoltage.*

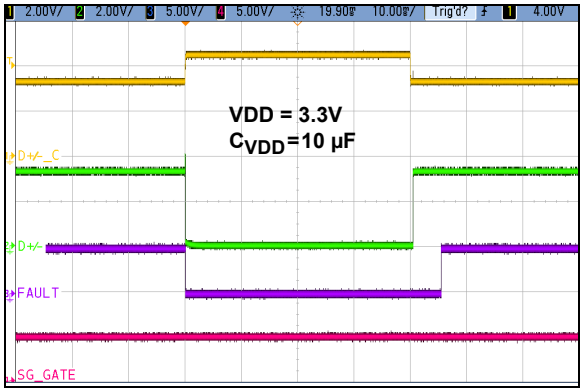



***FIGURE 3-18:*** *D+/-_C Overvoltage Long.*

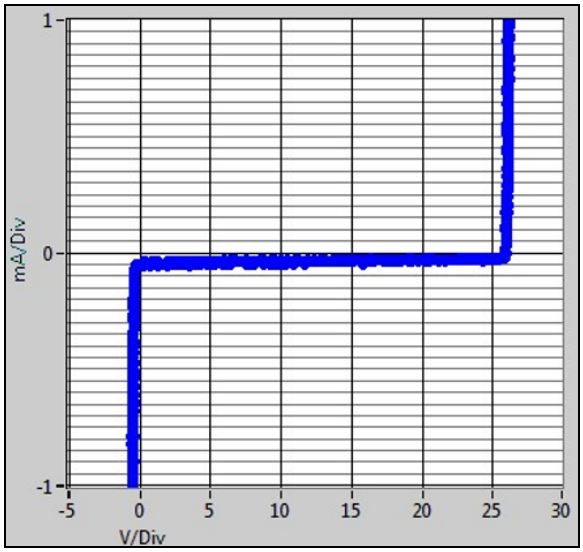



***FIGURE 3-19:*** *CC1/CC2 I-V Curve.*

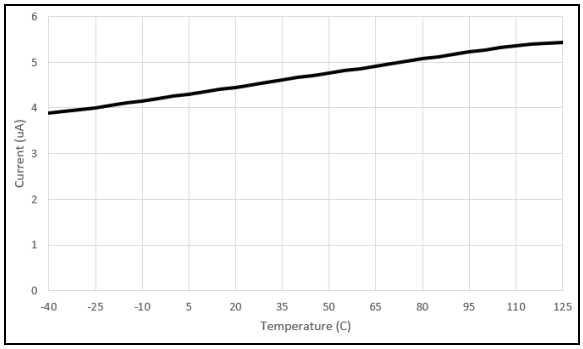



***FIGURE 3-20:*** *CC1_C/CC2_C Short-to-5.5V Across Temperature (Powered).*

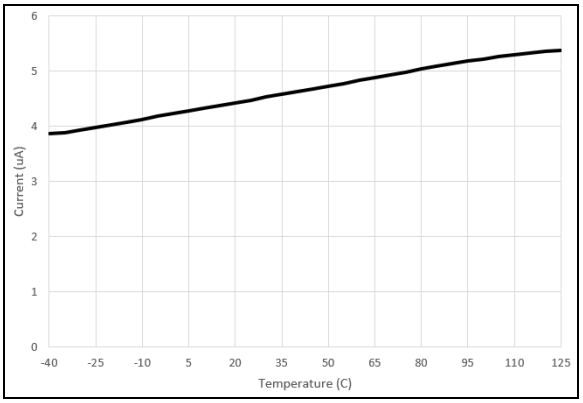



***FIGURE 3-21:*** *CC1_C/CC2_C Short-to-5.5V Across Temperature (Unpowered).*

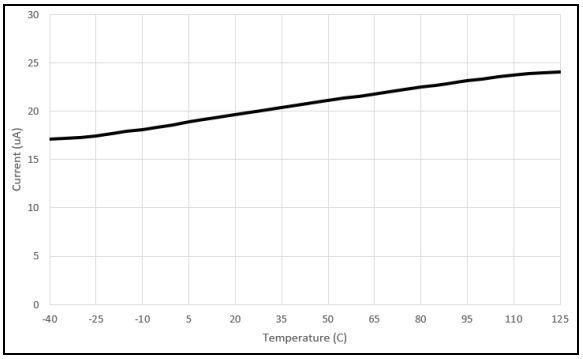



***FIGURE 3-22:*** *CC1_C/CC2_C Short-to-24V Across Temperature (Powered).*

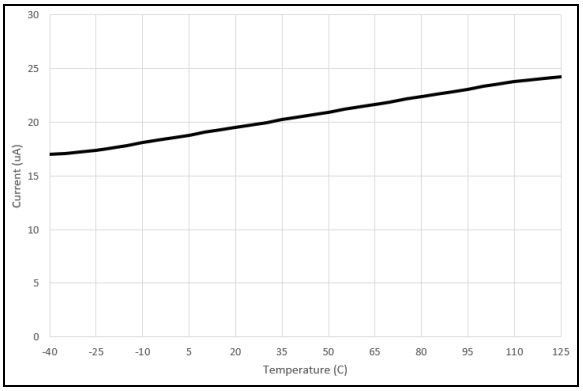



***FIGURE 3-23:*** *CC1_C/CC2_C Short-to-24V Across Temperature (Unpowered).*

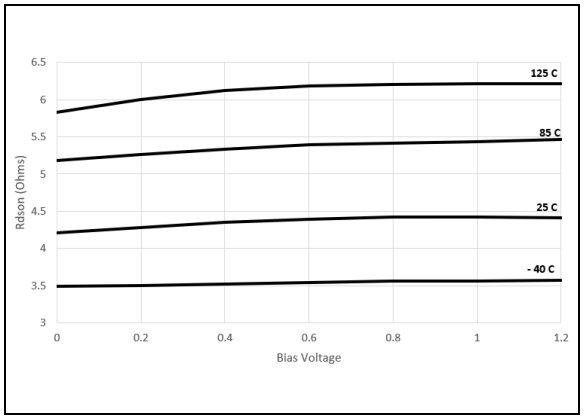



***FIGURE 3-24:*** *CC1, CC2 R_ON vs Bias Voltage.*

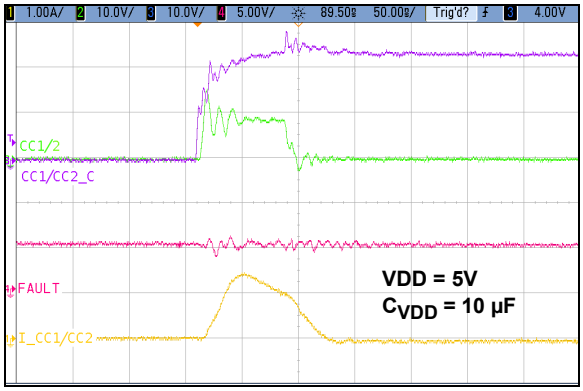



***FIGURE 3-27:*** *CC1, CC2 Short-to-24V Response Waveform.*

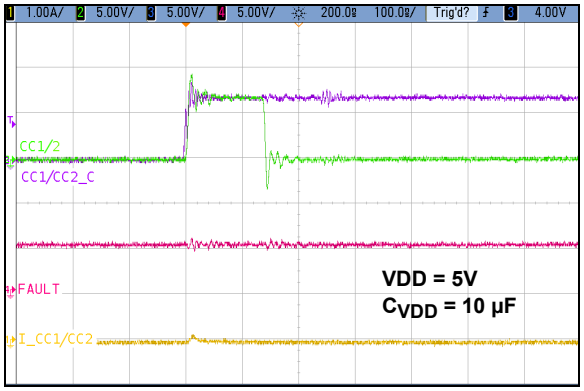



***FIGURE 3-25:*** *CC1, CC2 Short-to-7V Response Waveform.*

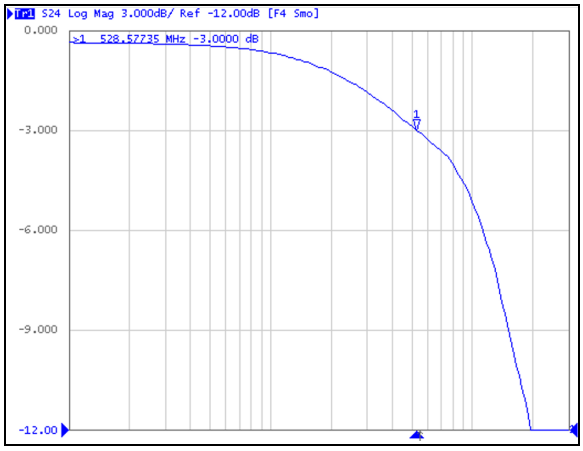



***FIGURE 3-28:*** *CC1, CC2 Bandwidth.*

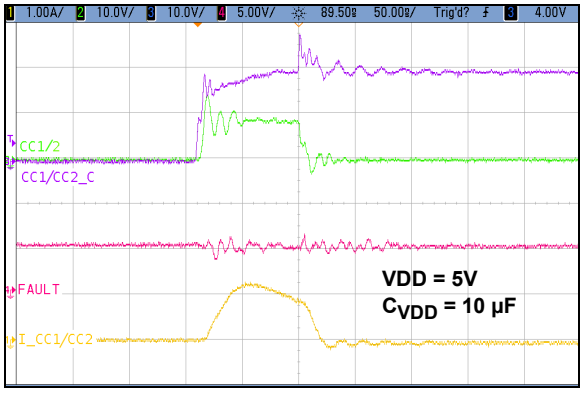



***FIGURE 3-26:*** *CC1, CC2 Short-to-20V Response Waveform.*

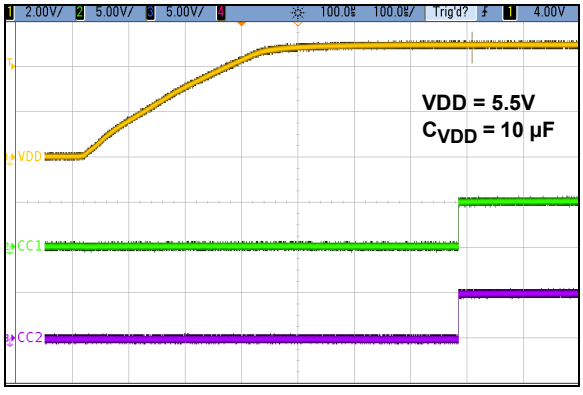



***FIGURE 3-29:*** *Soft Start Turn ON: CC1, CC2.*

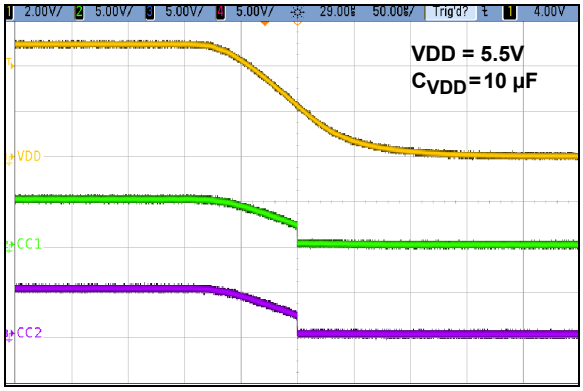



***FIGURE 3-30:*** *Soft Start Turn OFF: CC1, CC2.*

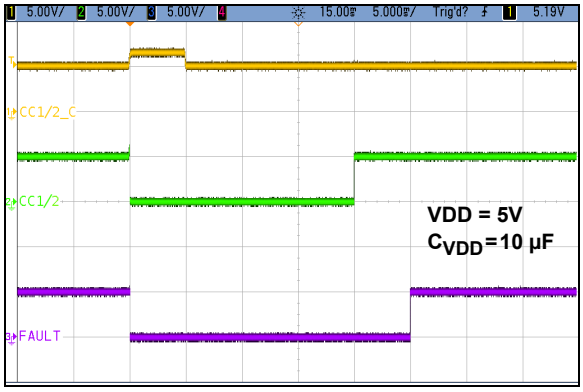



***FIGURE 3-31:*** *CC1_C, CC2_C Overvoltage.*

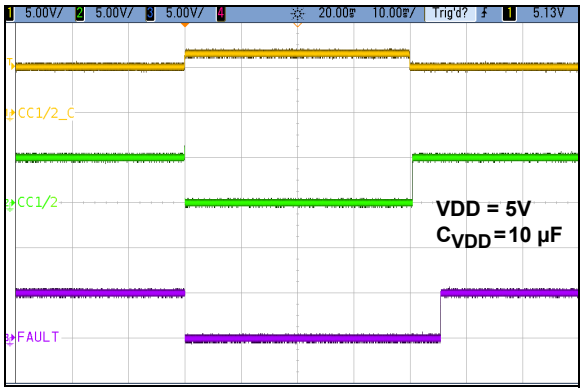



***FIGURE 3-32:*** *CC1_C, CC2_C Overvoltage Long.*

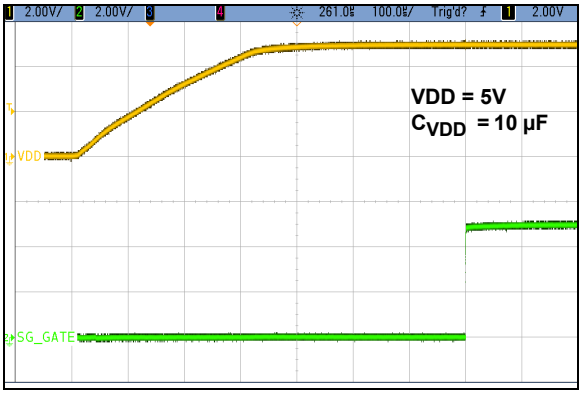



***FIGURE 3-33:*** *Soft Start Turn ON: SG_GATE.*

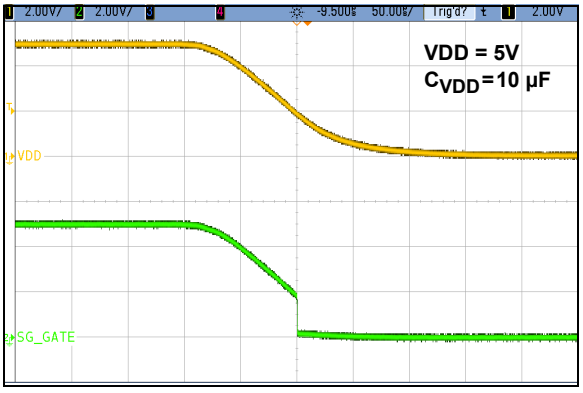



***FIGURE 3-34:*** *Soft Start Turn OFF: SG_GATE.*

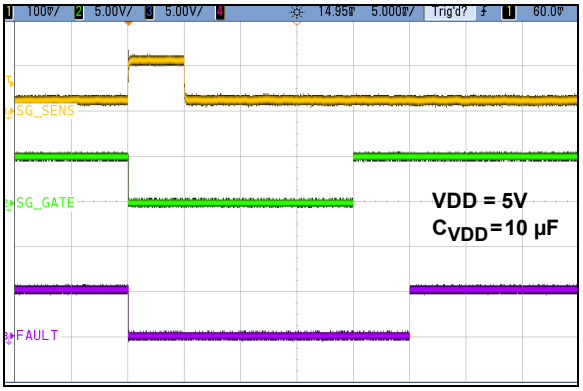



***FIGURE 3-35:*** *Battery Short-to-GND.*

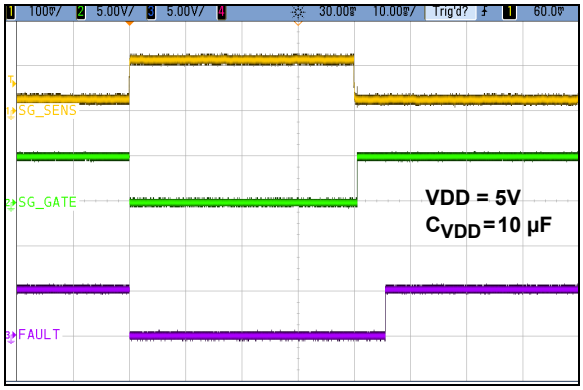
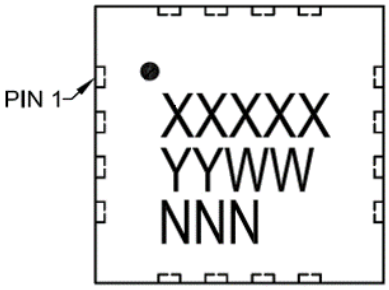



***FIGURE 3-36:*** *Battery Short-to-GND Long.*

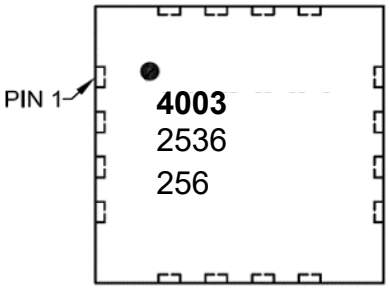
## 4.0 PACKAGING INFORMATION

### 4.1 Package Drawing

16-Lead VQFN, 3x3x1.0 mm
(UCS4003)




Example:

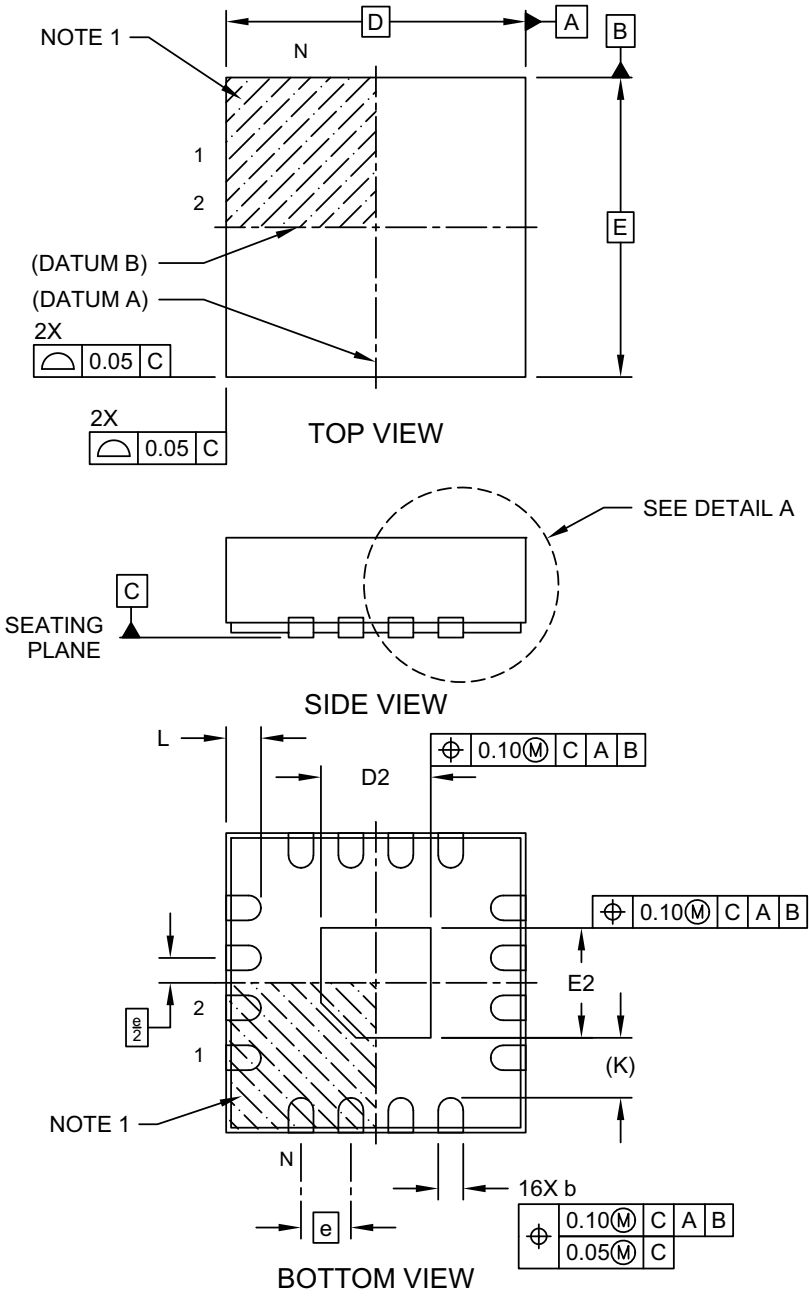



| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

**16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN]**
**Wettable Flanks (Stepped), 0.35 mm Terminal Length**

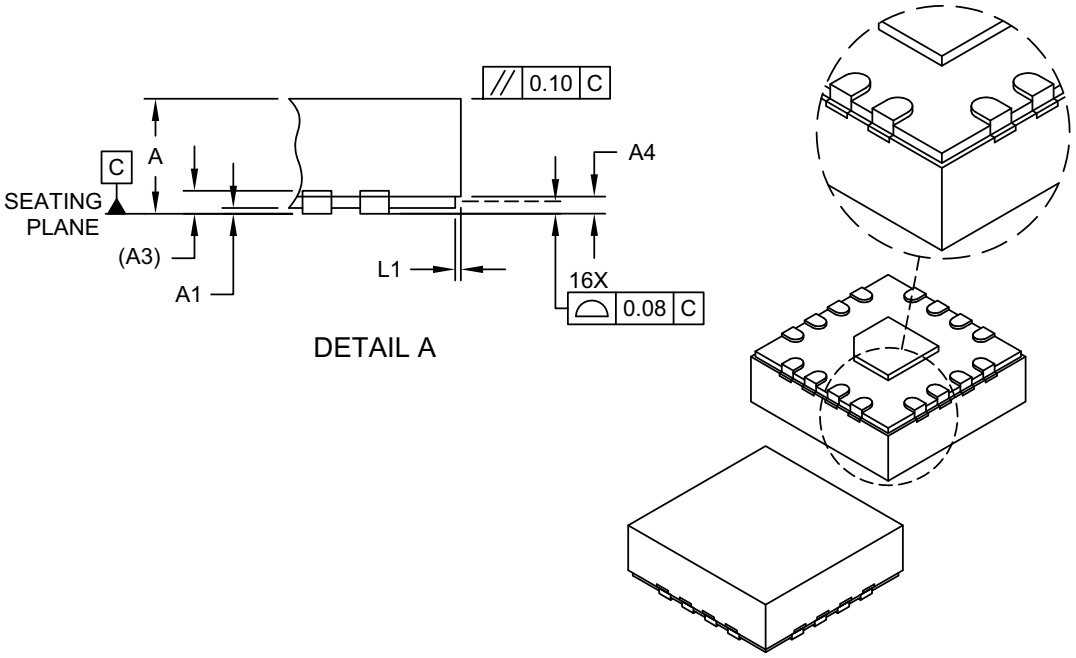
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-404-8N Rev. D Sheet 1 of 2

**16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN]**
**Wettable Flanks (Stepped), 0.35 mm Terminal Length**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Step Height | A4 | 0.10 | – | 0.19 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.20 |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.20 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.35 | 0.45 |
| Step Length | L1 | 0.035 | 0.060 | 0.085 |
| Terminal-to-Exposed Pad | K | | 0.60 REF | |

Notes:

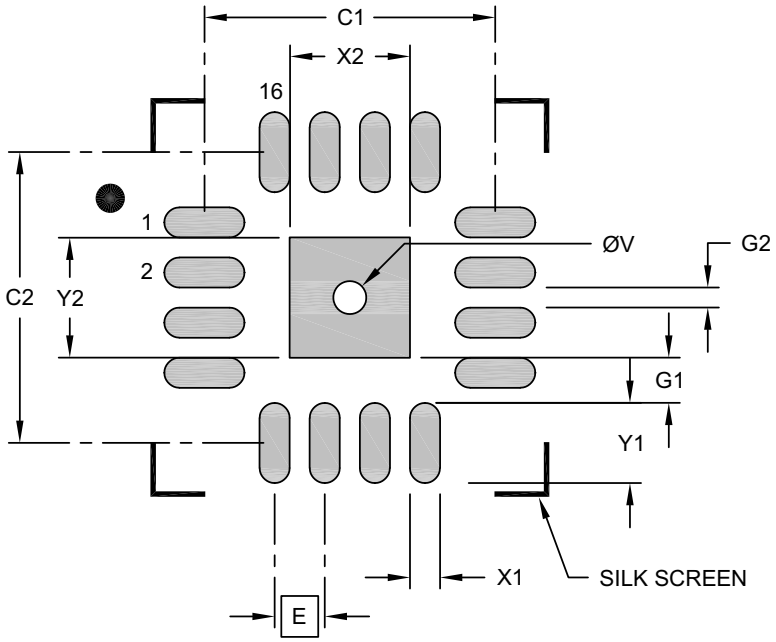
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-404-8N Rev.D Sheet 2 of 2

**16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.35 mm Terminal Length**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.20 |
| Optional Center Pad Length | Y2 | | | 1.20 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Spacing | C2 | | 2.90 | |
| Contact Pad Width (X16) | X1 | | | 0.30 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X16) | G1 | 0.30 | | |
| Contact Pad to Contact Pad (X12) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2404-8N Rev.D

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision B (December 2024)

- Updated Figure 1-7.

## Revision A (November 2024)

- Original release of this document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [T] | -X | /XX | XXX |
|---|---|---|---|---|
| Device | Tape and Reel | Temperature Range | Package | Qualification |

| | | |
|---|---|---|
| **Device:** | UCS4003: | Type-C Power Delivery (PD) port protector for D+, D- and CC |
| **Tape and Reel Option(1):** | (Blank)<br>T | = Standard packaging (tube: 120/tube)<br>= Tape and Reel[1] (3300/reel) |
| **Temperature Range:** | E | = -40°C to +125°C (Extended) |
| **Package:** | 8N | = Very Thin Quad Flatpack No-leads (VQFN) Package, with Wettable Flanks - 3x3x1.0 mm Body with 0.35 mm Terminal Contact Length, 16-lead (code: 8N) |
| **Qualification*:** | (Blank)<br>VAO | = Standard Part<br>= AEC-Q100 Automotive Qualified |

**Examples:**

a) UCS4003-E/8N: USB Type-C PD port protector for D+, D- and CC, Extended Temperature, VQFN Package, Standard Packaging (tube)

b) UCS4003T-E/8N: USB Type-C PD port protector for D+, D- and CC, Extended Temperature, VQFN Package, Tape and Reel

c) UCS4003-E/8NVAO: USB Type-C PD port protector for D+, D- and CC, Extended Temperature, VQFN Package, Standard Packaging (tube), AEC-Q100 Automotive Qualified

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

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