MICRON TECHNOLOGY, INC.

# 16 MEG x 4 EDO DRAM

# DRAM

MT4LC16M4G3
MT4LC16M4H9

## FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 12 row, 12 column addresses (H9) or 13 row, 11 column addresses (G3)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access cycle
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms

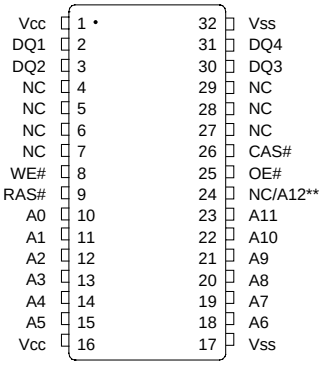
## OPTIONS — MARKING

- Refresh Addressing
  - 4,096 (i.e. 4K) Rows — H9
  - 8,192 (i.e. 8K) Rows — G3
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG*
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Part Number Example: MT4LC16M4H9DJ-5

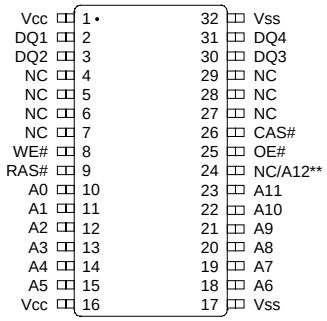
***Note:*** *The 16 Meg x 4 EDO DRAM base number differentiates the offerings in one place -* MT4LC16M4H9*. The fifth field distinguishes the address offerings: H9 designates 4K addresses and G3 designates 8K addresses.*

## PIN ASSIGNMENT (Top View)

**32-Pin SOJ** (DA-5)




**32-Pin TSOP*** (DB-4)




* Consult factory for availability
** NC on H9 version, A12 on G3 version

**Note:** The "#" symbol indicates signal is active LOW.

## KEY TIMING PARAMETERS

| SPEED | tRC | tRAC | tPC | tAA | tCAC | tCAS |
|---|---|---|---|---|---|---|
| -5 | 84ns | 50ns | 20ns | 25ns | 13ns | 8ns |
| -6 | 104ns | 60ns | 25ns | 30ns | 15ns | 10ns |

## 16 MEG x 4 PART NUMBERS

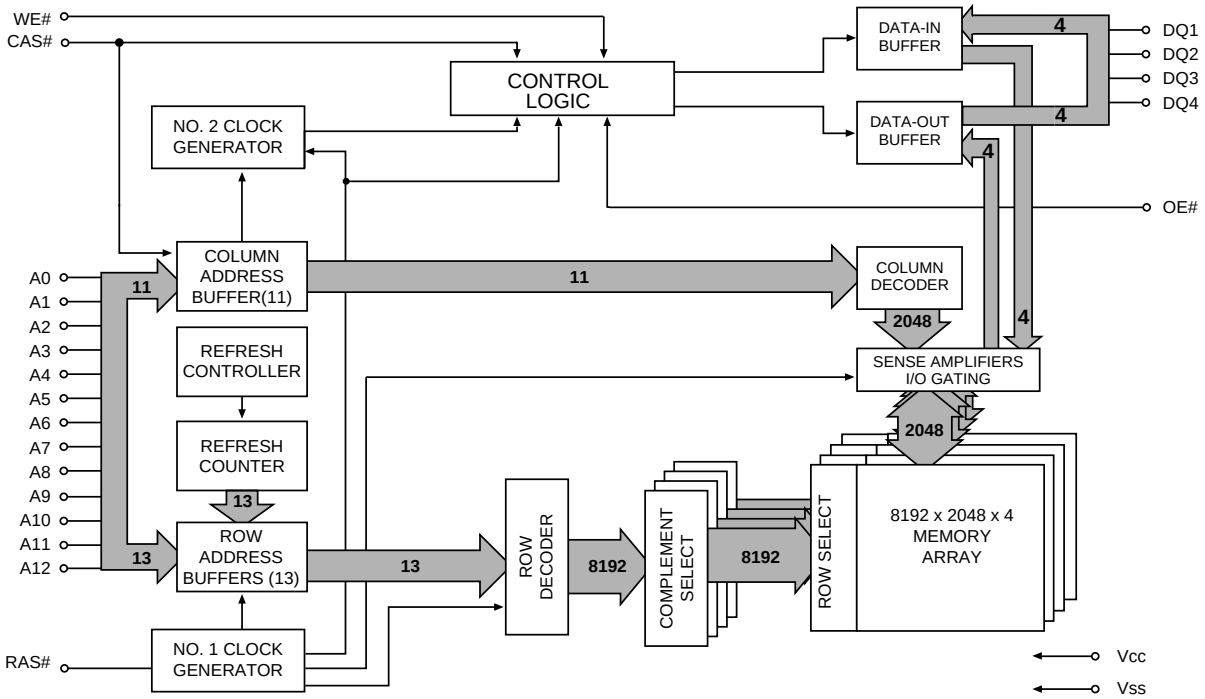
| PART NUMBER | Vcc | ADDRESSING | PACKAGE |
|---|---|---|---|
| MT4LC16M4H9DJ | 3.3V | 4K | SOJ |
| MT4LC16M4H9TG | 3.3V | 4K | TSOP |
| MT4LC16M4G3DJ | 3.3V | 8K | SOJ |
| MT4LC16M4G3TG | 3.3V | 8K | TSOP |

## GENERAL DESCRIPTION

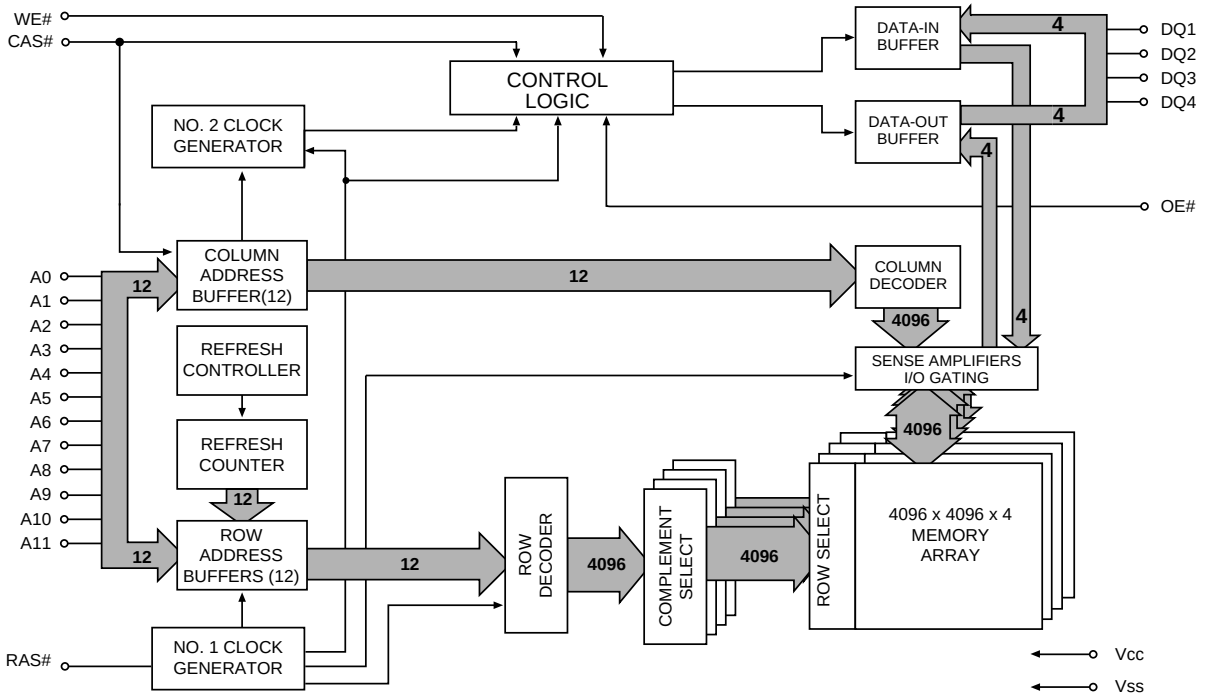
The 16 Meg x 4 DRAM is a high-speed CMOS, dynamic random-access memory device containing 67,108,864 bits and designed to operate from 3V to 3.6V. The MT4LC16M4H9 and MT4LC16M4G3 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 4,096 rows by 4,096 columns on the H9 version, while the G3 version is arranged in 8,192 rows by 2,048 columns. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address is latched by CAS#. The device provides EDO PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The 16 Meg x 4 DRAM must be refreshed periodically in order to retain stored data.

## FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4G3 (13 row addresses)




## FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4H9 (12 row addresses)



## FUNCTIONAL DESCRIPTION

The functional description for the 16 Meg x 4 DRAM is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet, following the timing specifications tables.

## DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ1-4). A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location.

## EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. If CAS# went HIGH and OE# was LOW (active), the output buffers would be disabled. The 16 Meg x 4 DRAM offers an accelerated PAGE MODE cycle by eliminating output disable from CAS# HIGH. This option is called EDO and it allows CAS# precharge time ($^{t}$CP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. OE# can be brought LOW or HIGH while CAS# and RAS# are LOW, and the DQs will transition between valid data and High-Z. Using OE#, there are two methods to disable the outputs and keep them disabled during the CAS# HIGH time. The first method is to have OE# HIGH when CAS# transitions HIGH and keep OE# HIGH for $^{t}$OEHC thereafter. This will disable the DQs and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. The second method is to have OE# LOW when CAS# transitions HIGH and then bring OE# HIGH for a minimum of $^{t}$OEP anytime during the CAS# HIGH period. This will disable the DQs and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. (Please refer to

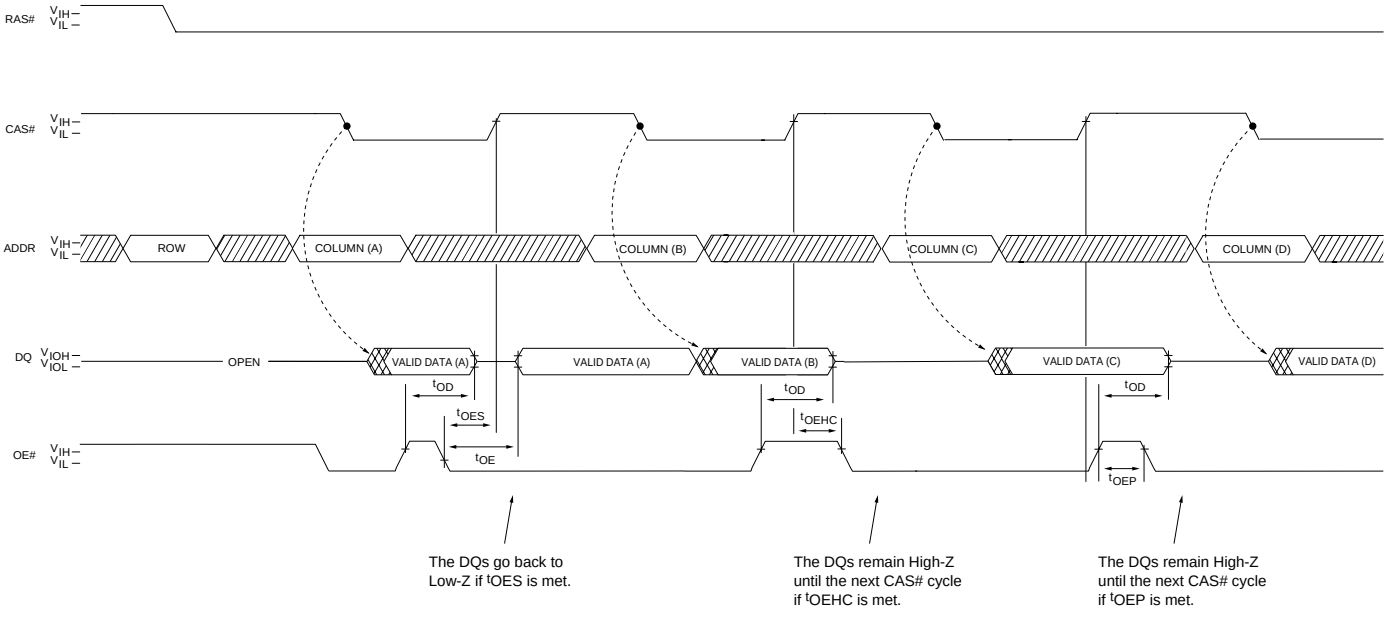



**Figure 1**
**OE# CONTROL OF DQs**

## EDO PAGE MODE (continued)

Figure 1.) During other cycles, the outputs are disabled at $^{t}$OFF time after RAS# and CAS# are HIGH or at $^{t}$WHZ after WE# transitions LOW. The $^{t}$OFF time is referenced from the rising edge of RAS# or CAS#, whichever occurs last. WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO PAGE MODE operations are always initiated with a row address strobed-in by the RAS# signal, followed by a column address strobed-in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO PAGE MODE operation.

## DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all rows in the 16 Meg x 4 DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method some compatibility issues may become apparent. For example, both G3 and H9 versions require 4,096 CBR REFRESH cycles, yet require a different number of RAS#-ONLY REFRESH cycles (G3 = 8,192 and H9 = 4,096). JEDEC strongly recommends the use of CBR REFRESH for this device.

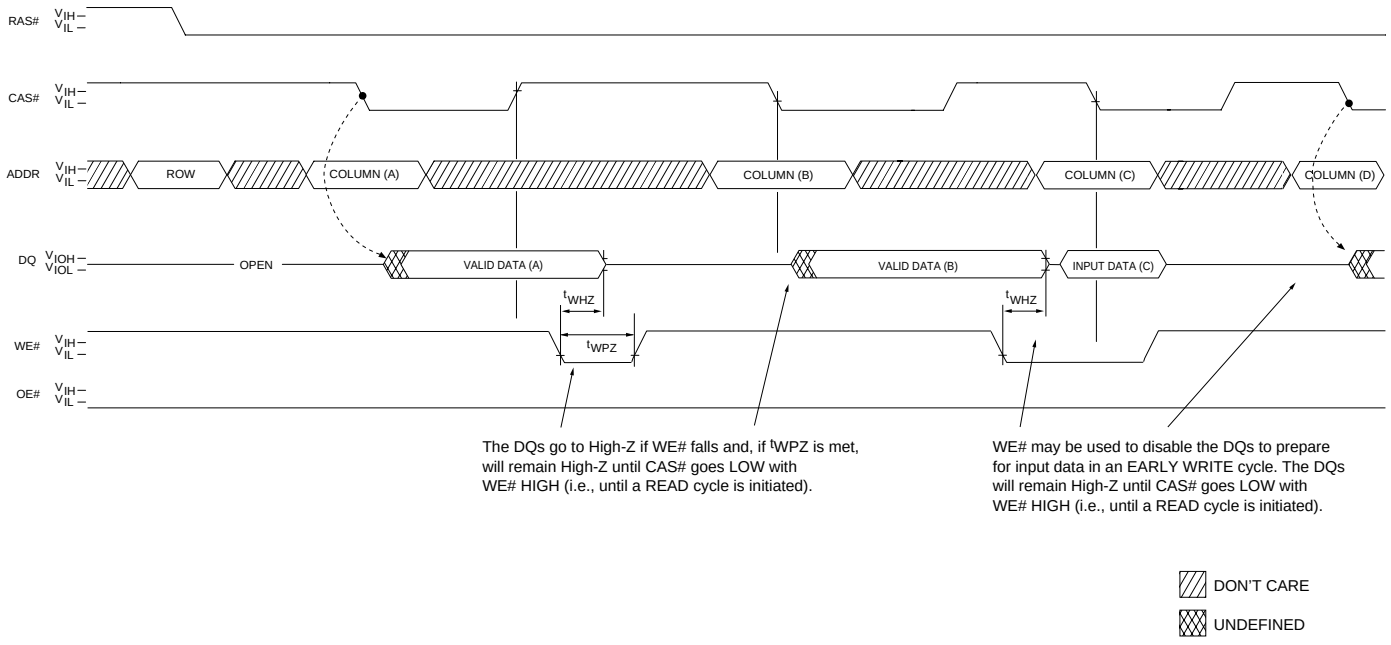



**Figure 2**
**WE# CONTROL OF DQs**

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ Relative to $V_{SS}$ ..... -1V to +4.6V
Voltage on NC, Inputs or I/O Pins
Relative to $V_{SS}$ ..... -1V to +4.6V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) ($V_{CC}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.6 | V | |
| Input High (Logic 1) Voltage, all inputs | $V_{IH}$ | 2.0 | $V_{CC}$ +.3 | V | |
| Input Low (Logic 0) Voltage, all inputs | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{CC}$ +.3V<br>(All other pins not under test = 0V) | $I_I$ | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ $V_{OUT}$ ≤ $V_{CC}$ +.3V) | $I_{OZ}$ | -5 | 5 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -2mA) | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 2mA) | $V_{OL}$ | | 0.4 | V | |

| PARAMETER/CONDITION | SYMBOL | SPEED | 4K ROW ADDRESSING | 8K ROW ADDRESSING | UNITS | NOTES |
|---|---|---|---|---|---|---|
| STANDBY CURRENT: (TTL)<br>(RAS# = CAS# = $V_{IH}$) | $I_{CC1}$ | ALL | 1 | 1 | mA | |
| STANDBY CURRENT: (CMOS)<br>(RAS# = CAS# ≥ $V_{CC}$ -0.2V, DQs may be left open, other inputs: $V_{IN}$ ≥ $V_{CC}$ -0.2V or $V_{IN}$ ≤ 0.2V) | $I_{CC2}$ | ALL | 500 | 500 | µA | |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | -5<br>-6 | 170<br>160 | 130<br>120 | mA | 3, 25 |
| OPERATING CURRENT: EDO PAGE MODE<br>Average power supply current (RAS# = $V_{IL}$,<br>CAS#, address cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC4}$ | -5<br>-6 | 150<br>120 | 150<br>120 | mA | 3, 25 |
| REFRESH CURRENT: RAS#-ONLY<br>Average power supply current<br>(RAS# cycling, CAS# = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC5}$ | -5<br>-6 | 170<br>160 | 130<br>120 | mA | 3, 22 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | -5<br>-6 | 170<br>160 | 130<br>120 | mA | 3, 4 |

## CAPACITANCE

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance: Address pins | $C_{I1}$ | 5 | pF | 2 |
| Input Capacitance: RAS#, CAS#, WE#, OE# | $C_{I2}$ | 7 | pF | 2 |
| Input/Output Capacitance: DQ | $C_{IO}$ | 7 | pF | 2 |

## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 20) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS | | -5 | | -6 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column address | $^tAA$ | | 25 | | 30 | ns | |
| Column address setup to CAS# precharge | $^tACH$ | 12 | | 15 | | ns | |
| Column address hold time (referenced to RAS#) | $^tAR$ | 38 | | 45 | | ns | |
| Column address setup time | $^tASC$ | 0 | | 0 | | ns | |
| Row address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Column address to WE# delay time | $^tAWD$ | 42 | | 49 | | ns | 18 |
| Access time from CAS# | $^tCAC$ | | 13 | | 15 | ns | |
| Column address hold time | $^tCAH$ | 8 | | 10 | | ns | |
| CAS# pulse width | $^tCAS$ | 8 | 10,000 | 10 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | $^tCHR$ | 8 | | 10 | | ns | 4 |
| CAS# to output in Low-Z | $^tCLZ$ | 0 | | 0 | | ns | |
| Data output hold after CAS# LOW | $^tCOH$ | 3 | | 3 | | ns | |
| CAS# precharge time | $^tCP$ | 8 | | 10 | | ns | 13 |
| Access time from CAS# precharge | $^tCPA$ | | 28 | | 35 | ns | |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | 5 | | ns | |
| CAS# hold time | $^tCSH$ | 38 | | 45 | | ns | |
| CAS# setup time (CBR REFRESH) | $^tCSR$ | 5 | | 5 | | ns | 4 |
| CAS# to WE# delay time | $^tCWD$ | 28 | | 35 | | ns | 18 |
| Write command to CAS# lead time | $^tCWL$ | 8 | | 10 | | ns | |
| Data-in hold time | $^tDH$ | 8 | | 10 | | ns | 19 |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 19 |
| Output disable | $^tOD$ | 0 | 12 | 0 | 15 | ns | 23, 24 |
| Output Enable time | $^tOE$ | | 12 | | 15 | ns | |
| OE# hold time from WE# during READ-MODIFY-WRITE cycle | $^tOEH$ | 8 | | 10 | | ns | 24 |
| OE# HIGH hold time from CAS# HIGH | $^tOEHC$ | 5 | | 10 | | ns | |
| OE# HIGH pulse width | $^tOEP$ | 5 | | 5 | | ns | |
| OE# LOW to CAS# HIGH setup time | $^tOES$ | 4 | | 5 | | ns | |
| Output buffer turn-off delay | $^tOFF$ | 0 | 12 | 0 | 15 | ns | 17, 23 |

## AC ELECTRICAL CHARACTERISTICS

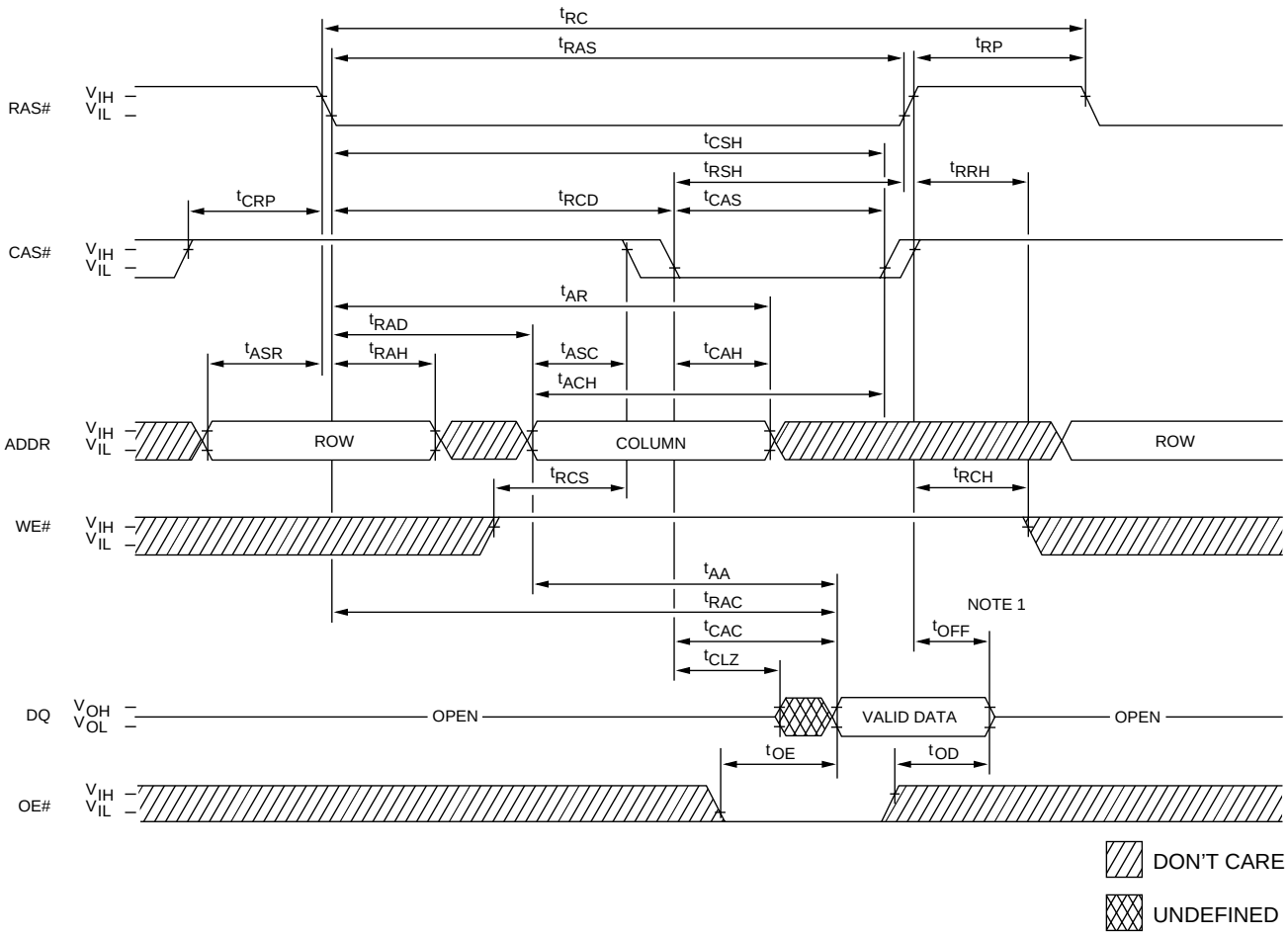
(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 20) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS | | -5 | | -6 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| OE# setup prior to RAS# during HIDDEN REFRESH cycle | $^{t}$ORD | 0 | | 0 | | ns | |
| EDO-PAGE-MODE READ or WRITE cycle time | $^{t}$PC | 20 | | 25 | | ns | |
| EDO-PAGE-MODE READ-WRITE cycle time | $^{t}$PRWC | 47 | | 56 | | ns | |
| Access time from RAS# | $^{t}$RAC | | 50 | | 60 | ns | |
| RAS# to column address delay time | $^{t}$RAD | 9 | | 12 | | ns | 15 |
| Row address hold time | $^{t}$RAH | 9 | | 10 | | ns | |
| RAS# pulse width | $^{t}$RAS | 50 | 10,000 | 60 | 10,000 | ns | |
| RAS# pulse width (EDO PAGE MODE) | $^{t}$RASP | 50 | 125,000 | 60 | 125,000 | ns | |
| Random READ or WRITE cycle time | $^{t}$RC | 84 | | 104 | | ns | |
| RAS# to CAS# delay time | $^{t}$RCD | 11 | | 14 | | ns | 14 |
| Read command hold time (referenced to CAS#) | $^{t}$RCH | 0 | | 0 | | ns | 16 |
| Read command setup time | $^{t}$RCS | 0 | | 0 | | ns | |
| Refresh period | $^{t}$REF | | 64 | | 64 | ms | 22 |
| RAS# precharge time | $^{t}$RP | 30 | | 40 | | ns | |
| RAS# to CAS# precharge time | $^{t}$RPC | 5 | | 5 | | ns | |
| Read command hold time (referenced to RAS#) | $^{t}$RRH | 0 | | 0 | | ns | 16 |
| RAS# hold time | $^{t}$RSH | 13 | | 15 | | ns | |
| READ WRITE cycle time | $^{t}$RWC | 116 | | 140 | | ns | |
| RAS# to WE# delay time | $^{t}$RWD | 67 | | 79 | | ns | 18 |
| Write command to RAS# lead time | $^{t}$RWL | 13 | | 15 | | ns | |
| Transition time (rise or fall) | $^{t}$T | 2 | 50 | 2 | 50 | ns | |
| Write command hold time | $^{t}$WCH | 8 | | 10 | | ns | |
| Write command hold time (referenced to RAS#) | $^{t}$WCR | 38 | | 45 | | ns | |
| WE# command setup time | $^{t}$WCS | 0 | | 0 | | ns | 18 |
| WE# to outputs in High-Z | $^{t}$WHZ | 0 | 12 | 0 | 15 | ns | |
| Write command pulse width | $^{t}$WP | 5 | | 5 | | ns | |
| WE# pulse width to disable outputs | $^{t}$WPZ | 10 | | 10 | | ns | |
| WE# hold time (CBR REFRESH) | $^{t}$WRH | 8 | | 10 | | ns | |
| WE# setup time (CBR REFRESH) | $^{t}$WRP | 8 | | 10 | | ns | |

## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = +3V; f = 1 MHz.
3. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 2.5ns.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If CAS# and RAS# = $V_{IH}$, data output is High-Z.
11. If CAS# = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF; and $V_{OL}$ = 0.8V and $V_{OH}$ = 2V.
13. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for $^{t}$CP.
14. The $^{t}$RAD (MAX) limit is no longer specified. $^{t}$RAD (MAX) was specified as a reference point only. If $^{t}$RAD was greater than the specified $^{t}$RAD (MAX) limit, then access time was controlled exclusively by $^{t}$AA ($^{t}$RAC and $^{t}$CAC no longer applied). With or without the $^{t}$RAD (MAX) limit, $^{t}$AA, $^{t}$RAC and $^{t}$CAC must always be met.
15. The $^{t}$RCD (MAX) limit is no longer specified. $^{t}$RCD (MAX) was specified as a reference point only. If $^{t}$RCD was greater than the specified $^{t}$RCD (MAX) limit, then access time was controlled exclusively by $^{t}$CAC ($^{t}$RAC [MIN] no longer applied). With or without the $^{t}$RCD limit, $^{t}$AA and $^{t}$CAC must always be met.
16. Either $^{t}$RCH or $^{t}$RRH must be satisfied for a READ cycle.
17. $^{t}$OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
18. $^{t}$WCS, $^{t}$RWD, $^{t}$AWD and $^{t}$CWD are not restrictive operating parameters. $^{t}$WCS applies to EARLY WRITE cycles. If $^{t}$WCS > $^{t}$WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. $^{t}$RWD, $^{t}$AWD and $^{t}$CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. $^{t}$WCS, $^{t}$RWD, $^{t}$CWD and $^{t}$AWD are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
22. RAS#-ONLY REFRESH requires that all rows be refreshed at least once every 64ms (4,096 rows for the H9 version and 8,192 rows for the G3 version). CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.
23. The DQs open during READ cycles once $^{t}$OD or $^{t}$OFF occur. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^{t}$OD and $^{t}$OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
25. Column address changed once each cycle.

## READ CYCLE



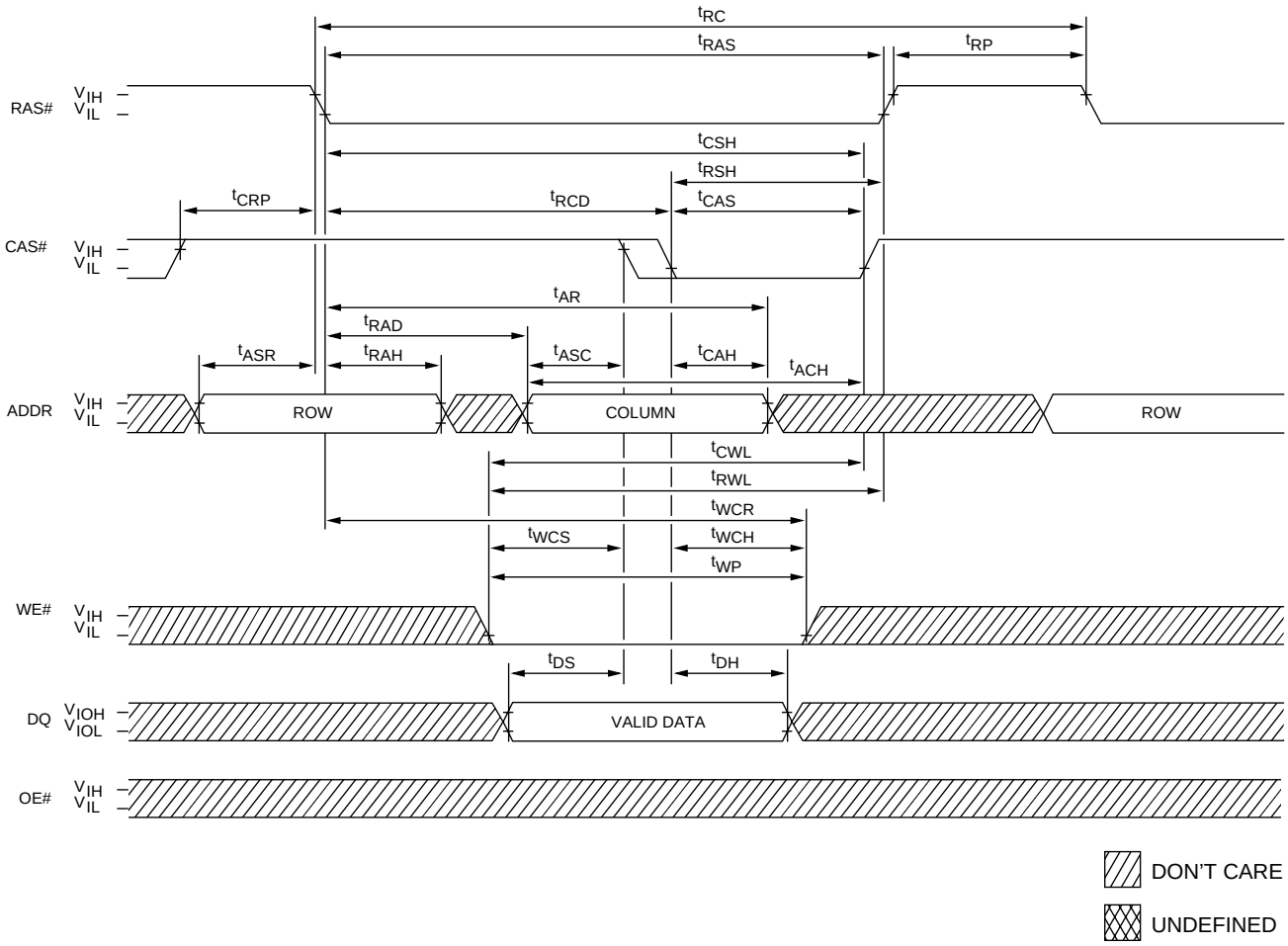

### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOFF | 0 | 12 | 0 | 15 | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

**NOTE:** 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

## EARLY WRITE CYCLE

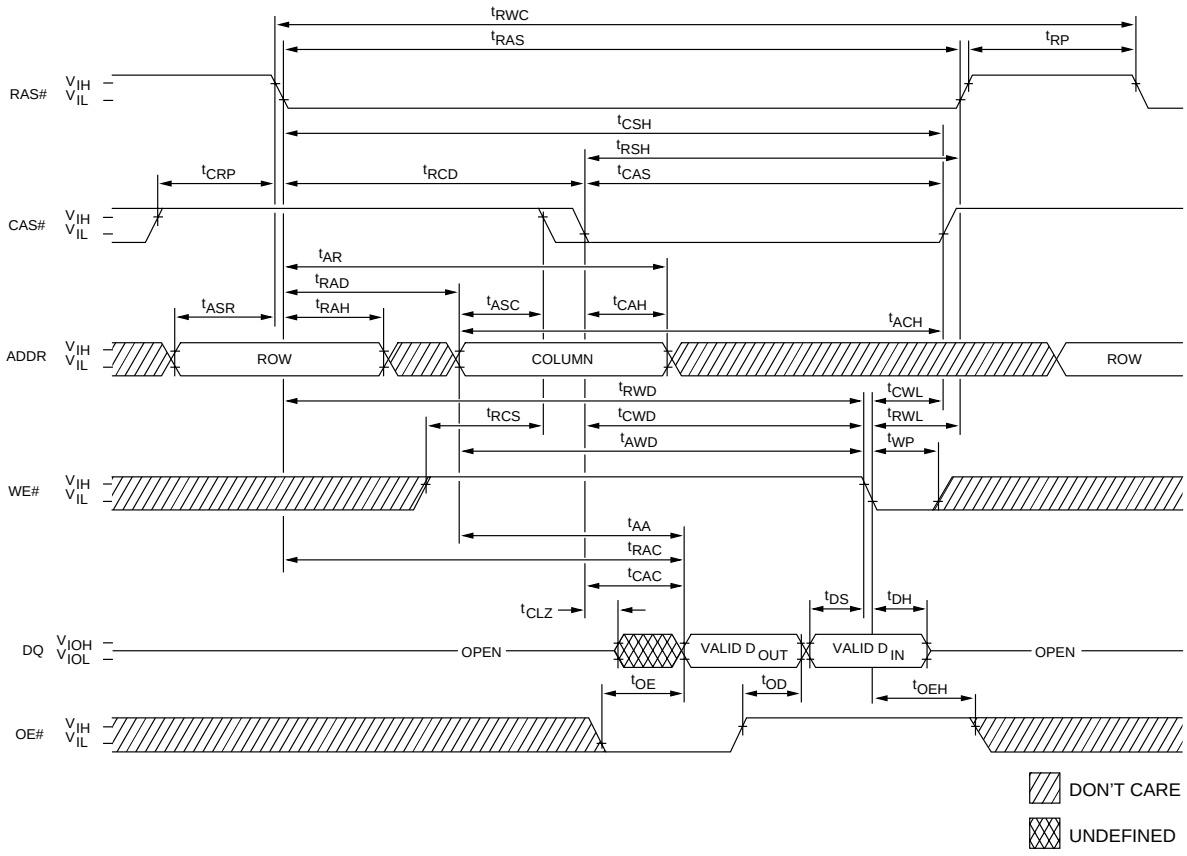



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWL | 8 | | 15 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |
| tRAD | 9 | | 12 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 5 | | 5 | | ns |

## READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

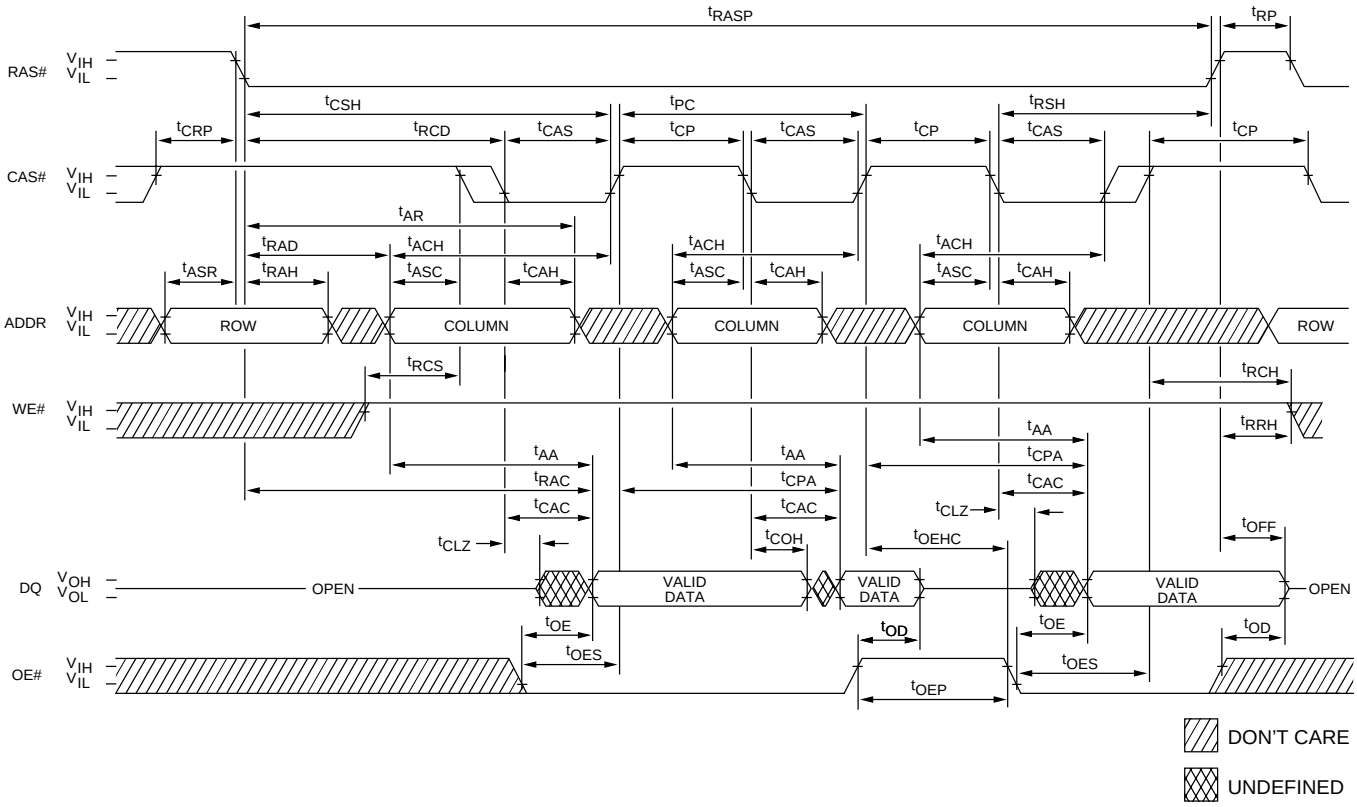



### TIMING PARAMETERS

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 42 | | 49 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWD | 28 | | 35 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tOEH | 8 | | 10 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWC | 116 | | 140 | | ns |
| tRWD | 67 | | 79 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWP | 5 | | 5 | | ns |

## EDO-PAGE-MODE READ CYCLE

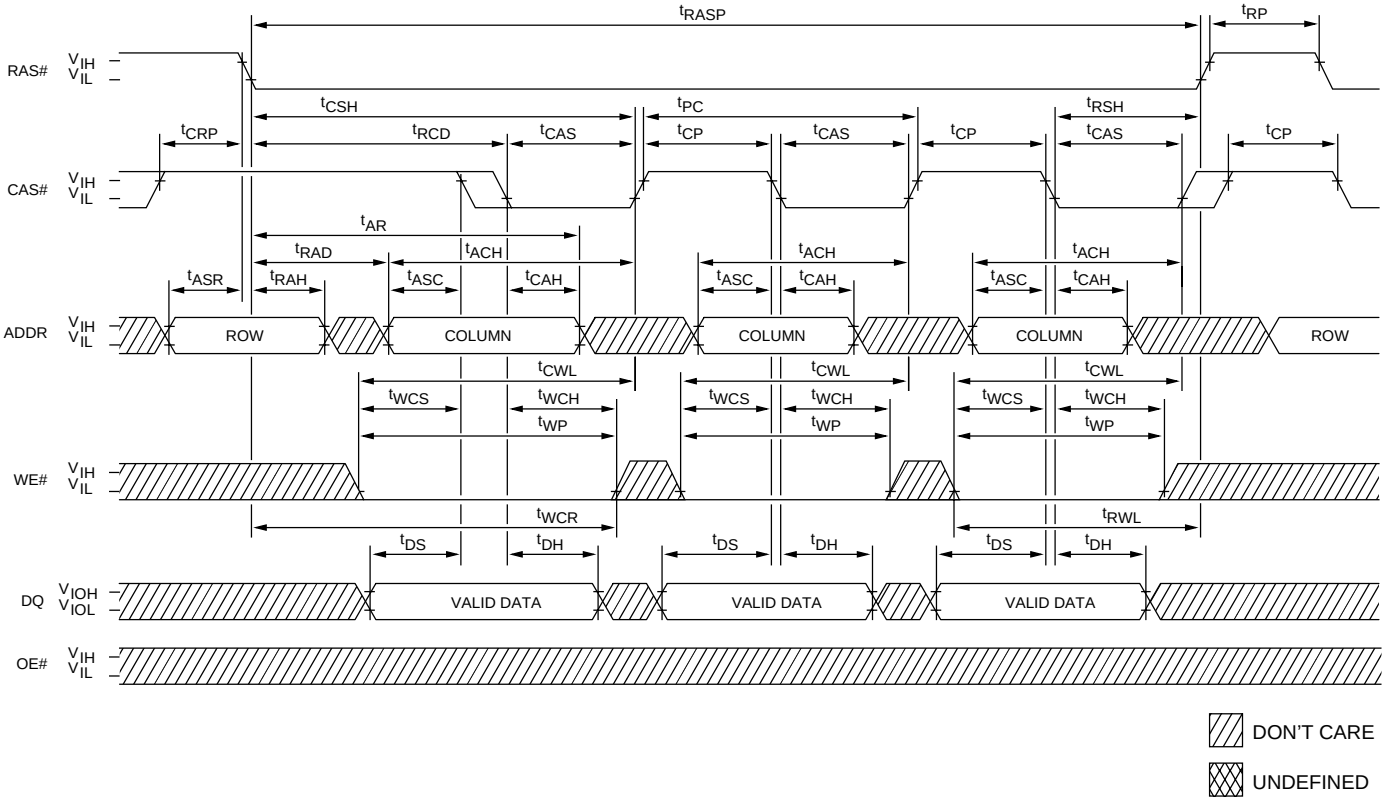



### TIMING PARAMETERS

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tOEHC | 5 | | 10 | | ns |
| tOEP | 5 | | 5 | | ns |
| tOES | 4 | | 5 | | ns |
| tOFF | 0 | 12 | 0 | 15 | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

## EDO-PAGE-MODE EARLY WRITE CYCLE

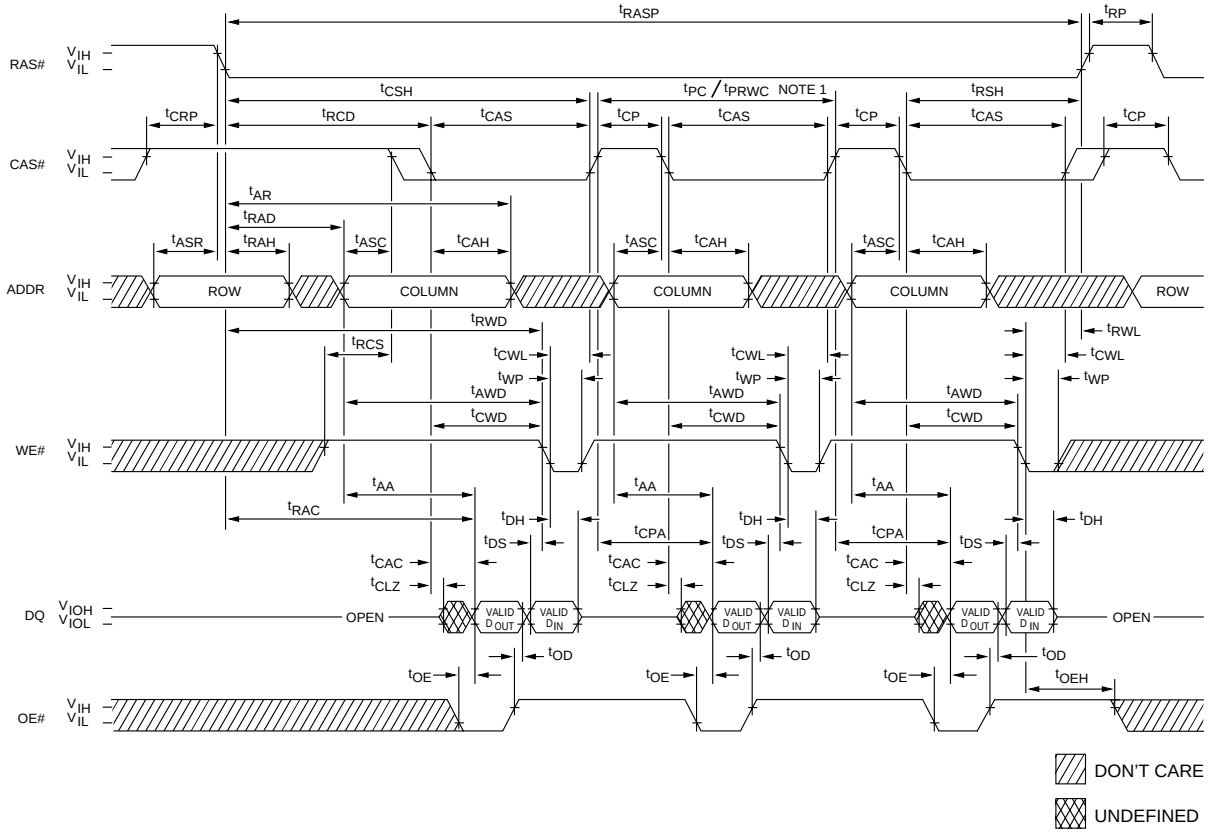



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tPC | 20 | | 25 | | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 5 | | 5 | | ns |

## EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



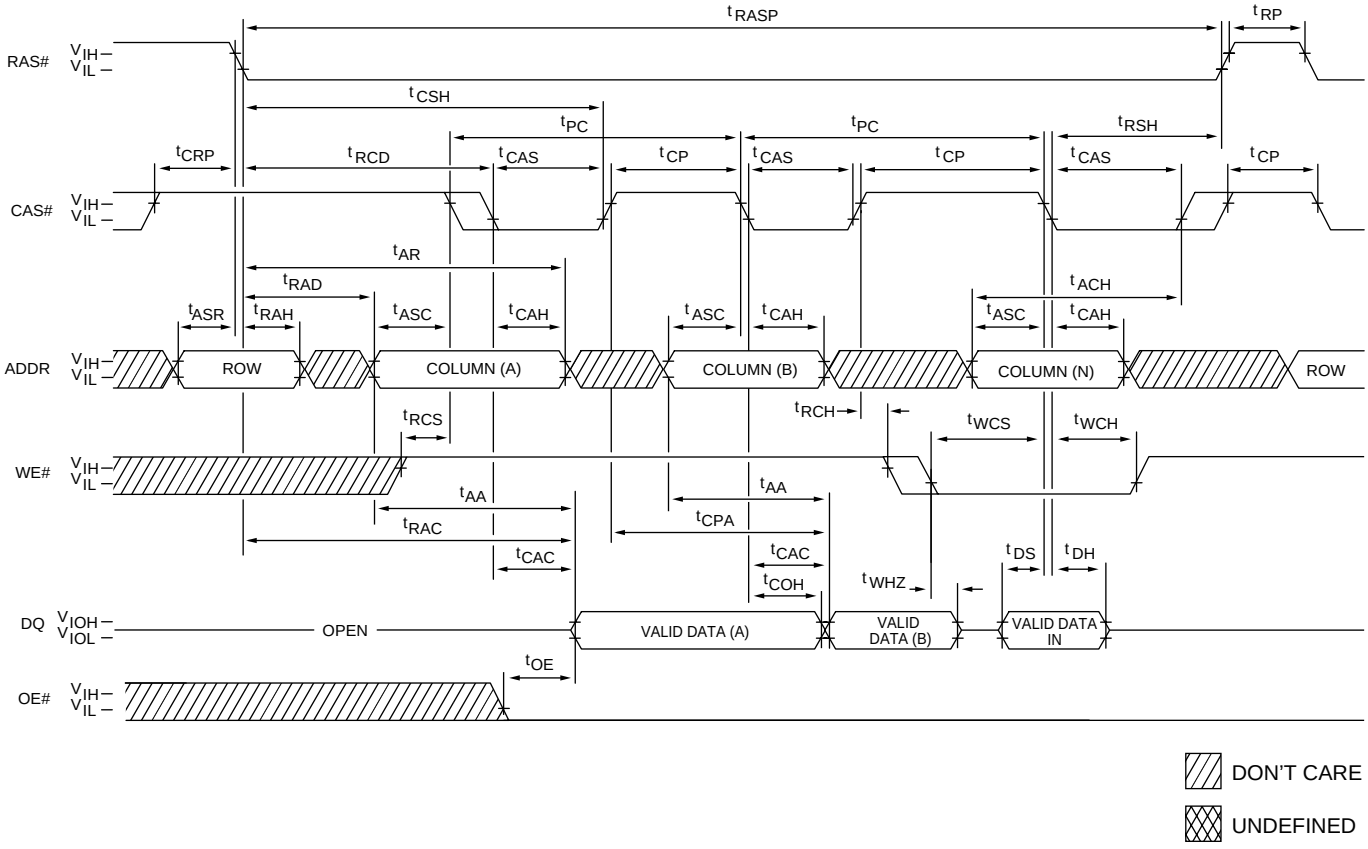

### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 42 | | 49 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWD | 28 | | 35 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tOEH | 8 | | 10 | | ns |
| tPC | 20 | | 25 | | ns |
| tPRWC | 47 | | 56 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWD | 67 | | 79 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWP | 5 | | 5 | | ns |

**NOTE:** 1. tPC is for LATE WRITE cycles only.

## EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

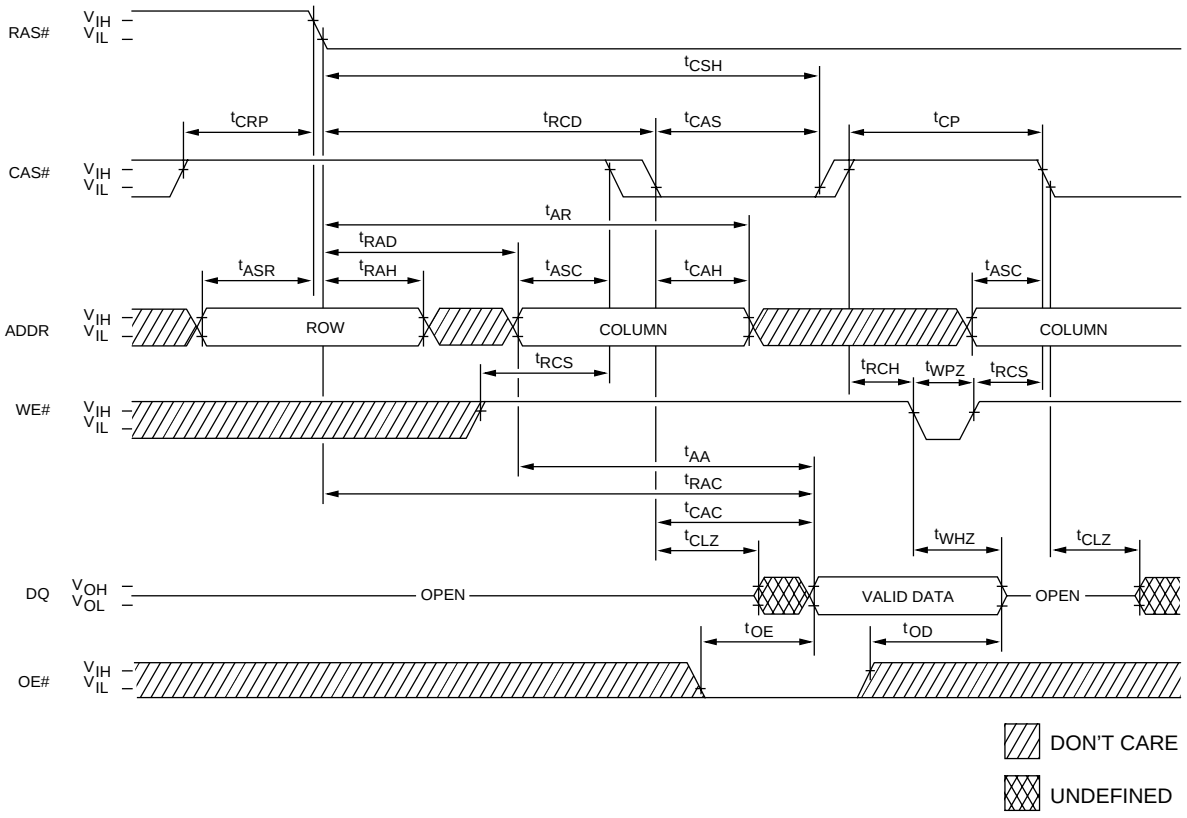



### TIMING PARAMETERS

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 12 | | 15 | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWHZ | 0 | 12 | 0 | 15 | ns |

## READ CYCLE
(With WE#-controlled disable)

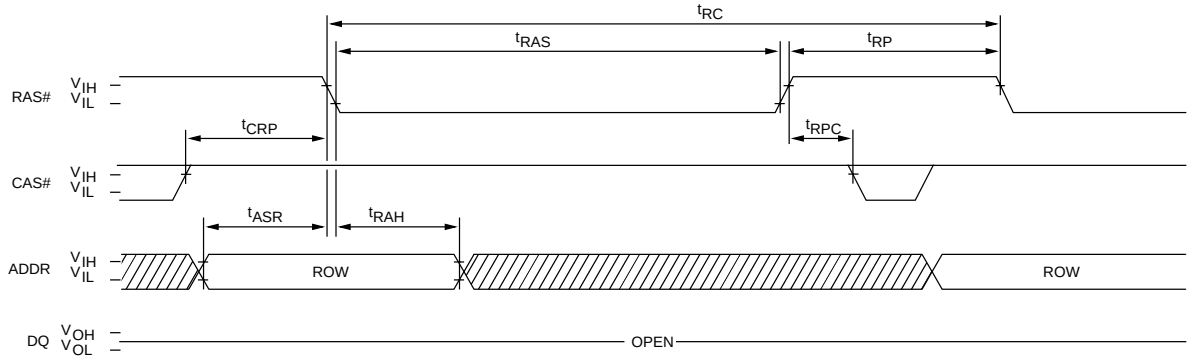



### TIMING PARAMETERS

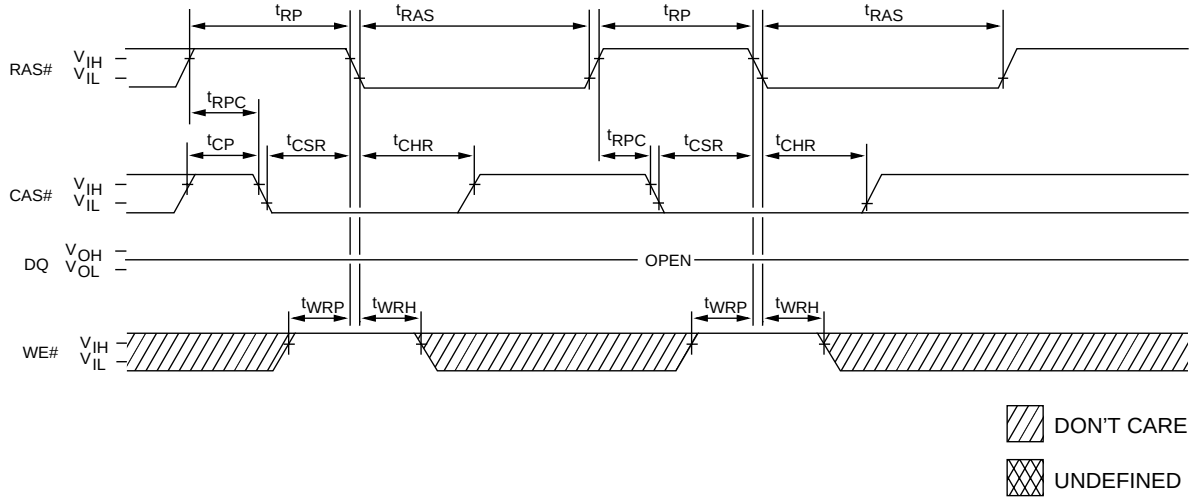
| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tWHZ | 0 | 12 | 0 | 15 | ns |
| tWPZ | 10 | | 10 | | ns |

## RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)




## CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)

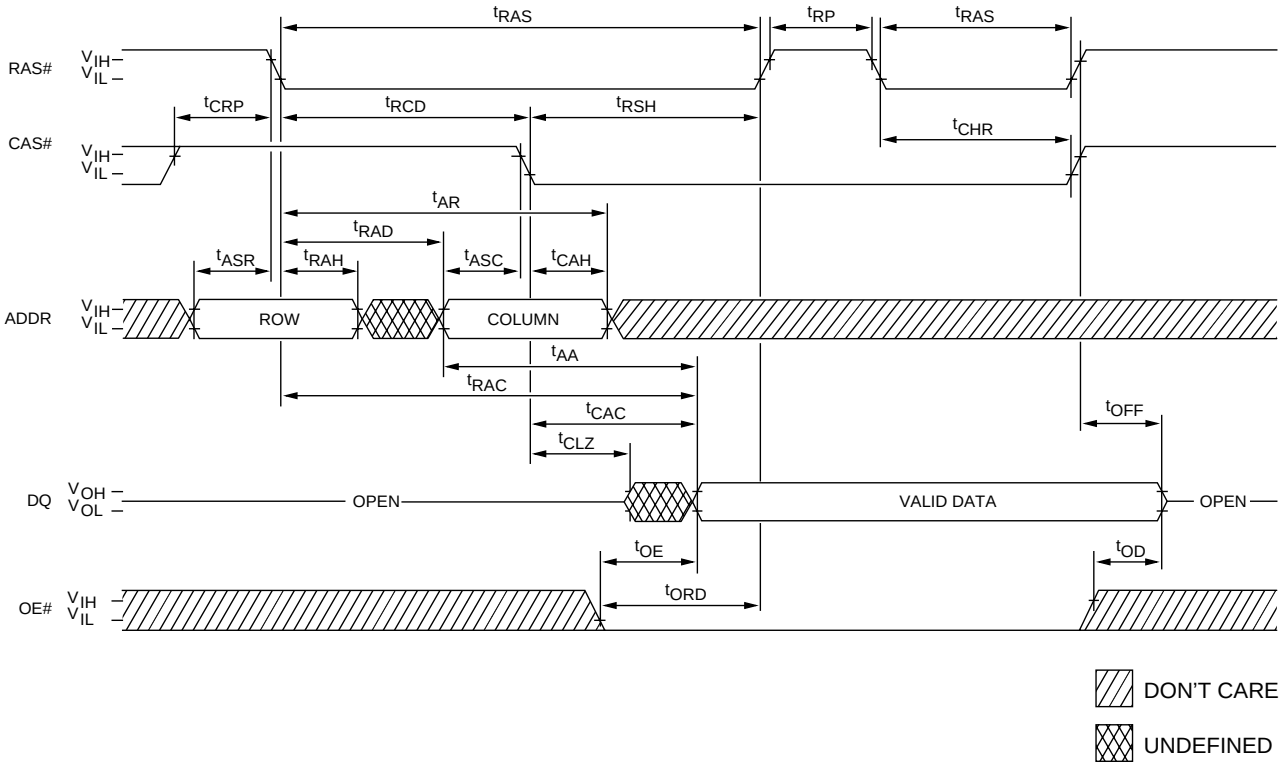



### TIMING PARAMETERS

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tASR | 0 | | 0 | | ns |
| tCHR | 8 | | 10 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSR | 5 | | 5 | | ns |
| tRAH | 9 | | 10 | | ns |

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRP | 30 | | 40 | | ns |
| tRPC | 5 | | 5 | | ns |
| tWRH | 8 | | 10 | | ns |
| tWRP | 8 | | 10 | | ns |

## HIDDEN REFRESH CYCLE [24]
(WE# = HIGH; OE# = LOW)



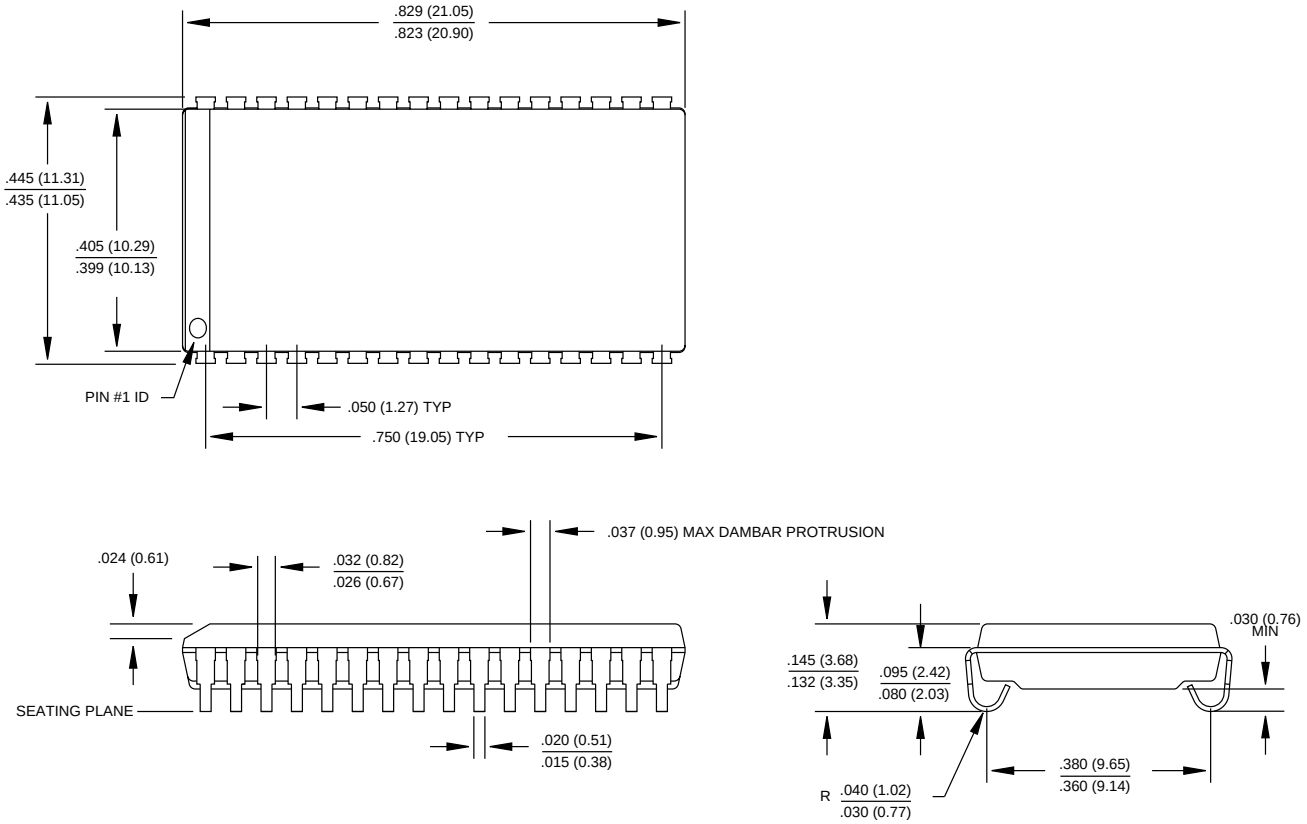

### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCHR | 8 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOE | | 12 | | 15 | ns |
| tOFF | 0 | 12 | 0 | 15 | ns |
| tORD | 0 | | 0 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |

## 32-PIN PLASTIC SOJ (400 mil)

DA-5

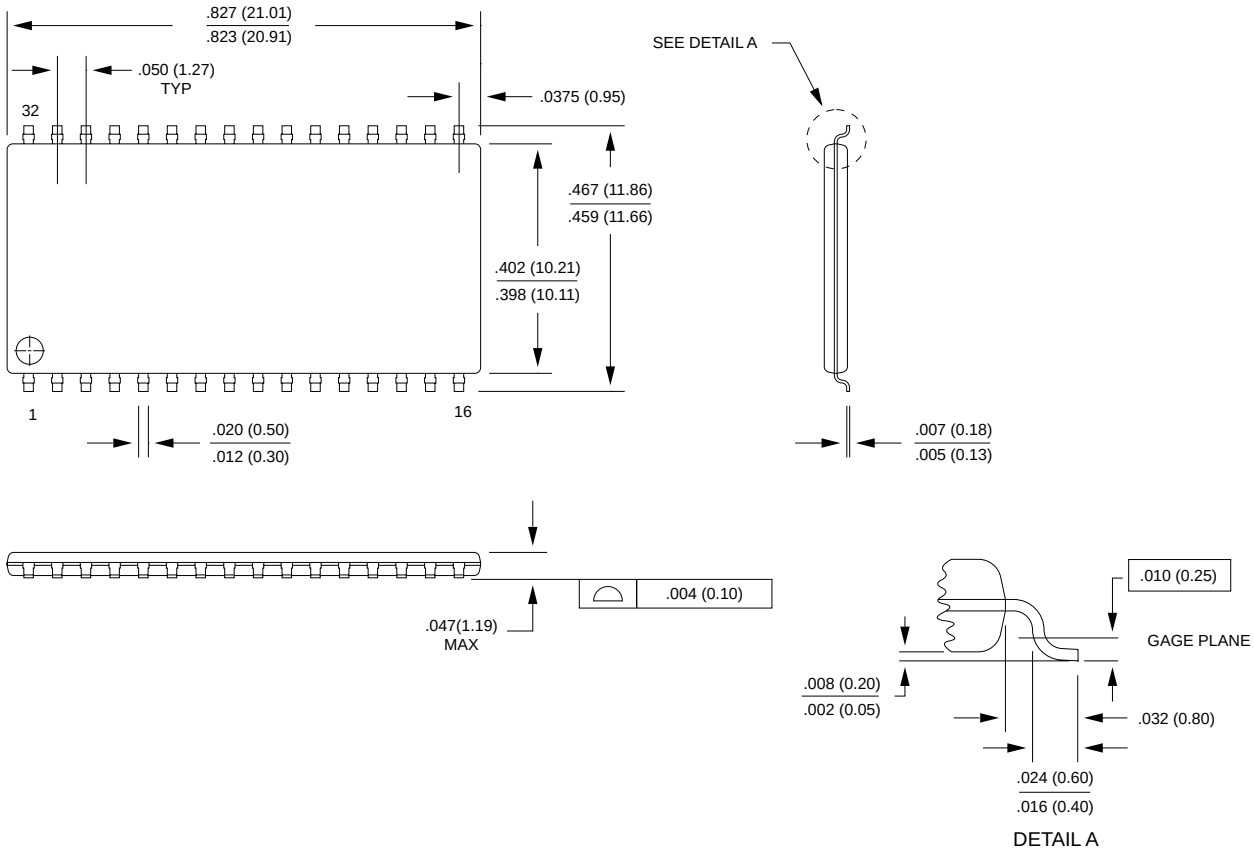



**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

## 32-PIN PLASTIC TSOP (400 mil)

DB-4




**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900, Micron DataFax: 208-368-5800
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